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⑤⁴ Reference voltage generator.

57) A CMOS circuit which can act as a current regulator for a variety of general MOS circuits. The circuit has current-biasing network connected to the source electrode of a first transistor. The drain electrode of the first transistor is connected to an input terminal of a current mirror arrangement. The output terminal of the current mirror is connected to the

drain electrode of a first diode-configured transistor. The source electrode of the first diode-configured transistor is connected to a second diode-configured transistor. By connecting output terminals at various nodes of the circuit, the current of a variety of MOS circuits may be regulated by the current-biasing network.

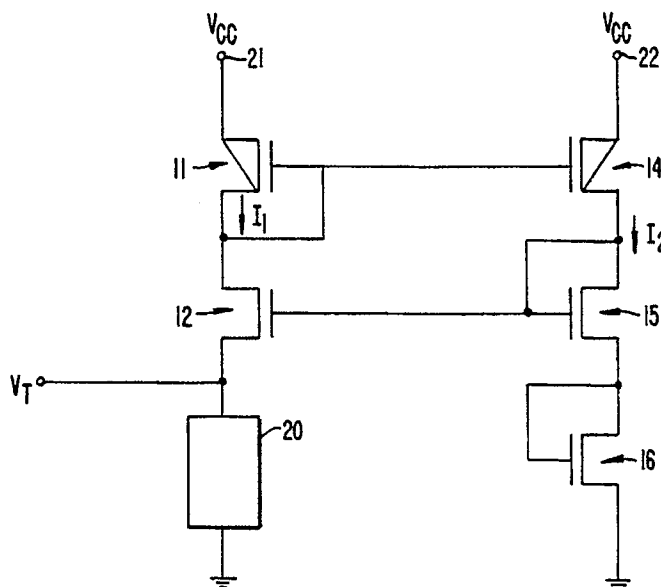


FIG. 1.

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The present application is related to integrated circuits and, in particular, to reference voltage generator circuits.

We will describe an integrated circuit regulator for controlling the current in a variety of MOS circuits. One type of circuit has a cascode transistor with its source electrode coupled to one voltage supply (ground) through a network and its drain electrode connected to an undefined network. Another type of circuit has simply a transistor having its source electrode connected to ground and its drain connected to an undefined network. A third type of circuit which could benefit from the current regulator of the present invention has a transistor with a source electrode connected to a second voltage supply (V_{CC}) and its drain electrode connected to an undefined network.

Typically with the general cascode transistor-current source MOS circuit there are currents nearly proportional to the square of the supply voltage, V_{CC} . Power dissipation is thus nearly proportional to the cube of V_{CC} . Thus, power dissipation can be a significant problem.

Another problem for this general circuit is that the current through the circuit typically varies with processing variations. For example, if processing is "good", the particular lot of integrated circuits has transistors with more current drive. If the processing has not been good, then the current drive of the processed transistor is not as large. Typically with better processing the threshold voltage, V_T , of the MOS transistors in the integrated circuit falls while the $\beta = \frac{1}{2} \mu_0 C_{OX}(W/L)$ of the individual transistors increases. These processing variations in the transistor device parameters result in operational currents in the general circuit and the integrated circuit containing this circuit to vary wildly depending upon the vagaries of processing.

The present invention solves or substantially mitigates these problems of the general cascode transistor-current source circuit. In one particular embodiment, the current flowing in the circuit is proportional to V_{CC} , not V_{CC}^2 , and is substantially independent of processing variations.

We will also describe a circuit for regulation for the other two types of general circuits.

We will describe a circuit which can act as reference voltage generator by providing for a reference voltage equal to the threshold voltage of MOS transistors, V_T .

We will describe an integrated circuit connected between a first voltage supply at V_{CC} and a second voltage supply at ground. The circuit has a current-biasing network connected to ground at one end and to the source electrode of a first MOS transistor at the other end. The current by the current-biasing network appears at the drain electrode of the first transistor. By a current mirror

arrangement this current is duplicated through a second transistor which is in a diode configuration. The gate electrode of the second transistor is connected to that of the first, while the second transistor's source electrode is connected to the drain electrode of the third transistor also in diode configuration. The source electrode of the third transistor is connected to ground.

By designing the device parameters of the first, second and third transistors such that β_1 is one-fourth β_2 and β_2 is equal to β_3 , then the voltage at the source electrode of the first transistor is substantially the threshold voltage V_T of the transistors.

If the current-biasing network comprises a fourth transistor in the linear mode, an output terminal can be connected to the gate electrode of the first transistor. By connecting this output terminal to parallel circuits in the integrated circuit which circuits have an MOS transistor connected to ground through a network, the current through each parallel current becomes regulated. By connecting the output terminal to the MOS transistor, which is operating as a cascode transistor, the current through the parallel circuit become substantially independent of processing variations. Furthermore, the current becomes proportional to V_{CC} , rather than V_{CC}^2 as is typical in such cascode transistor circuits. Thus power dissipation becomes less worrisome with a variable supply voltage.

Furthermore, by connecting output terminals to other nodes in the described circuit current regulation can also be provided for other types of general circuits.

Brief Description of the Drawings

Fig. 1 is a circuit diagram of one embodiment of the present invention.

Fig. 2 is a circuit diagram of another embodiment of the present invention in which the current-biasing network is a transistor in the linear mode.

Fig. 3 is a circuit diagram of one embodiment of the present invention which avoids startup problems.

Fig. 4 is a circuit diagram of one embodiment of the present invention which illustrates the various nodes available for current regulation, and,

Figure 5 is a circuit diagram of an alternative arrangement.

Specific Embodiments of the Invention

The present invention takes advantages of many of the benefits of integrated circuit technology. In an integrated circuit precise matching of

specific relationships of the operational characteristics of two or more devices are possible. For example, in the present invention the threshold voltage, V_T , of the NMOS transistors are designed to be equal. This is also true of the device parameters, such as channel width over channel length ratios, unless stated otherwise.

Fig. 1 shows a generalized concept of the present invention. The circuit has a current-biasing network 20 connected to ground and source electrode of an NMOS transistor 12. The drain electrode of the transistor 12 is connected to a current mirror arrangement of two PMOS transistors 11, 14. The transistor 11 has its drain electrode connected to its gate electrode, which is in turn connected to the gate electrode of the transistor 14. The source electrode of the transistor 11 is connected to a positive supply voltage at V_{CC} , typically +5 volts for MOS and CMOS circuits. Similarly, the source electrode of the PMOS transistor 14 is connected to the V_{CC} supply voltage.

Thus whatever current I_1 is drawn from the drain electrode of transistor 11 is supplied by the drain electrode of the transistor 14. I_1 is equal to I_2 .

The PMOS transistor 14 has its drain electrode connected to a drain electrode of an NMOS transistor 15. A source electrode of the transistor 15 is connected to the drain region of a NMOS transistor 16 having its source electrode connected to the second voltage supply at ground. Both NMOS transistors 15, 16 are connected as diodes, i.e., the gate electrode of each transistor is connected to the drain region of that transistor. Finally, the gate electrode of the transistor 15 is connected to the gate electrode of the transistor 12.

Since the current from the PMOS transistor 11 is equal to the current from the PMOS transistor 14, the drain current through transistor 12 is equal to the drain current through the transistor 15. Since both transistors are in the saturated mode,

$$\beta_{12}(V_{GS12} - V_T)^2 = \beta_{15}(V_{GS15} - V_T)^2$$

where

$$B_i = \frac{1}{2} \mu_0 C_{OX} (W_i/L_i)$$

and

V_{GSi} = the source/drain voltage for the transistor i.

With some manipulation,

$$(\beta_{15}/\beta_{12})^{1/2} V_{GS15} - V_{GS12} = V_T [(\beta_{15}/\beta_{12})^{1/2} - 1]$$

By setting the dimensions of transistor 15 with those of transistor 12 so that

$$\beta_{15} = 4\beta_{12},$$

then

$$2V_{GS15} - V_{GS12} = V_T$$

Assuming to the first order that V_{GS16} is approximately equal to V_{GS15} , i.e., that voltage on the substrate of the integrated circuit does not substantially affect the source-gate voltages of the two transistors 15, 16, thus

$$V_{GS16} + V_{GS15} - V_{GS12} = V_T$$

$$V_{20} \approx V_T$$

Thus the voltage across the current biasing network 20 is substantially V_T , which is determined by the particular steps used to manufacture the integrated circuit. An output terminal connected to the source electrode of the transistor 12 is thus set at threshold voltage of the NMOS transistors in the circuit. Furthermore, it should be noted that amount of current I_1 biased by the network 20 was not accounted for to fix the source electrode voltage at V_T .

Upon the startup of the described circuit, one possible but unstable state is the non-conducting state where none of the transistors are on. To avoid this possibility, a transistor 17 having its source electrode connected to ground and its drain electrode connected to the drain electrode of the transistor 11 can be added to the circuit as shown in Fig. 3. The gate electrode of the transistor 17 is at small reference voltage V_{CS} above ground so that small current always follows through the transistor 11 to turn it on at startup. This avoids the non-conducting state.

The present invention is also a current regulator. As shown in Fig. 4, various nodes in the circuit of the present invention may be used to generate reference voltages for controlling currents for different general circuits. If the node 21 is used for reference voltage V_{REF1} , then general circuits having a cascode transistor connected to ground through a network are suitable for current regulation. The gate electrode of the cascode transistor is connected to node 21, while the drain electrode of the transistor may be connected to an undefined network.

If node 22 is used, then a general circuit having a transistor with its source electrode connected to ground, its gate electrode connected to node 22 and its drain electrode connected to an undefined network may be current-regulated.

With node 23, a general circuit with a transistor having its source electrode connected to V_{CC} , its gate electrode connected to node 23 and its drain electrode connected to an undefined network is suitable.

In all three general circuits, the current is controlled by I_1 , the current set by the current-biasing network 20. Thus the network 20 can be a simple device, such as resistor R, to set the current independent at V_T/R as shown in Figure 5.

More interesting is the case where the network 20 acts like a transistor, or transistors, operating in the linear mode. As shown in Fig. 2, the network 20 is represented by a transistor 13 connected to operate in the linear model. Thus its gate electrode is connected to a relatively high voltage, in this case V_{CC} .

Since I_1 is equal to the current through the

transistor 13, which is in the linear mode,

$$I_1 = \beta_{17}[2(V_{GS17} - V_T)V_T - V_T^2] \\ = 2\beta_{17}V_{GS17}V_T - 3\beta_{17}V_T^2$$

Therefore,

$$I_1 \propto \beta_{17}V_TV_{GS17}$$

Thus the current flowing through the transistor 12 is proportional to the source-gate voltage of the transistor 17, which is V_{CC} . As noted previously, in most D.C. circuits the current is nearly proportional to V_{CC}^2 . Also, the major processing terms β_{17} and V_T tend to cancel changes in each other as processing variations become extreme. The present invention consumes much less power.

Thus if the node 21 at V_{REF1} is connected to the gate electrode of a cascode transistor which has its source electrode coupled to ground through a current supply as shown in Fig. 4, the present invention can regulate the current through the cascode transistor to reduce power and avoid the vagaries of semiconductor processing.

This type of connection is particularly useful where the network 20 mimicks the network connected to the source electrode of the cascode transistor. Thus the current through the cascode transistor tracks the desired range of currents suitable for the network connected to the drain electrode of the cascode transistor. Yet power consumption is restrained and the effects of processing variations are reduced.

One example of such an application of the present invention may be useful is found in a U. S. patent application, entitled "High Speed Differential Current Sense Amplifier," has been filed by the assignee and on the same date as the present invention. The inventors named on that application are William C. Plants and Scott Fritz. The patent application is incorporated herein by reference. If the network 20 is designed to duplicate the bit line network including one of the static RAM cell current sources which are selectively coupled to the bit lines described in the patent application, then the advantages above may be achieved in the circuit described in the incorporated reference.

While the description above provides a full and complete disclosure of the preferred embodiments of the present invention, various modifications, alternate constructions and equivalents may be employed without departing from the true scope and spirit of the invention. For example, the circuits of the inventions may be designed in standard BIC-MOS technology, rather than CMOS. Therefore, the present invention should be limited only by the metes and bounds of the appended claims.

Claims

1. An MOS integrated circuit connected be-

tween a first voltage supply and a second voltage supply for generating a reference voltage, comprising

a current-biasing device having first and second electrodes, said first electrode connected to said second voltage supply, said device having a first current through said second electrode;

a first transistor having first and second source/drain electrodes and a gate electrode, said first source/drain electrode connected to said second electrode of said current-biasing device;

a current mirror connected to said first voltage supply having first and second electrodes, said first electrode connected to said second electrode of said first transistor, said second terminal having a second current therethrough mirroring the current through said first electrode;

a second transistor in a diode configuration, said second transistor having first and second source/drain electrodes and a gate electrode, said second source/drain electrode connected to said second electrode of said current mirror, said gate electrode connected to said gate electrode of said first transistor; and

a third transistor in a diode configuration, said third transistor having a first and second source/drain electrodes, said second source/drain electrode connected to a first source/drain electrode of said second transistor, a first source/drain electrode connected to said second voltage supply; whereby the voltage at said first source/drain electrode of said first transistor is fixed at substantially the threshold voltage of said first transistor.

2. The integrated circuit as in claim 1 wherein the device parameters are such that β_1 equals β_2 where

$$\beta_1 = \frac{1}{2} \mu_0 C_{OX}(W/L) \text{ for the } i\text{th transistor.}$$

3. The integrated circuit as in claim 2 wherein the channel width over channel length ratio of said second transistor is approximately four times the channel width over channel length ratio of said first transistor.

4. The integrated circuit as in claim 1 wherein said current mirror comprises

a fourth transistor in diode-connected configuration having first and second source/drain electrodes and a gate electrode, said first source/drain electrode connected to said first voltage supply and said second/drain electrode comprising said first current mirror electrode; and

a fifth transistor having first and second source/drain electrodes and a gate electrode, said first source/drain electrode connected to said first voltage supply, said gate electrode connected to said fourth transistor gate electrode, and said second source/drain electrode comprising said second current mirror electrode.

5. The integrated circuit as in claim 4 wherein

said first, second, and third transistors are of one polarity type and said fifth and sixth transistors are of another polarity type.

6. The integrated circuit as in claim 5 wherein transistors of one polarity type are NMOS transistors and transistors of another polarity type are PMOS transistors.

7. The integrated circuit as in claim 1 wherein said current-biasing device comprises a resistor.

8. The integrated circuit as in claim 1 wherein said current-biasing device comprises sixth transistor operating in the linear mode, whereby the current through said first transistor is substantially independent of processing variations.

9. The integrated circuit as in claim 8 further comprising an output terminal connected to said gate electrode of said first transistor, said output terminal for connection to an electrical circuit comprising

a seventh transistor having first and second source/drain electrodes and a gate electrode, and a current source having first and second electrodes, said first electrode connected to said second voltage supply and said second electrode connected to said first source/drain electrode of said seventh transistor, whereby the current through said electrical circuit is substantially independent of processing variations.

10. The integrated circuit as in claim 2 further comprising a current source, said current source connected between said second source/drain electrode of said first transistor and said second voltage supply, whereby a non-conducting state in said integrated circuit is prevented.

11. An MOS integrated circuit for generating a reference voltage between a first supply voltage and a second supply voltage, comprising first, second and third transistors connected in series between said first supply voltage and said second supply voltage, said first transistor having a first source/drain electrode of said first transistor coupled to said first supply voltage and having a gate electrode connected to a second source/drain electrode, said third transistor having a first source/drain electrode coupled to said second supply voltage and having a gate electrode coupled to said predetermined such that said third transistor operates in the linear region; fourth, fifth and sixth transistors connected in series between said first supply voltage and said second supply voltage, said fourth transistor having a first source/drain electrode coupled to said first supply voltage and a gate electrode connected to said first transistor gate electrode, said sixth transistor having a first source/drain electrode coupled to said second supply voltage and a gate electrode connected to a second source/drain electrode, said

fifth transistor having a gate electrode connected to said second transistor gate electrode and to said second source/drain electrode of said fourth transistor;

an output terminal connected to said fifth transistor gate electrode;

whereby said output terminal voltage remains relatively independent of processing variations.

12. The MOS integrated circuit as in claim 11 wherein said predetermined voltage is substantially said first supply voltage.

13. The MOS integrated circuit as in claim 12 wherein said first and fourth transistors are a first polarity type and said second, third, fifth and sixth transistors are a second polarity type.

14. The MOS integrated circuit as in claim 13 wherein said first polarity type is PMOS and said second polarity type is NMOS.

15. The MOS integrated circuit as in claim 14 wherein the device parameters of said first and fourth transistors are predetermined such that the current through said first transistor is substantially equal to the current through said fourth transistor.

16. The MOS integrated circuit as in claim 15 wherein the device parameters of said second and fifth transistors are approximately equal so that V_T , the threshold voltage, of both transistors are substantially equal.

17. The MOS integrated circuit as in claim 16 wherein the channel width over channel length ratio of said fifth transistor is approximately four times the channel width over channel length ratio of said second transistor.

18. The MOS integrated circuit as in claim 17 wherein the device parameters of said fifth and sixth transistors are such that V_{GS} , the gate-source voltage, of said fifth and sixth transistors are substantially equal, whereby V_{DS} , the source-drain voltage, of said third transistor, is substantially V_T .

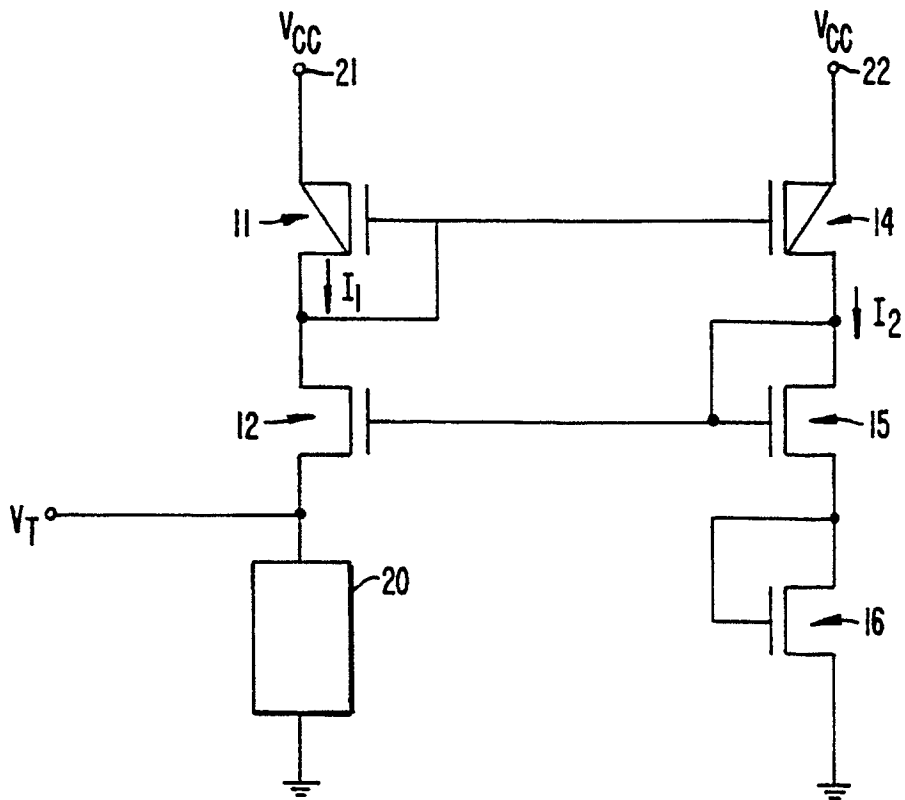


FIG. 1.

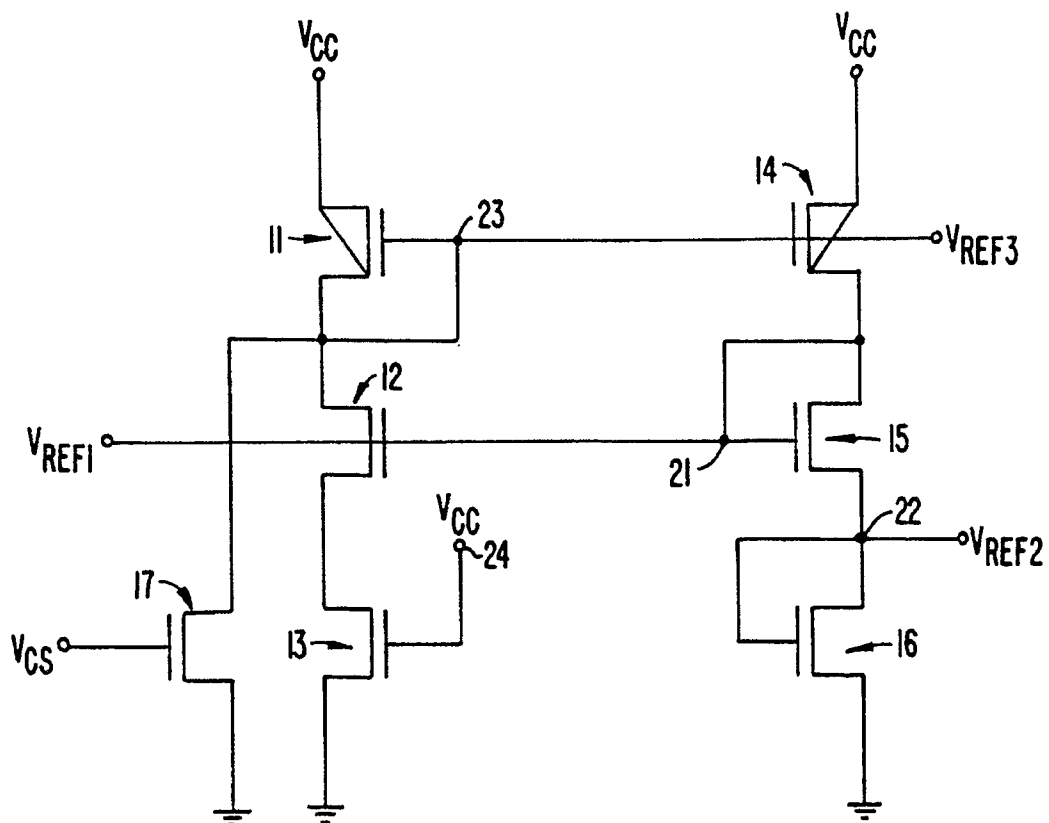


FIG. 2.

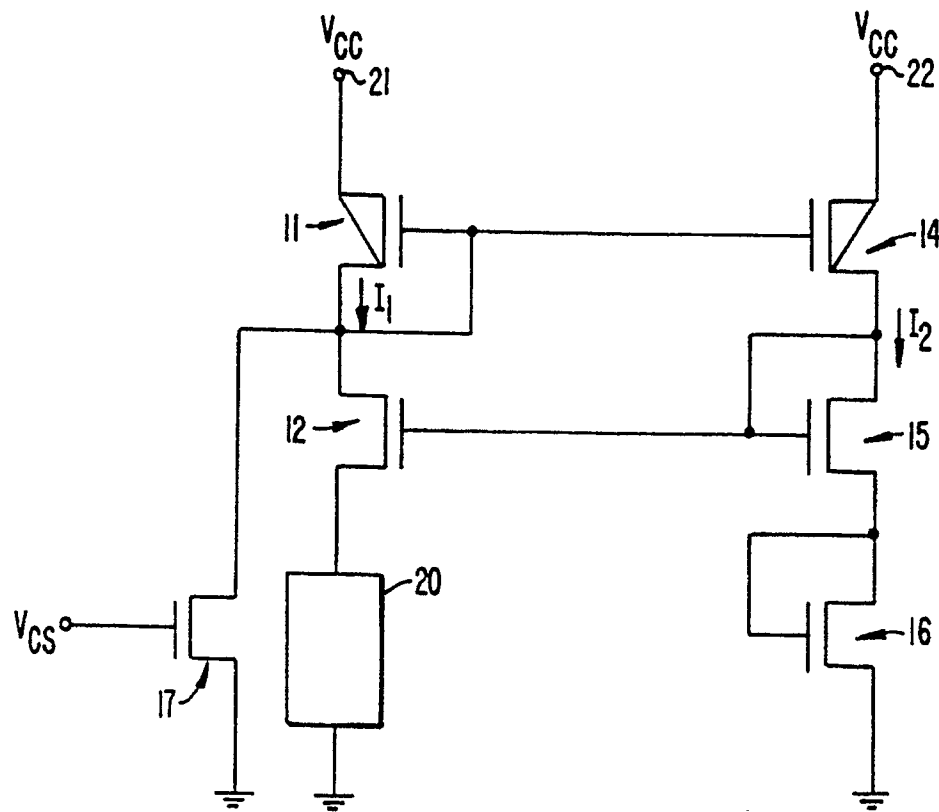


FIG. 3.

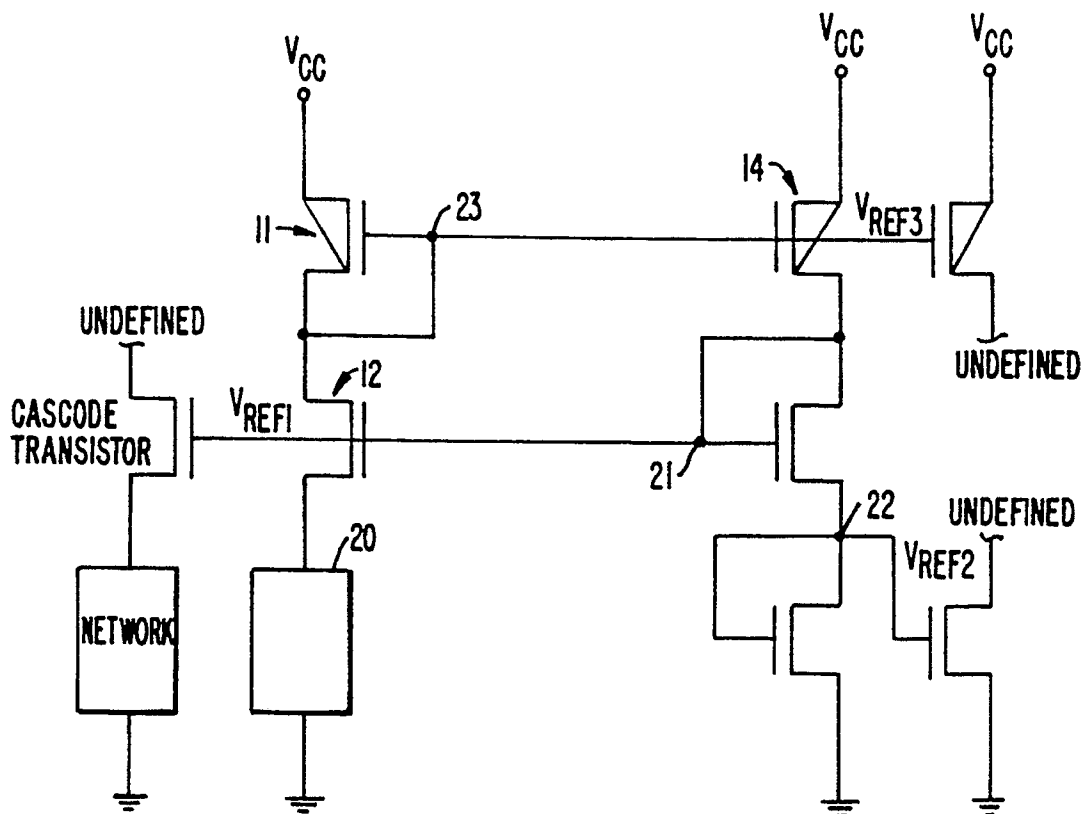


FIG. 4.

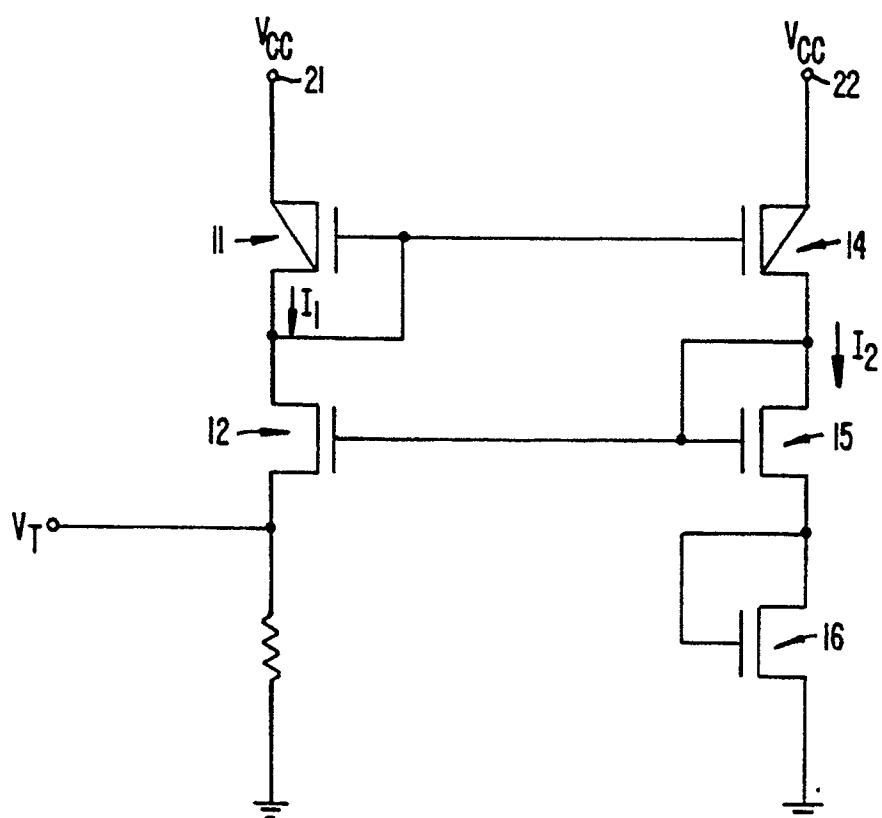


FIG. 5.



European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP 90 30 4863

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	RESEARCH DISCLOSURE. no. 281, September 1987, New York US page 572 J.K. MORIARTY Jr.: "FET Threshold Voltage Generator" * the whole document *	1-7	G05F3/24 G05F3/28
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 116 (P-452)(2173) 30 April 1986, & JP-A-60 245007 (MITSUBISHI) 4 December 1985, * the whole document *	1	
A	US-A-4477737 (R.W. ULMER) * abstract; figure 2 *	1	
A	US-A-4723108 (C.N. MURPHY) * abstract; figure 1 *	1	
A	GB-A-2081940 (STANDARD TELEPHONES AND CABLE LTD) * abstract; figure 1 *	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G05F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 29 JUNE 1990	Examiner ZAEGEL B.C.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		I : theory or principle underlying the invention F : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	