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(71) Applicant: **N.V. Philips' Gloeilampenfabrieken**
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(72) Inventor: **Lorteije, Jean Hubertus Josef**
c/o INT. OCTROOIBUREAU B.V., Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(74) Representative: **Kooiman, Josephus Johannes Antonius et al**
INTERNATIONAAL OCTROOIBUREAU B.V.
Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(54) Driving circuit for a matrix display device.

(57) The matrix (MX) comprises row and column conductors (L and C, respectively) in which pixels (P) are present between conductor crossings, which pixels can be excited by means of a row selection and a specific column drive with an excitation pulse from an associated column drive circuit (CD1, CD2, CD3, etc.). For performing a pulse width modulation there is a pulse counting circuit (CC) for each column conductor (C), which circuit has inputs (I) for supplying an excitation pulse number, an enable input (EI) and a clock pulse input (CLI), while after enabling and under the supply of clock pulses the counting circuit (CC1) counts from the excitation pulse number to a reference number which leads to a counting period corresponding to the excitation pulse number, which counting period determines the period of the excitation pulse via a column drive stage (DS1) coupled to outputs $\overline{(Q)}$ of the counting circuit (CC1). To be able to optionally perform a colour adaptation in the case of colour display, in which the pixels (P) each with their primary colour (R, G, B) are grouped in composite colour pixels (P11, P12, P13), the frequency (fR, fG, fB) of the clock pulses (CLR, CLG, CLB) for the counting circuits (CC) is different for at least two primary colours.

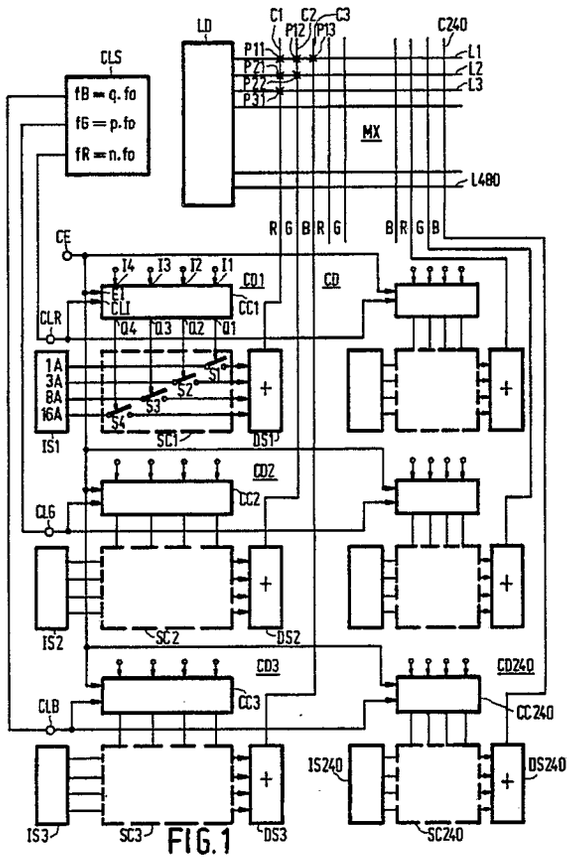

FIG.1

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Matrix display device.

The invention relates to a matrix display device, comprising a matrix of row and column conductors in which pixels are present between conductor crossings, which pixels can be excited by means of a row selection and a specific column drive with an excitation pulse, each column conductor being coupled to a column drive circuit comprising a counting circuit for each column conductor and having inputs for the supply of an excitation pulse number, an enable input and a clock pulse input, while after enabling and under the supply of clock pulses the counting circuit counts from the excitation pulse number to a reference number which leads to a counting period corresponding to the excitation pulse number, which counting period determines the period of the excitation pulse via a column drive stage coupled to outputs of the counting circuit.

Such a matrix display device is known from United States Patent 4,353,062. Dependent on the clock pulse count either down or up to the reference number which is a maximum or minimum and which is equal to, for example zero, the excitation pulse which is pulse-width modulated by the counting period is generated. Said Patent describes a drive circuit which also operates with pulse amplitude modulation.

The said Patent does not describe any specific measures for using the display device for colour display in which the pixels, each with their primary colour are grouped in composite colour pixels.

It is an object of the invention to realise a simple colour adaptation upon display when using such a display device. To this end a matrix display device according to the invention is characterized in that when using the display device for colour display, in which the pixels, each with their primary colour are grouped in composite colour pixels, the frequency of the clock pulses for the counting circuits is different for at least two primary colours.

As a result the excitation pulse period for the pixels of these primary colours is no longer only dependent on the associated excitation pulse number but is also dependent on the associated clock pulse frequency, which yields a simple possibility of colour adaptation.

An embodiment of the matrix display device according to the invention which leads to a display device having an optionally selectable colour adaptation is characterized in that at least two clock pulse frequencies are adjustable.

A further embodiment providing a colour adaptation having sufficient possibilities in practice is characterized in that an adjustability factor of the order of two to four increasing the clock pulse frequency is provided.

An embodiment for use with a colour mosaic filter is characterized in that the clock pulses can be applied to the counting circuits via a multiplex circuit.

The invention will be described in greater detail by way of example with reference to the accompanying drawings in which

Fig. 1 is a block diagram of a matrix display device according to the invention and

Fig. 2 shows a different colour pixel structure at the matrix.

In Fig. 1 the reference MX denotes a matrix of crossing row conductors L and column conductors C. A number of row conductors L1, L2, L3 to L480 and a number of column conductors C1, C2, C3 to C240 are shown by way of example. Pixels P are present between the conductor crossings, showing pixels P11, P12, P13 of the first row L1, P21 and P22 of the second row L2 and pixels P31 of the third row L3. The row conductors L are connected for the known row selection to outputs of a row drive circuit LD. The column conductors C are connected for a specific column drive by means of an excitation pulse to outputs of a column drive circuit CD. The circuit CD is connected to outputs of a clock pulse source CLS which according to one aspect of the invention supplies clock pulses at different clock pulse frequencies. Thus, Fig. 1 shows a matrix display device (MX, LD, CD, CLS) in which the references R, G and B show respective red, green and blue colour filter strips so as to indicate that it is suitable for colour display. The light-transmitting strips thus coloured are arranged in the column direction so that colour pixels located in the row direction are formed for which a colour pixel (P11, P12, P13) is mentioned as an example.

The display device (MX, LD, CD, CLS) can be used for colour television or for the coloured display of graphic or other data and may comprise gas discharge display cells, light-emitting diodes, liquid crystals, etc. Independent of the specific pixel structure it is presupposed that it is desirable to perform a colour adaptation upon display. As an example this presupposition is based on pixels formed with liquid crystals which operate as light switches. A light source, artificial or the sun, is assumed to be present for which the liquid crystal as a light switch determines the transmitted and/or reflected light intensity at the red, green or blue pixel. The light intensity ratio determines the colour of the composite colour pixel. This colour is further determined by the own colour of the light from the light source. Furthermore, different filter thicknesses for the red, green and blue colour filters influ-

ence the ultimate colour of the composite colour pixel. Dependent on lamp or ambient light colour, different colour filter thicknesses, the desire for a given picture colour upon display etc., there is a need of a facility to adapt the colour. According to the invention this facility is provided in a simple manner by the use of different clock pulse frequencies, as is denoted in Fig. 1 at the clock pulse source CLS by the clock pulse frequencies fR = n.f0, fG = p.f0 and fB = q.f0 in which n, p and q are multiplication factors which are equal to or larger than 1 and for which it holds that at least two of the factors n, p and q are different.

The facility to adapt the colour is realised, inter alia by applying to three separate input terminals CLR, CLG and CLB of the column drive circuit CD clock pulses indicated by the same references and having the respective frequencies fR, fG and fB. Three separate groups of column drive circuits the first of which being denoted by CD1, CD2 and CD3 follow the terminals CLR, CLG and CLB in the circuit CD. The last column drive circuit subsequent to the terminal CLB is denoted by CD240. The first circuit CD1 subsequent to the terminal CLR is shown in greater detail and will be described by way of example for the other circuits.

The column drive circuit CD1 comprises a counting circuit CC1 having inputs I1, I2, I3 and I4 for the supply of an excitation pulse number, an enable input EI, a clock pulse input CLI and outputs Q1, Q2, Q3 and Q4. The input terminal conveying the clock pulses CLR is connected to the clock pulse input CLI. The enable input EI is connected to a terminal CE for the supply of an enable signal to be referred to similarly. Fig. 1 shows that the terminal CE is connected to all column drive circuits CD1, CD2, CD3 to CD240. A, for example 4-bit excitation pulse number associated with the instantaneous pixel between the column conductor C1 and the selected row conductor L is applied in known manner (not shown) to the inputs I1, I2, I3 and I4. For the 4-bit choice there are 15 possible excitation levels at the pixel P under the supply of one of the numbers from 0001 to 1111. After the supply of all excitation pulse numbers a joint enabling operation via the enable signal CE follows, whereafter under the supply of the clock pulses CL each counting circuit CC counts from its own excitation pulse number to a reference number, for example 0000. This may be effected by means of an up-counting or a down-counting operation. The resultant counting period is fixed by both the excitation pulse number and the clock pulse frequency fR, fG and fB.

For obtaining the excitation pulse for the pixel corresponding to the counting period, Fig. 1 shows a column drive stage DS1 connected to the column conductor, a switching circuit SC1 and a current source circuit IS1. On-off switches S1, S2, S3 and S4 in the switching circuit SC1 are controlled from the outputs Q1, Q2, Q3 and Q4, respectively, via which switches S outputs of the current source circuit IS1 conveying respective currents A, 3A, 8A and 16A are connected to inputs of a circuit DS1 shown as an adder stage (+). For a more detailed description of the operation of the circuit CD1 with the components CC1, SC1, IS1 and DS1, reference is made to the previously mentioned United States Patent 4,353,062. Apart from the fact that the circuit CD1 provides for a pulse width modulation, there is also a pulse amplitude modulation.

To illustrate the facility of colour adaptation the following is stated as an example, starting from the colour television standard with Y = 0.3 R + 0.59 G + 0.11 B for the luminance Y, with R = G = B = 1 for peak white and with R = G = B = 0 for black. It is assumed that n = p = q (fR = fG = fB) so that the same excitation pulse number for the pixels of a composite pixel implies that this has a white colour. If a greenish picture is desired, for example the following factors are chosen: n = 2, p = 1 and q = 2. A pixel which is originally white and has the same excitation pulse number for all three colours is now displayed with the original counting period for green but with half the counting period for red and blue. In fact, the clock pulse frequencies fR and fB are twice the clock pulse frequency fG. If one further proceeds to the factors n = 2, p = 1 and q = 4, with fB = 2 fR = 4 fG, the primary colour blue is considerably reduced and the primary colour red is relatively increased so that a yellowish tint appears in the greenish image.

In practice, it appears that an adjustability of the factors n, p, and q up to the order of two to four results in the desired colour adaptations.

The matrix MX with pixels P shown in Fig. 1 has colour strips R, G and B arranged in the column direction. The composite colour pixels (R, G, B) occur in the row direction and the pixel (P11, P12, P13) has been given by way of example. Fig. 2 shows a different colour pixel structure, namely with a colour mosaic filter. In this case different primary colours occur in the column direction, as is illustrated at the column conductor C1 by means of R, B, G, R at the row conductors L1, L2, L3, L4. The column conductors C must be driven in a cycle over three row conductors L, which is illustrated by means of a solid line L1, a broken line L2, a dotted line L3 and a solid line L4. In Fig. 2 the drive is shown for six column conductors C1 to C6 in which the R, G, B sequence of Fig. 1 in the row direction is present at the row conductors L1 and L4.

The column drive circuit CD is shown with six column drive circuits CD1 to CD6 all of which have

three inputs for supplying the clock pulses CLR, CLG or CLB in the said cycle. For the sake of simplicity the inputs for the supply of the excitation pulse numbers are not shown. It is evident that for the clock pulse cycle (CLR, CLG, CLB) excitation pulse numbers are also cyclically applied for red, green and blue to each circuit CD1, CD2, etc. For the cyclic clock pulse supply a multiplex circuit MUX is shown in Fig. 2 with three change-over switches MR, MG and MB each having a main contact T0 and three selector contacts T1, T2 and T3. To illustrate the simultaneous through-connections of the contacts T1, T2 and T3 with T0, these are shown by means of solid, broken and dotted lines. The reference 3LS denotes a switching terminal to which a switching signal denoted by the same reference is applied, which has a period which is equal to the said cycle. The main contacts T0 of the change-over switches MR, MG and MB are connected to the input terminals CLR, CLG and CLB, respectively, which are connected to an output of the clock pulse source CLS.

The clock pulse distribution over the column drive circuits CD1 to CD6 is described by way of example at the through-connection of the contacts T0 and T1. The circuits CD1 and CD4 receive the clock pulses CLR, the circuits CD2 and CD5 receive the clock pulses CLG and the circuits CD3 and CD6 receive the clock pulses CLB. The references R, G and B denote the processing of the relevant red, green and blue colour at the connection lead. In the cycle the signals of the colours R, B and G às associated with the column conductors C1 and C4 and the row conductors L1, L2 and L3 are indicated at the connection leads. In a corresponding manner the signals of the colours G, R, B and B, G, R are indicated at the connection leads between the circuits CD2 and CD5 and CD3 and CD6, respectively.

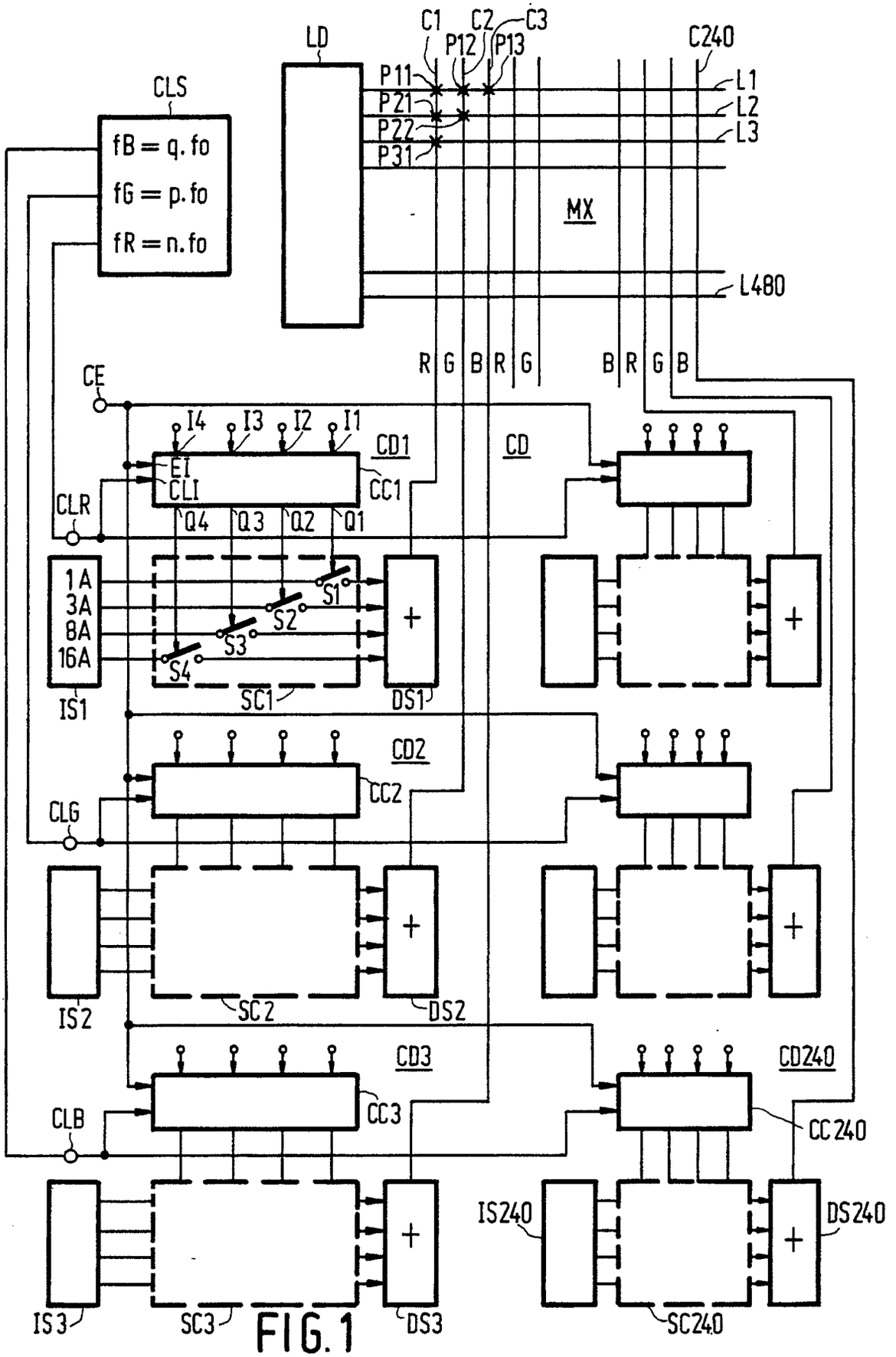
Claims

1. A matrix display device, comprising a matrix of row and column conductors in which pixels are present between conductor crossings, which pixels can be excited by means of a row selection and a specific column drive with an excitation pulse, each column conductor being coupled to a column drive circuit comprising a counting circuit for each column conductor and having inputs for the supply of an excitation pulse number, an enable input and a clock pulse input, while after enabling and under the supply of clock pulses the counting circuit counts from the excitation pulse number to a reference number which leads to a counting period corresponding to the excitation pulse number, which counting period determines the period of the excitation pulse via a column drive stage coupled to outputs of the counting circuit, characterized in that when using the display device for colour display, in which the pixels each with their primary colour are grouped in composite colour pixels, the frequency of the clock pulses for the counting circuits is different for at least two primary colours.

2. A matrix display device as claimed in Claim 1, characterized in that at least two clock pulse frequencies are adjustable.

3. A matrix display device as claimed in Claim 2, characterized in that an adjustability factor of the order of two to four for increasing the clock pulse frequency is provided.

4. A matrix display device as claimed in Claim 1, 2 or 3, comprising a colour mosaic filter characterized in that the clock pulses can be applied to the counting circuit via a multiplex circuit.


LD
C1
C2
C3
P12
P13
C240
CLS
fB = q. fo
fG = p. fo
fR = n. fo
P11
P21
P22
P31
L1
L2
L3
MX
L480
R G B R G
B R G B
CE
I4 I3 I2 I1
CD1
CD
EI
CLI
CC1
CLR
Q4 Q3 Q2 Q1
1A
3A
8A
16A
S1
S2
S3
S4
IS1
SC1
DS1
CD2
CC2
CLG
IS2
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CC3
CC240
CLB
IS240
DS240
IS3
SC3
DS3
SC240

FIG.1

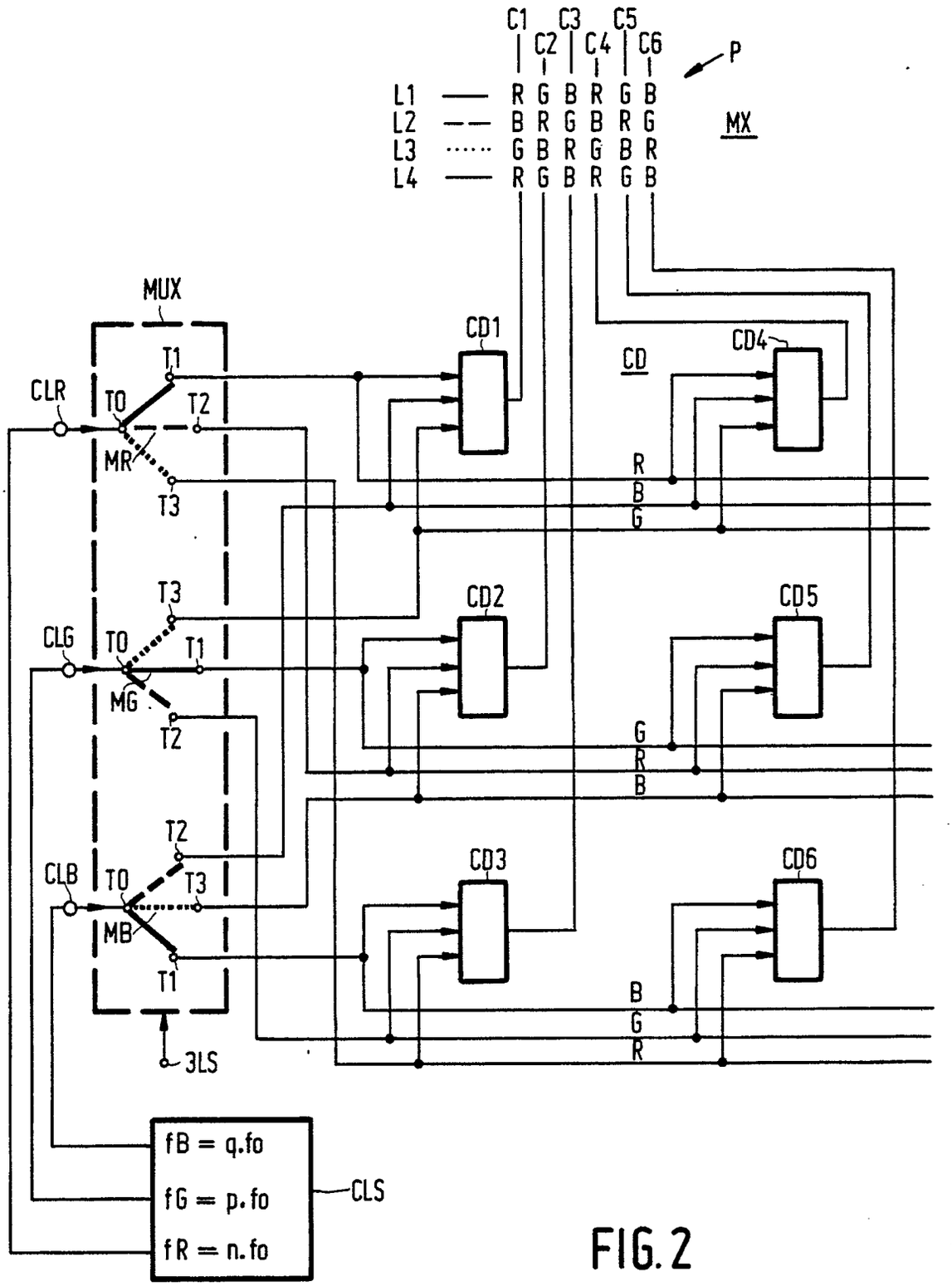
C1
C3
C5
C2
C4
C6
P
L1 R G B R G B
L2 B R G B R G
L3 G B R G B R
L4 R G B R G B
MX
MUX
CD1
CD4
CD
T1
CLR
T0
T2
MR
T3
R
B
G
T3
CD2
CD5
CLG
T0
T1
MG
T2
G
R
B
T2
CD3
CD6
CLB
T0
T3
MB
T1
B
G
R
3LS
fB = q.fo
fG = p.fo
fR = n.fo
CLS

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number

EP 90 20 1436

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A,D	US-A-4 353 062 (J.H.J. LORTEIJE) * Figure 1; abstract; column 4, line 27 - column 5, line 64 *	1	G 09 G 3/20
A	EP-A-0 260 146 (IBM CORP.) * Figures 1,2; abstract; column 3, line 19 - column 4, line 49 *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 09 G
H 04 N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31-01-1990	VAN ROOST L.L.A.

CATEGORY OF CITED DOCUMENTS

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