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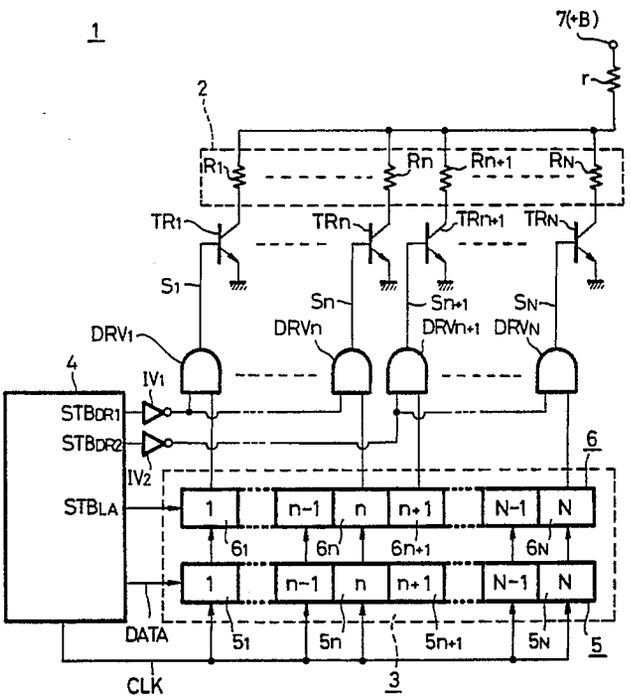
(54) Thermal printing apparatus.

(57) A thermal printing apparatus (1) comprises a printing head (2) having a plurality of heating devices (R) for printing an image, and a driving device (4, 5, 6) for driving the heating devices (R) so as to gradate the image, wherein the plurality of heating devices (R) are grouped into a plurality of blocks and the driving device (4, 5, 6) drives the printing head (2) sequentially at each block in dependence on each required gradational level.

FIG. 4



THERMAL PRINTING APPARATUS

This invention relates to thermal printing apparatus and methods of thermal printing.

In a previously proposed method of thermal printing, full-heating resistance elements R1, R2, ..., RN (Figure 1) are divided into two blocks, and the elements R1 to RN are turned ON and OFF block by block, thereby to perform the printing. This will be further described with reference to Figures 1 and 2A to 2F.

Figure 1 shows the arrangement of a thermal printing apparatus 1 including a linear thermal printing head 2 comprising N heating resistance elements (N = 640, for example) with n elements R1, R2, Rn forming one block and n elements Rn + 1, ..., Rn forming another block. A drive control circuit 3 comprises an N-stage head shift register 5 (51 to 5n and 5n + 1 to 5N) and N head latch circuits 6 (61 to 6n and 6n + 1 to 6N). A system controller in is formed of a microcomputer, and N drive signal output circuits DRV1, DRV2, DRVn, DRVn + 1, DRVN are provided, each of which is formed of an AND circuit.

N NPN transistors TR1, TR2, ..., TRn, TRn + 1, ..., TRN are provided to drive the printing head 2. Drive signals S1 to Sn and Sn + 1 to SN from the output circuits DRV1 to DRVN are respectively supplied to the bases of the transistors TR1, TR2, ..., TRn, TRn + 1, TRN, whose collectors are connected through the elements Ri to RN to a power supply terminal 7 to which a positive DC voltage (+B) is connected. The emitters of the transistors TR1 to TRN are earthed.

Serial printing data DATA (Figure 2B) of one line period are generated from the system controller in and are fed to the shift register 5, in which the data DATA are shifted in response to a clock pulse signal CLK (Figure 2A) from the system controller in. Data contents from the register stages 51 to 5n and 5n + 1 to 5N are respectively supplied to the N latch circuits 6, and are thereby latched in response to latch strobe pulse signals STBLA1 and STBLA2 (Figures 2C and 2D) from the system controller in. Outputs from the N latch circuits 6 are respectively supplied to the output circuits DRV1 to DRVN. Drive strobe signals STBDR1 and STBDR2 (Figures 2E and 2F) are generated from the system controller in and are fed through inverters IV1 and IV2 to the output circuits DRV1 to DRVn and DRVn + 1 to DRVN, respectively.

The serial printing data DATA from the system controller in are accumulated in all the register stages 51 to 5N in response to N pulses of the clock pulse signal CLK. Then, the data stored in the register stages 51 to 5n are latched by the n latch circuits 61 to 6n in response to the latch strobe pulse STBLA1 from the system controller 4. If the cycle of the clock pulse signal CLK is taken as τ, the data accumulated in the register stages 51 to 5n are latched in the N latch circuits 61 to 6n during a predetermined period (that is, predetermined period $\geqq N_\tau = t$). den data DATA of logic [L] (low) level of the printing data DATA latched in the n latch circuits 6 are supplied to the output circuits (AND circuits) DRV1 to DRVn, if the drive strobe signal STBDR1 is at logic [L] level, outputs of logic [N] (high) level are generated from the output circuits DRV1 to DRVn, whereby the transistors TR1 to TRn which are respectively supplied with the outputs of the circuits DRV1 to DRVn are turned ON to cause the elements R1 to Rn to be energised for a predetermined heating-process time ($\geqq N_\tau$, Figure 2A), whereby the printing of 1/2 line (left-hand half portion of one line) is effected on a printed sheet.

The data accumulated in the register stages 5n + 1 to 5N are latched in the n latch circuits 6n 1 to 6N in response to the latch strobe signal STBLA2 during a predetermined period ($\geqq N_\tau$) where τ is a cycle of the clock pulse signal CLK. When data DATA of logic [LJ level in the printing data latched in the N latch circuits 6 are supplied to the output circuits DRVn + 1 to DRVN, if the drive strobe signal STBDR2 is at logic [L] level, outputs of logic [N] level are generated from the output circuits DRVn + 1 to DRVN, whereby the transistors TRn + 1 to TRN which are respectively supplied with the outputs from the circuits DRV1 to DRVn are turned ON to energise the resistance elements Rn + 1 to RN for a predetermined heating-process time ($\geqq N_\tau$, Figure 2A), whereby the printing of the other 1/2 line (right-hand half portion of one line) is effected on the printing sheet.

Printing with M gradation will be described next. If, for example, M = 5, there are five gradations from 0th order gradation, where printing is not carried out, to 4th order gradation where the printing is darkest.

When printing of the 0th order gradation to the (M-1)th order gradation is carried out, as shown in Figure 2D, the elements are energised to perform the printing with the lst order gradation to the (M-1)th order gradation during a first heating-process time T1, the printing with the 2nd order gradation to (M-1)th order gradation is performed during a next heating-process time T2, the printing with the 3rd order gradation to (M-1)th order gradation is performed during a next heating-process time T3, ..., then the printing of the (M-1)th order gradation is performed during the final heating-process time

TM-1. In that case, during the heating-process time TM to TM-1 of the 1st order gradation to the (M-1)-th order gradation, the drive strobe signal STBDR1 or STBDR2 supplied to the inverter IV1 or IV2 from the system controller 4 is at logic [L] level, and this period is referred to as a printing period ST.

Whereas, during a period T0 of the 0th order gradation in which printing is not carried out, the drive strobe signal STBDR1 or STBDR2 is at logic [N] level. The interval between the adjacent pulses of each of the above-described latch strobe pulse signals STBLA1 and STBLA2, that is, the durations of the heating-process times T1 to TM-1 are determined such that they become shorter as the gradation approaches the oth order gradation (white), while they become longer as the gradation approaches the (M-1)th order gradation (darkest), considering the gamma characteristics from a visual standpoint when a user sees a printed image on the printing sheet.

This will be described with reference to Figure 3, in which A and B designate blocks of the plurality of heating resistance elements RI to RN which form the thermal printing head 2. The blocks A and B are respectively formed of the resistance elements R1 to Rn and Rn 1 to RN. To the right of numerals indicating respective gradations, that is, numerals representing 0, 1, ..., (M-1)th gradation orders corresponding to the block A, there are shown printing lines (1/2 lines) of corresponding gradations. To the right of numerals indicating respective gradations, that is, numerals representing 0, 1, ..., (M-1)th gradation orders corresponding to the block B, there are shown printing lines (1/2 lines) of corresponding gradations with hatches. Although the 1/2 printing lines of the blocks A and B are parallelly represented in correspondence with the respective gradations for simplicity, in actual practice, the printing is carried out such that the printing lines are overlapped with one another. Accordingly, the 1/2 printing line from the oth order to the (M-1)th order gradations corresponding to the block A and the 1/2 printing line from the oth order to the (M-1)th order gradations corresponding to the block B are mixed to print one line.

More specifically, the heating resistance elements R1 to Rn of the block A are driven (M-1) times by making the drive strobe signal STBDR1 logic [L] level to print one half portion of one line from the lst order to the (M-1)th order gradations. Then, the heating resistance elements An + 1 to RN of the block B are driven (M-1) times by making the drive strobe signal STBDR2 logic [L] level to print the other half portion of one line from the lst order to the (M-1)th order gradations, thus to print one line.

When video image data or the like is printed on a printing sheet by the above thermal printing apparatus, the heating resistance elements forming the thermal printing head are divided to provide two blocks alternately to perform the printing at every oth order to (M-1)th order gradation, so that a voltage drop across a common resistor r between the heating resistance elements R1 to RN and the terminal 7 applied with the positive DC voltage (that is, a resistor of a thin film lead wire on the common substrate when the heating resistance elements are formed on the common substrate as a thin film) is increased, whereby the power consumption is increased considerably. Moreover, there is the substantial possibility that undesirable lines will occur in the printed image on a printing sheet between the blocks, because the heat accumulating and heat radiating characteristics of the heating resistance elements are different.

According to the present invention there is provided a thermal printing apparatus comprising:
a printing head having a plurality of heating devices for printing an image; and
driving means for driving said heating devices so as to gradate said image;
wherein said heating devices are grouped into a plurality of blocks, and said driving means drives said printing head sequentially at said each block in dependence on each gradational level.

According to the present invention there is also provided a method of thermal printing using an apparatus comprising a printing head having a plurality of heating devices for printing an image, and driving means for driving said heating devices so as to gradate said image, comprising:
grouping said heating devices into a plurality of blocks; and driving said printing head sequentially at each block in dependence on the required printing gradation level.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Figure 1 is a block diagram of previously proposed thermal printing apparatus;

Figures 2A to 2F are timing charts to which reference will be made in explaining the apparatus of Figure 1;

Figure 3 is a schematic diagram used to explain a printing method of the apparatus of Figure 1;

Figure 4 is a block diagram of an embodiment of thermal printing apparatus according to the present invention;

Figures 5A to 5E are timing charts to which reference will be made in explaining the apparatus of Figure 4; and

Figure 6 is a schematic diagram used to explain a printing method of the apparatus of Figure 4.

Throughout Figures 4 to 6, like parts corresponding to those of Figures 1 to 3 are marked

with the same references, and therefore need not be described in detail.

Figure 4 shows a thermal printing apparatus 1 forming an embodiment of the present invention. The system controller in is formed of a microcomputer or the like, and serial printing data DATA (see Figure 58) of each line are generated from the system controller in and are then fed to the H shift register stages 51 to 5n and 5n + 1 to 5N (N = 2, 3, 4, ...), in which the data DATA are shifted in response to the clock pulse signal CLK (Figure 5A) from the system controller in. Data or contents accumulated in the registers 51 to 5n and 5n + 1 to 5N of the respective stages of the shift register 5 are respectively supplied to the H latch circuits 6 (61 to 6n and 6n + 1 to 6N), in which they are latched in response to the latch strobe pulse signal STBLA from the system controller in. The pulse intervals of the latch strobe pulse STBLA are 2T0, 2T1 ... 2TM-1 are shown in Figure SC. Outputs of the H latch circuits 6 are respectively supplied to the output circuits DRV1 to DRVn and DRVn 1 to DRVN. The drive strobe signals STBDR1 and STBDR2 (Figures SD and SE) from the system controller in are supplied through the inverters IV1 and IV2 to the output circuits DRV1 to DRVN, respectively.

The operation will be described with reference to timing charts forming Figures 5A to 5E.

The serial printing data DATA from the system controller in are accumulated in all register stages of the shift register 5 in response to H clock pulses CLK, and are then latched in the latch circuits 6 in response to the latch strobe pulse STBLA during the periods 2T0, 2T1, ..., 2TM-1 of duration longer than $2N\tau$, where τ represents the cycle of the clock pulse signal CLK.

When data DATA of logic [L] level in the printing data DATA latched in the N latch circuits 6 are supplied to the output circuits (AND circuits) DRV1 to DRVN, if the drive strobe signal STBDR1 is at logic [L] level, outputs of logic [H] level are generated from the output circuits DRV1 to DRVn, whereby the transistors TR1 to TRn supplied with the outputs are turned ON to energise the heating resistance elements R1 to Rn, that is, heating head elements during the heating-process times t1 to tM - 1 (Figure 5A), whereby one 1/2 line portion of one gradation is printed on the printing sheet.

On the other hand, if the drive strobe signal STBDR2 is at logic [L] level, outputs of logic [N] level are generated from the output circuits DRVn + 1 to DRVN, whereby the transistors TRn + 1 to TRN supplied with the outputs are turned ON to energise the heating resistance elements Rn + 1 to RN, that is, heating head elements during heating-process t1 to tM - 1 (Figure 5A), whereby the other 1/2 line portion of one gradation is printed on the printing sheet. In a like manner, the printing is carried out up to the (M-1)th order gradation, completing the printing of one line portion.

Figure 6 shows such a printing method. The arrangement of Figure 6 is similar to that of Figure 3 and therefore need not be described. In this case, one 1/2 printing line and the other 1/2 printing line are alternately printed in the sequential order of the oth order gradation of block A, 0th order gradation of block B; the 1st order gradation of block A, the 1st order gradation of block B; ...; the (M-1)th order gradation of block A and the (M-1)th order gradation of block B, thereby to form a printed image of one printing line on the printing sheet.

Thus, in a thermal printing apparatus, a plurality of heating elements or devices forming a thermal printing head are repetitively driven in response to the number of gradations, the plurality of heating devices are divided to provide a plurality of blocks, and the plurality of heating devices are sequentially driven at every block in response to respective gradations. Thus, the apparatus consumes a small power, and can eliminate the undesirable line corresponding to the border between the blocks resulting from a difference of heat accumulation and heat radiation characteristics of heating devices.

Claims

1. A thermal printing apparatus (1) comprising:
a printing head (2) having a plurality of heating devices (R) for printing an image; and
driving means (4, 5, 6) for driving said heating devices (R) so as to gradate said image;
wherein said heating devices (R) are grouped into a plurality of blocks, and said driving means (4, 5, 6) drives said printing head (2) sequentially at said each block in dependence on each gradational level.

2. Apparatus (1) according to claim 1 wherein said each heating device (R) comprises a resistance element (R).

3. Apparatus (1) according to claim 1 or claim 2 wherein said driving means (4, 5, 6) comprises a shift register (5) and a latch circuit (6).

4. Apparatus (1) according to claim 3 wherein said shift register (5) is supplied with serial data of said image, and said latch circuit (6) is supplied with a latch strobe pulse for deriving gradational information.

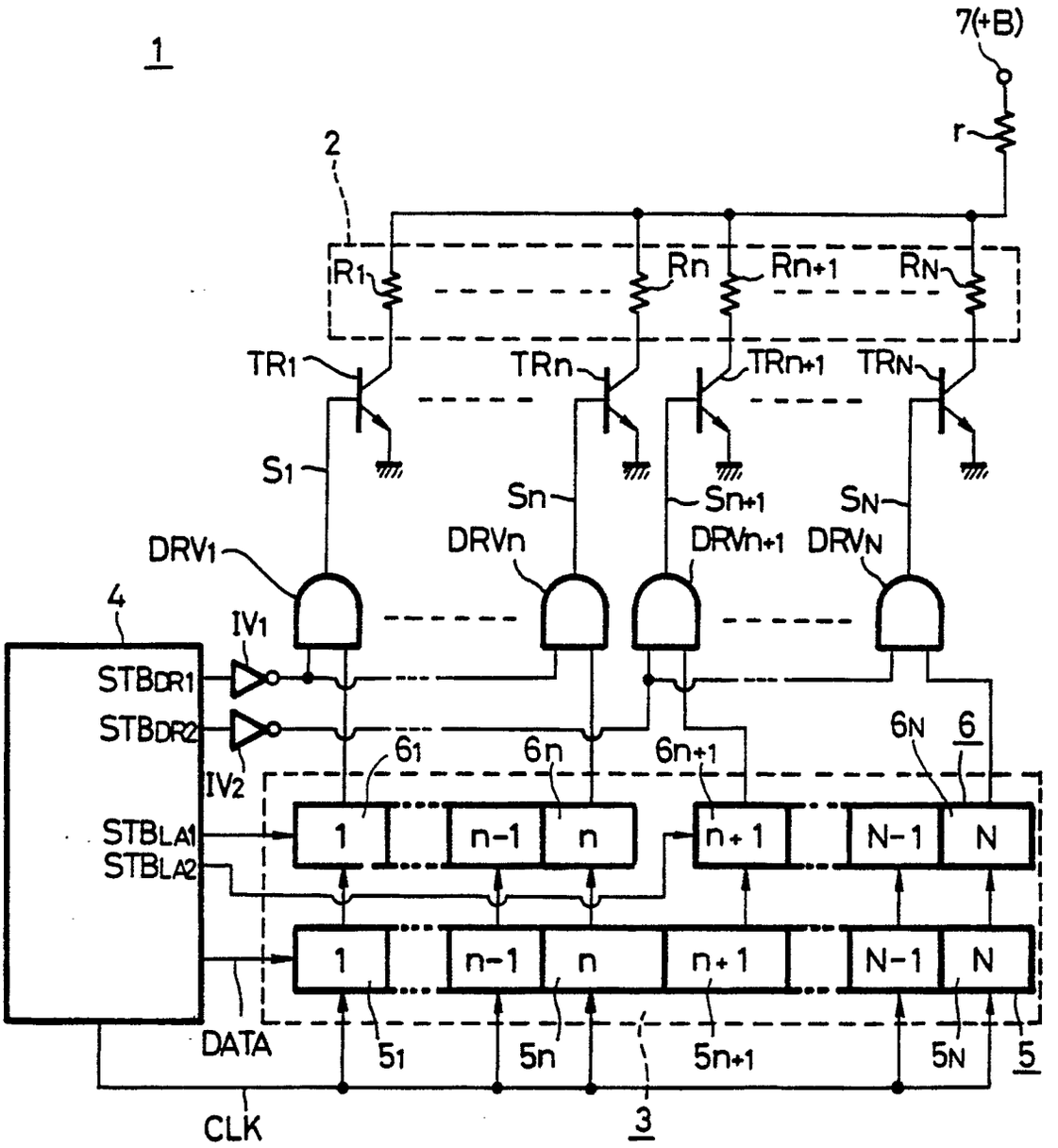
5. Apparatus (1) according to claim in wherein said each block is driven in sequence by a driving strobe signal supplied from a system controller (4).

6. A method of thermal printing using an apparatus (1) comprising a printing head (2) having a plurality

of heating devices (R) for printing an image, and driving means (4, 5, 6) for driving said heating devices (R) so as to gradate said image, comprising:

grouping said heating devices (R) into a plurality of blocks; and driving said printing head (2) sequentially at each block in dependence on the required printing gradation level.

FIG. 1


1
7(+B)
r
2
R1
Rn
Rn+1
RN
TR1
TRn
TRn+1
TRN
S1
Sn
Sn+1
SN
DRV1
DRVn
DRVn+1
DRVN
4
IV1
STBDR1
STBDR2
IV2
STBLA1
STBLA2
DATA
CLK
61
6n
6n+1
6N
6
1
n-1
n
n+1
N-1
N
51
5n
5n+1
5N
5
3

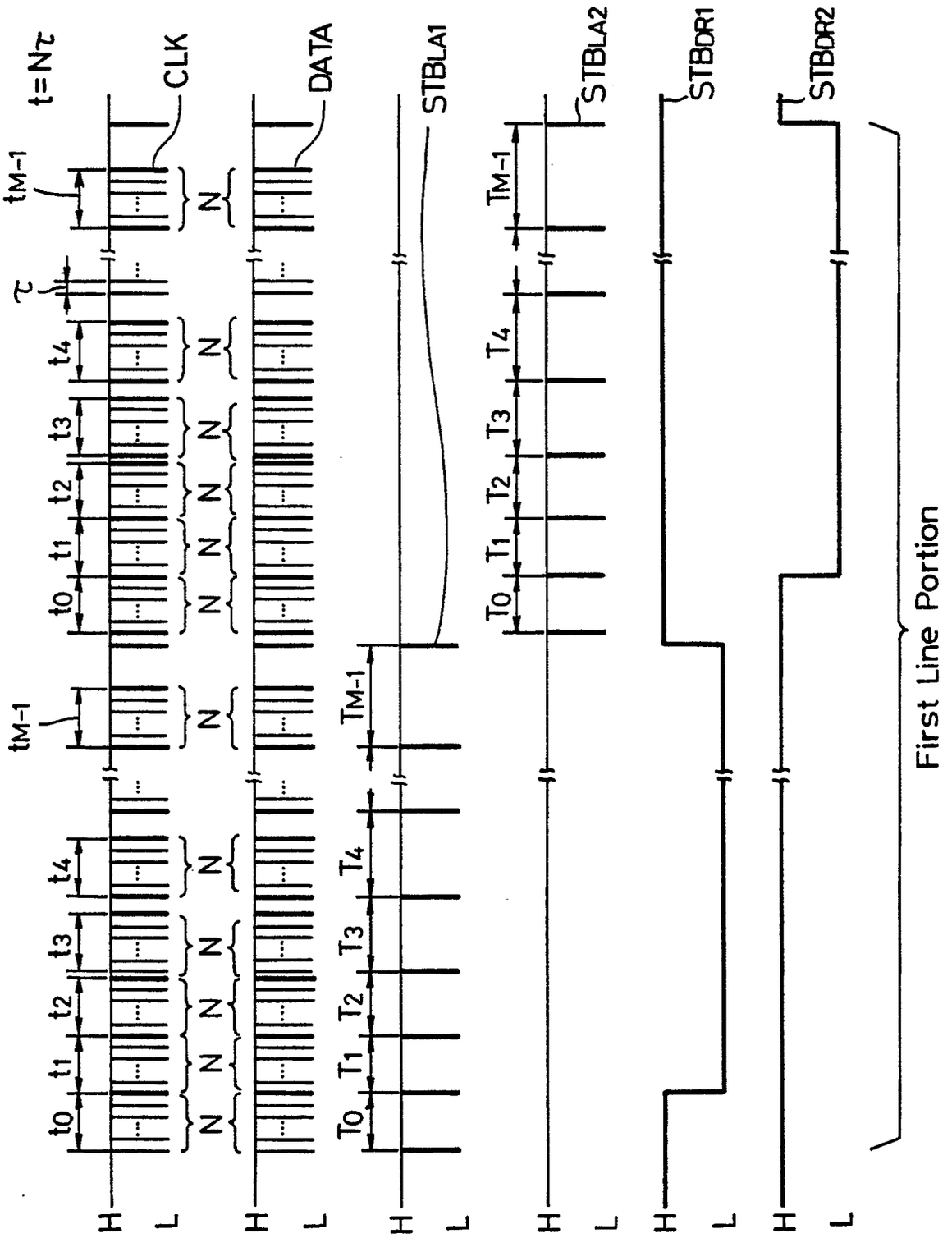


FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

FIG. 2E

FIG. 2F

FIG. 3

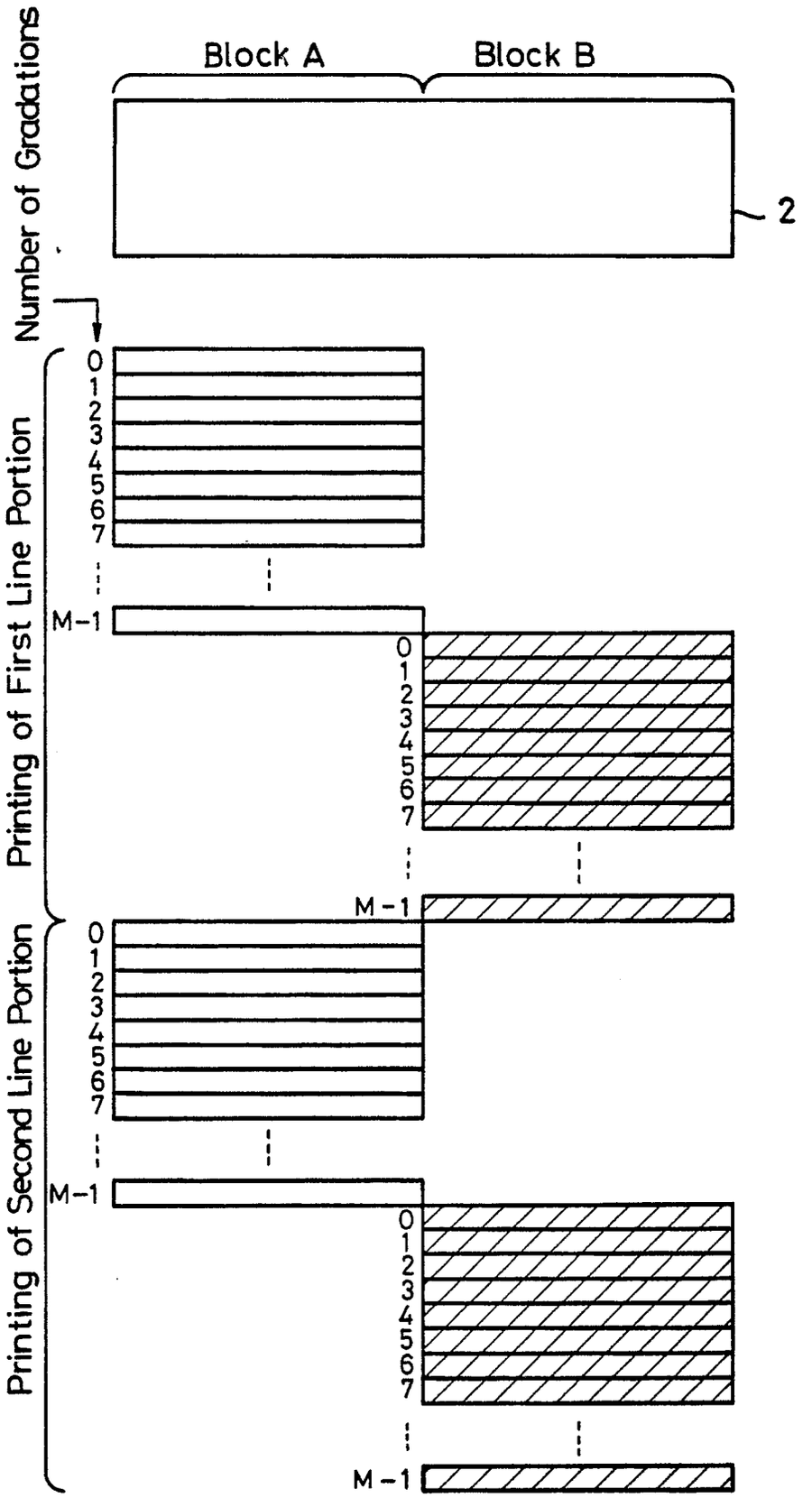
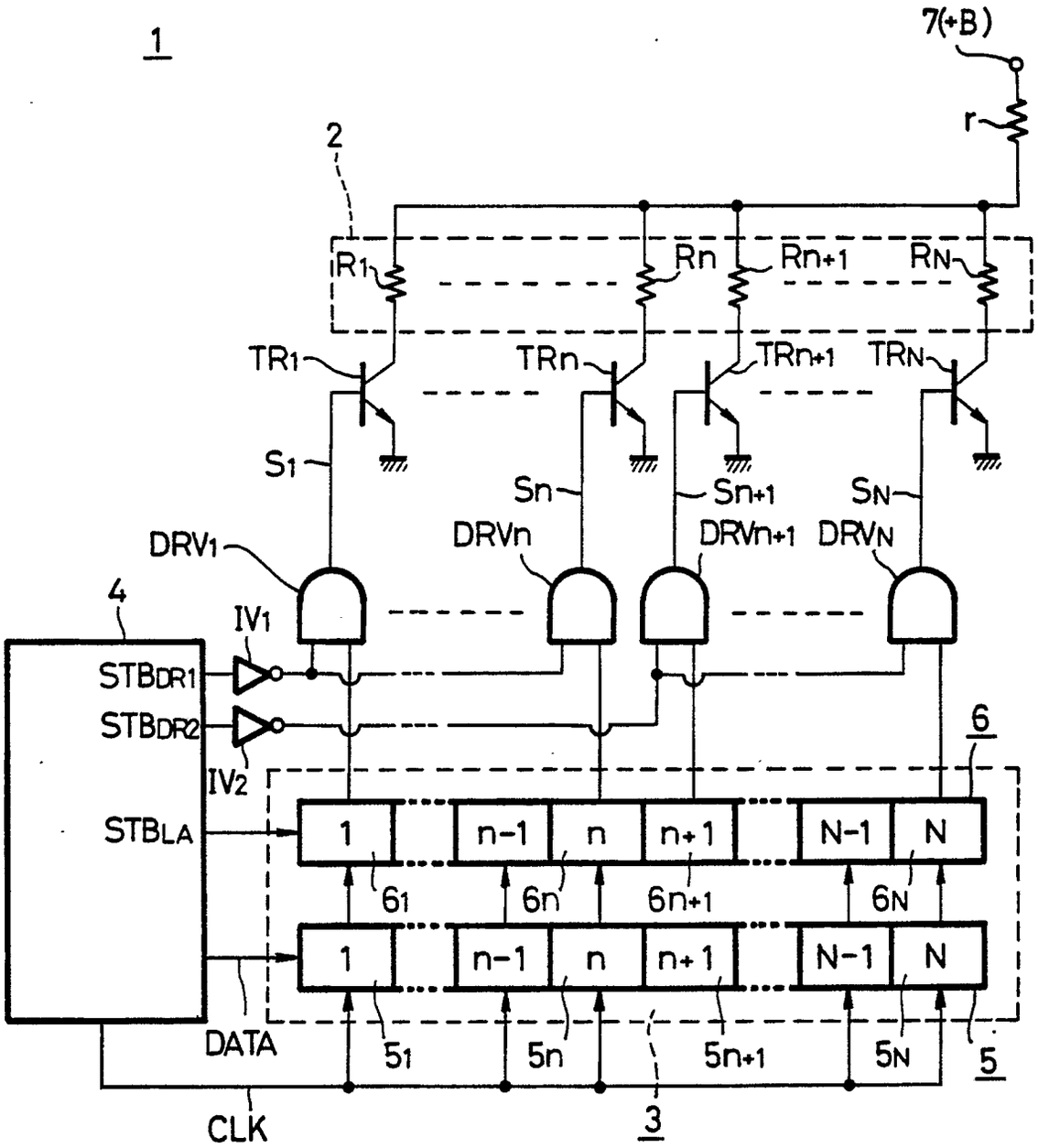

Block A
Block B
2
Number of Gradations
Printing of First Line Portion
Printing of Second Line Portion
0
1
2
3
4
5
6
7
M-1

FIG. 4


1
7(+B)
r
2
R1
Rn
Rn+1
RN
TR1
TRn
TRn+1
TRN
S1
Sn
Sn+1
SN
DRV1
DRVn
DRVn+1
DRVN
4
IV1
STBDR1
STBDR2
IV2
STBLA
6
1
n-1
n
n+1
N-1
N
61
6n
6n+1
6N
DATA
51
5n
5n+1
5N
5
CLK
3

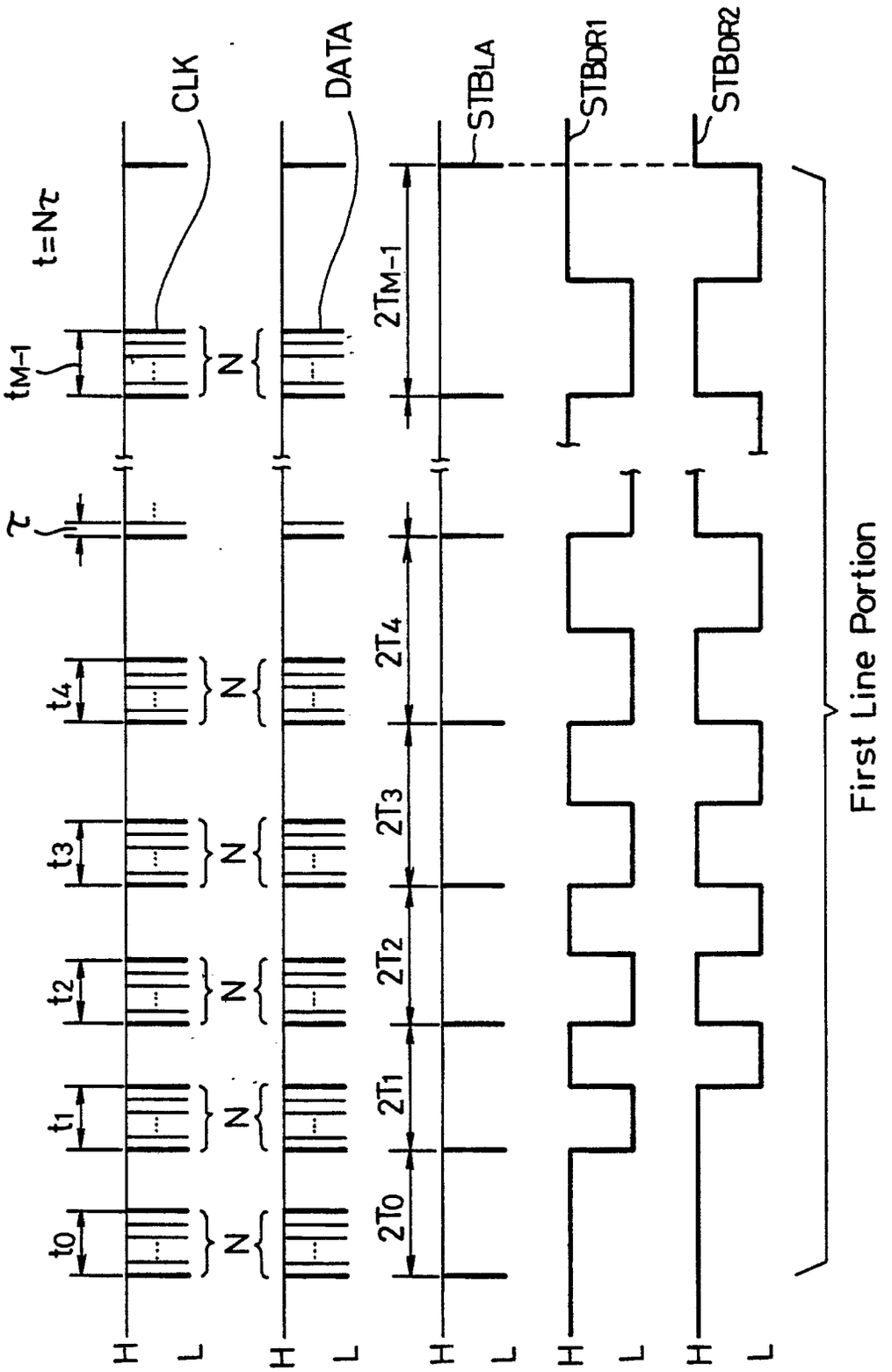


FIG. 5A

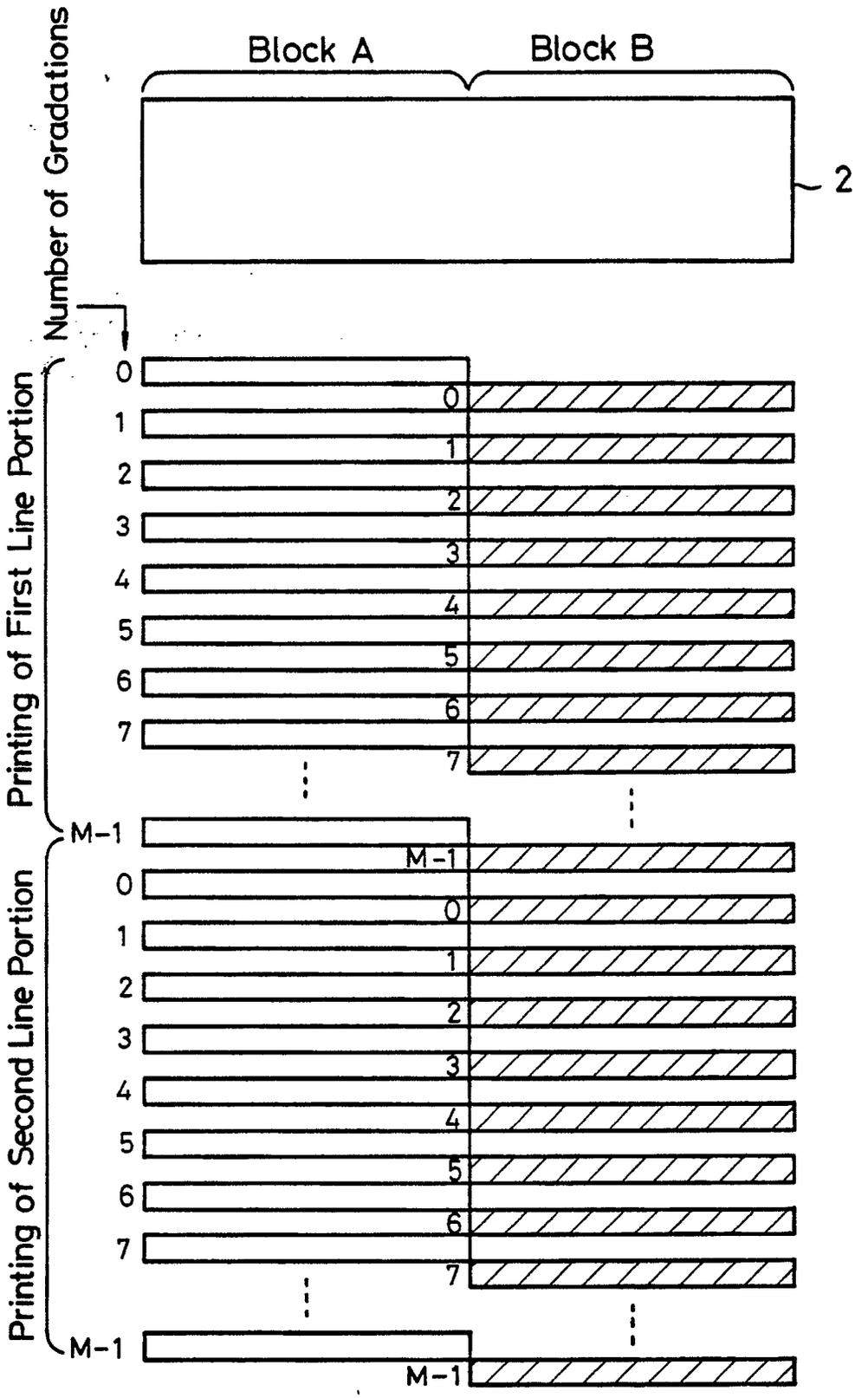
FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

FIG. 6


Block A
Block B
2
Number of Gradations
Printing of First Line Portion
Printing of Second Line Portion
0
1
2
3
4
5
6
7
M-1