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(54) **Dynamic random access memory cells and methods for fabrication.**

(57) The described embodiments of the present invention provide DRAM cells, structures and manufacturing methods. In a first embodiment, a DRAM cell with a trench capacitor having a first plate formed as a diffusion on the outside surface of a trench formed in the substrate and a second plate having a conductive region formed inside the trench is fabricated. The transfer transistor is formed using a field plate isolation structure which includes a self-aligned moat area for the transfer transistor. The moat area slightly overlap the capacitor area and allows for increased misalignment tolerance thus foregoing the requirement for misalignment tolerances but into the layout of the DRAM cell. The field plate itself is etched so that it has sloped sidewalls to avoid the formation of conductive filaments from subsequent conductive layers formed on the integrated circuit. The use of a self-aligned bitline con-

tact between two memory cells allows for the elimination of alignment tolerances between the bitline contact and the gates of the transfer transistors of the memory cells.

In another embodiment of the present invention, a planar capacitor is used with a field plate isolation scheme including a transfer transistor moat region self-aligned to the field plate. This structure allows the elimination of alignment tolerances between the capacitor and the transistor thus reducing the space necessary between the transistor and the capacitor. In addition, self-aligned techniques between the bitline and the drain of two adjacent transfer transistors allows for the elimination of many alignment tolerances between the bitline contact and the transfer transistors.

In another embodiment of the present invention, a memory cell using two conductive plates formed

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inside a trench as the storage capacitor is fabricated. A field plate isolation scheme which allows for self-alignment of the moat containing the transfer transistor is used thus allowing for self-alignment of the moat and elimination of alignment tolerances between the moat region and the source drain diffusions. In addition, sloped sidewalls on the field plate are used to avoid the fabrication of conductive filaments formed when depositing conductive layers subsequent to the field plate. A self-alignment technique between the transfer transistor and the capacitor is used in order to eliminate many alignment tolerances between the transfer transistor and the storage capacitor. A self-aligned bitline contact technique is used between two adjacent transfer transistors, thus allowing the elimination of many alignment tolerances between the bitline contact and the transfer transistors.

In addition, a sidewall insulator technique using two different materials, which may be selectively etched between one another, is used to provide a less destructive fabrication technique for forming sidewall insulating layers and allowing the use of gate insulator layer to protect the surface of the substrate during the formation of the sidewall insulating layers.

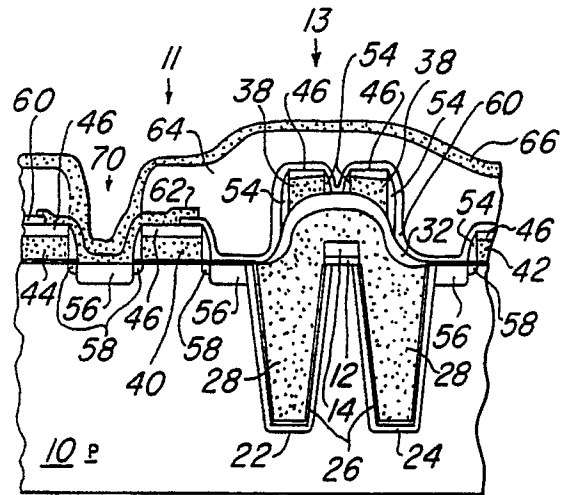


Fig. 1

## DYNAMIC RANDOM ACCESS MEMORY CELLS AND METHODS FOR FABRICATION

### FIELD OF THE INVENTION

The present invention relates to the field of integrated circuit design and fabrication. More specifically, the present invention relates to the field of dynamic random access memory arrays, cells and other structures and the methods for fabricating those structures.

### BACKGROUND OF THE INVENTION

The quest to develop smaller and smaller dynamic random access memory (DRAM) cells and related structures is a well-known goal. In integrated circuit manufacturing, certain costs are relatively fixed no matter what integrated circuit is fabricated. Thus, the greater density of memory on a single integrated circuit provides greater economy on a per bit basis by spreading these fixed costs across more memory capacity. In addition, greater memory storage capacity allows greater memory capacity of the end user products, such as computers, in a smaller package. Therefore, the value to the customer is increased. Because 50% or more of the area of a DRAM is used for memory cells themselves, reduction of the memory cell size allows for far greater numbers of those memory cells to be placed on the DRAM.

Several techniques have been developed to try to reduce the size of memory cells. For example, the fundamental dynamic random access memory cell has been reduced to a minimum of components, i.e. a transistor and a capacitor connected to the source of the transistor. The transistor allows access to the charge stored on the capacitor and the stored charge represents data. The first step in reducing the size of DRAM cells was the effective integration of the transfer transistor and the capacitor. An example of this is found in Kuo, "Random Access Memory Cell with Different Capacitor and Transistor Oxide Thickness", U.S. Patent No. 4,240,092, issued December 16, 1980 and assigned to the assignee of this application. Kuo is an example of a "Hy-C" cell. As the density of DRAMs increased, limitations of the Hy-C cell became apparent. In order to provide accurate data storage and retrieval, the capacitance of the storage capacitor must be as large as possible. However, the capacitance of the storage capacitor is directly proportional to the area between the plates of the capacitor. In a planar capacitor cell, like the Hy-C cell, this creates a fundamental tradeoff between cell size and cell capacitance.

In order to minimize the surface area occupied by the memory cell while maintaining adequate storage capacitor capacitance, vertical capacitor structures were developed. An example of such a structure is found in Sunami, "Cell Structures for Featured DRAMs", International Electron Devices Meeting Technical Digest (1985), Paper 29.1, pages 694-697. In some cases, the capacitor is formed on a trench etched into the surface of the substrate. An example of this can be found in Ishiuchi, et al., "Submicron CMOS Technologies for 4Megabit Dynamic RAM", International Electron Devices Meeting Technical Digest (1985), Paper 29.4, pages 706-709. In other cases, a stacked or multiple plate concept providing a vertically stacked capacitor was investigated. An example of this can be found in Sunami, et al., supra.

The difficulties of forming the storage capacitor in a trench have introduced a great deal of complexity into the fabrication of the DRAM cells. For example, see Baglee, et al., U.S. Patent No. 4,721,987, "Trench Capacitor Process for High Density Dynamic RAM", issued January 26, 1988 and assigned to the assignee of this application. Although the storage capacitor itself has been made smaller, the additional difficulties in connecting the transfer transistor to the capacitor have introduced requirements for spacing tolerances and increased complexity in leakage components. These have all necessitated complex processing steps and additional area occupied to fabricate the DRAM cells.

### SUMMARY OF THE INVENTION

The described embodiments of the present invention provide DRAM cells, structures and manufacturing methods. In a first embodiment, a DRAM cell with a trench capacitor having a first plate formed as a diffusion on the outside surface of a trench formed in the substrate and a second plate having a conductive region formed inside the trench is fabricated. The transfer transistor is formed using a field plate isolation structure which includes a self-aligned moat area for the transfer transistor. The moat area slightly overlaps the capacitor area and allows for increased misalignment tolerance thus foregoing the requirement for misalignment tolerances built into the layout of the DRAM cell. The field plate itself is etched so that it has sloped sidewalls to avoid the formation of conductive filaments from subsequent conductive layers formed on the integrated circuit. The use of a self-aligned bitline contact between two memory

cells allows for the elimination of alignment tolerances between the bitline contact and the gates of the transfer transistors of the memory cells.

In another embodiment of the present invention, a planar capacitor is used with a field plate isolation scheme including a transfer transistor moat region self-aligned to the field plate. This structure allows the elimination of alignment tolerances between the capacitor and the transistor thus reducing the space necessary between the transistor and the capacitor. In addition, self-aligned techniques between the bitline and the drain of two adjacent transfer transistors allows for the elimination of many alignment tolerances between the bitline contact and the transfer transistors.

In another embodiment of the present invention, a memory cell using two conductive plates formed inside a trench as the storage capacitor is fabricated. A field plate isolation scheme which allows for self-alignment of the moat containing the transfer transistor is used thus allowing for self-alignment of the moat and elimination of alignment tolerances between the moat region and the source drain diffusions. In addition, sloped sidewalls on the field plate are used to avoid the fabrication of conductive filaments formed when depositing conductive layers subsequent to the field plate. A self-alignment technique between the transfer transistor and the capacitor is used in order to eliminate many alignment tolerances between the transfer transistor and the storage capacitor. A self-aligned bitline contact technique is used between two adjacent transfer transistors, thus allowing the elimination of many alignment tolerances between the bitline contact and the transfer transistors.

In addition, a sidewall insulator technique using two different materials, which may be selectively etched between one another, is used to provide a less destructive fabrication technique for forming sidewall insulating layers and allowing the use of gate insulator layer to protect the surface of the substrate during the formation of the sidewall insulating layers.

## DESCRIPTION OF THE DRAWINGS

The present invention is best understood with regard to the following described embodiments read in conjunction with the drawings provided herewith wherein:

Figure 1 is a side view schematic diagram of a dynamic random access memory cell which is one embodiment of the present invention;

Figure 2 is an electrical schematic diagram showing the electrical operation of the DRAM cell shown in Figure 1;

Figures 3A through 3M are schematic diagrams

showing the processing steps necessary to fabricate the DRAM cell shown in Figure 1, where all but Figure 3I are side view schematic diagrams and Figure 3I is a plan view schematic diagram;

Figure 4 is a schematic plan view diagram of a memory array including the DRAM cell described with regard to Figure 1;

Figure 5 is a side view schematic diagram of a DRAM cell with a planar storage capacitor which is one embodiment of the present invention;

Figure 6 is an electrical schematic diagram showing the electrical characteristics of the DRAM cell shown in Figure 5;

Figure 7 is a plan view diagram showing the layout of the cell shown in Figure 5;

Figure 8 is a side view schematic diagram showing another embodiment of the present invention;

Figure 9 is an electrical schematic diagram showing the electrical operation of the embodiment shown in Figure 8;

Figures 10A through 10Q are schematic diagrams showing processing steps for fabricating the embodiment shown in Figure 8 where all but Figure 10O are side view schematic diagrams and Figure 10O is a plan view schematic diagram; and

Figure 11 is a plan view diagram of an array of memory cells such as the embodiment shown in Figure 8.

## DETAILED DESCRIPTION

Figure 1 is a side view schematic diagram showing one embodiment of the present invention which is DRAM cell. Figure 2 is an electrical schematic diagram showing the electrical operation of components of the embodiment shown in Figure 1, with correspondingly numbered components in Figure 2 corresponding to those components in Figure 1. Figures 3A through 3M are schematic diagrams showing the processing steps for fabricating the embodiment shown in Figure 1. Figure 4 is a memory array including the memory cell shown in Figure 1. Figure 5 is a side view schematic diagram of another embodiment of the present invention using simplified manufacturing steps as explained with regard to Figures 3A through 3M but including a planar capacitor. Figure 6 is an electrical schematic diagram showing the electrical operation of the embodiment shown in Figure 5. Figure 7 is a plan view diagram showing the layout of components of the embodiment shown in Figure 5. Figure 8 is a side view schematic diagram of another embodiment of the present invention including a stacked capacitor comprising two plates

formed in a trench. Figure 9 is an electrical schematic diagram showing the operation of the embodiment of Figure 8. Figures 10A through 10Q are schematic diagrams showing the processing steps for fabricating the embodiment shown in Figure 8. Figure 11 is a plan view diagram showing the layout of a memory array including the embodiment of Figure 8.

Figure 1 is a side view schematic diagram of one embodiment of the present invention. The memory cell of Figure 1 consists of a transfer transistor 11 and a storage capacitor 13. When data is to be stored on the memory cell, the data is placed on bitline 66 and a high voltage signal (approximately 3.3 volts) is placed on gate 40. Thus, the voltage placed on bitline 66 is passed through via source 56 to storage node 22. Capacitor 13 is comprised of storage diffusion 22 in capacitive coupling with field plate 28. Field plate 28 is tied to a reference potential and thus a charge representing the voltage applied by bitline 66 is stored on storage diffusion 22. To store the data on storage diffusion 22, the positive voltage is removed from gate 40 thus stopping continuity between source/drain regions 56. Gate 40 is part of a word line extending perpendicular to the page of Figure 1. Gate 44 controls access to a storage capacitor off to the left hand side of the page. Wordlines 36 and 38 pass over field plate 28 to provide control for memory cells extending perpendicularly into the page and out from the page. Partial wordline 42 controls access to the capacitor formed by field plate 28 and storage diffusion 24.

Figure 2 is an electrical schematic diagram showing the electrical operation of transfer transistor 11 in capacitor 13 of Figure 1. The reference numerals of Figure 2 correspond to the reference numerals of Figure 1 and indicate the electrical functions of the reference components.

Figures 3A through 3M are schematic diagrams showing the processing steps for forming the embodiment shown in Figure 1. P substrate 10 is a crystalline silicon substrate doped to a P-type conductivity of approximately 0.9 ohm-centimeters. P substrate 10 may be a complete substrate of 0.9 per ohm centimeter material or a 0.9 ohm centimeter epitaxial layer may be formed on the surface of a substrate having a differing doping type or concentration. Silicon dioxide layer 12 is formed by thermal oxidation of P substrate 10 to a thickness of approximately 350 Angstroms by thermal oxidation in an oxygen ambient in approximately 950°C for approximately 50 minutes. Silicon nitride layer 14 is formed by low pressure chemical vapor deposition to a thickness of approximately 1000 Angstroms. A hardmask 16 is formed to a thickness of approximately 5000 Angstroms by chemical vapor deposition of phospho-

rous doped silicon dioxide. A layer of photoresist (not shown) is then patterned and silicon dioxide layer 12, silicon nitride layer 14 and silicon dioxide layer 16 are etched to provide openings 18 and 20 as shown in Figure 3A.

Using silicon dioxide layer 16 as a mask, trenches 18 and 20 are etched into the surface of substrate 10 as shown in Figure 3B. A suitable etching method can be found in Douglas, "Trench Etch Process for a Single-Wafer RIE Dry Etch Reactor", U.S. Patent No. 4,784,720, issued November 15, 1988 and assigned to the assignee of this application. The walls of trenches 18 and 20 are then doped using arsenic to a doping concentration of approximately  $3 \times 10^{19}$  dopant atoms per centimeter<sup>3</sup> using one of many processes. For example, an angled ion implantation with arsenic ions at an angle of 8° while rotating substrate 10 may be performed. The ions are implanted at an energy of approximately 100 kiloelectron volts in a density of approximately  $5 \times 10^{15}$  ions per centimeter<sup>2</sup>. Other suitable doping techniques such as deposition of doped materials and diffusion of the dopants into substrate 10 may suitably be used.

Silicon dioxide layer 16 is then removed using wet etching in a 10% buffered hydrofluoric acid solution for approximately 40 seconds. The resulting structure is shown in Figure 3C.

A suitable capacitor dielectric 26 such as thermally grown silicon dioxide is then formed to a thickness of approximately 60 Angstroms using thermal oxidation in an oxygen ambient for approximately 40 minutes at a temperature of approximately 850°C. Other suitable dielectrics include silicon dioxide, silicon nitride, silicon dioxide stacks, oxidized silicon nitride and other deposited materials such as tantalum oxide. A layer of polycrystalline silicon 28 is then deposited by low pressure chemical vapor deposition of silane to a thickness of approximately 5000 Angstroms. The resulting structure is shown in Figure 3E. Polycrystalline silicon layer 28 is doped by in situ doping to provide a conductivity of approximately 0.005 ohm-centimeters. Polycrystalline silicon layer 28 may then be thinned on the surface to a thickness of approximately 2,000 Angstroms using wet etching or plasma etching in a carbon tetrafluoride plasma. This reduces the topology of polycrystalline silicon layer 28. Polycrystalline silicon layer 28 provides a field plate which covers all areas of the array excepting where the transfer transistors are to be formed. Field plate 28 provides an implantation mask for formation of those transistors thus providing a self-aligned system for aligning field plate 28 and the transfer transistors. This provides a greater packing density because no alignment tolerance is required between the transfer transistors and the

field isolation device. A layer of photoresist 30 is formed on the surface of field plate 28 and field plate 28 is etched using a combination isotropic and anisotropic process. An anisotropic etch is used such as hydrofluoric/bromic acid for approximately 1 minute. An isotropic etch is then performed to provide sloped sidewalls to leave the structure as shown in Figure 3F.

Photoresist layer 30 is then removed using standard photoresist removal processes such as wet removal or ashing. Silicon nitride layer 14 and silicon dioxide layer 12 are then removed by etching in a plasma of  $C_2F_6/CHF_3$ . The structure of Figure 3F with photoresist layer 30 thus removed is then subjected to an oxidation step in a oxygen/steam ambient for approximately 30 minutes to form silicon dioxide layers 27 and 32 as shown in Figure 3G. Because of the higher rate of oxidation of polycrystalline silicon layer 28, silicon dioxide layer 32 is much thicker than silicon dioxide layer 27. The use of an overall oxidation step provides a contiguous isolation layer from the moat surface of substrate 10 to field plate 28. Thus complete sealing of field plate 28 from subsequent conductive layers is achieved. In another embodiment, the surface of the moat is protected by silicon nitride layer 14 and silicon dioxide layer 12 while polycrystalline silicon layer 28 is oxidized. Silicon dioxide layer 27 is then formed in a separate oxidation step. A polycrystalline silicon layer 34 and a silicon dioxide layer 46 are then deposited on the surface of the structure of Figure 3G as shown in Figure 3G. Polycrystalline silicon layer is approximately 2500 Angstroms thick. Silicon dioxide layer 46 is approximately 1,000 Angstroms thick. Polycrystalline silicon layer 34 has a conductivity of approximately 0.005 ohms-centimeter.

Polycrystalline silicon layer 34 and silicon dioxide layer 46 are then patterned and etched to provide wordlines 36, 38, 40, 42 and 44 as shown in Figure 3H.

Figure 3I is a plan view of a portion of the structure of Figure 3H. As can be seen from Figure 3I, exposed moat regions of substrate 10 (covered by silicon dioxide layer 27) are left where field plate 28 and wordlines 40 and 44 do not cover substrate 10. Field plate 28 and the wordlines provide an implantation mask for the formation of source drains which provides an automatic alignment between the gates provided by the wordlines 40 and 44, and field plate 28. Because of this automatic alignment, no additional alignment tolerance is required to form the source/drains of the transfer transistor 11 (Fig. 1) and an additional masking step its potential for yield loss is avoided. The capacitor structures in Figure 3I are indicated by trenches 18 and 20 although, of course, the capacitors are actually the more complex struc-

tures shown in Figure 3H.

The structure of Figure 3H is subjected to an ion implantation of phosphorous ions having an energy of approximately 60 kiloelectron volts and a density of approximately  $4 \times 10^{13}$  ions per centimeter<sup>2</sup> to form lightly doped source/drain regions 50 as shown in Figure 3J. A layer of silicon nitride 52 is then deposited by low pressure chemical vapor deposition to a thickness of approximately 1000 Angstroms on the structure of Figure 3J as shown in Figure 3K. Silicon nitride layer 52 is then etched anisotropically using a sulphur hexafluoride etchant in reactive ion etching to provide sidewall nitride layers 54 as shown in Figure 3L. Because the reactive ion etching step which formed sidewall nitride layers 54 is selective to silicon dioxide, silicon dioxide layers 46 and 26 protect wordlines 36, 38, 40, 42 and 44 and substrate 10, respectively. Prevention of this damage caused by ion bombardment protects the conductivity of the word lines and the source/drain regions formed in substrate 10.

The structure of Figure 3L is subjected to ion implantation of arsenic ions having an energy of approximately 100 kiloelectron volts and a density of approximately  $3 \times 10^{15}$  ions per centimeter<sup>2</sup> to form source/drain regions 56 as shown in Figure 3L. The remaining portions of lightly doped source/drain regions 50 (Figure 3K) provide lightly doped drain regions 58 as shown in Figure 3L. Lightly doped drain regions 58 reduce the field density at the edges of transfer transistor 11 thus reducing the incidence of hot electrons in the operation of transistor 11 and increasing the lifetime of transistor 11. In another embodiment, source/drain regions 50 may be omitted. Because of the close spacing of DRAM cells, the high conductivity of source/drain 50 is not critical, therefore, they may be omitted.

Silicon dioxide layer 60 is formed by chemical vapor deposition to a thickness of approximately 200 Angstroms. A photoresist pattern (not shown) is then formed on the surface of the structure of Figure 3M to provide an opening for bitline contact to source/drain region 56 between gates 40 and 44. Silicon dioxide layer 60 is then subjected to reactive ion etching using an etchant selective to silicon dioxide such as carbon tetrafluoride to provide opening 70. This opening is used for the deposition of thin polycrystalline silicon layer 62 which has a thickness of approximately 300 Angstroms and a conductivity of approximately 0.005 ohm-centimeters. Polycrystalline silicon layer 62 is then patterned using common lithographic techniques to provide the structures shown in Figure 3M. Polycrystalline silicon layer 62 provides a "landing pad" for deposition of bitline 66. Because polycrystalline silicon layer 62 extends up onto silicon dioxide

layer 60, a much larger alignment tolerance area for positioning of the contact to source/drain 56 is available.

Boron-phosphorous doped silicon dioxide layer 64 is deposited to a thickness of approximately 5,000 Angstroms on the surface of the structure of Figure 1. A photoresist pattern (not shown) is then formed to allow the formation of opening 70 as shown in Figure 1. Silicon dioxide layer 64 is then etched using an etchant such as carbon tetrafluoride which is selective to silicon dioxide to provide an opening to the top surface of polycrystalline silicon layer 62. Because polycrystalline silicon layer 62 extends up wider than the opening between wordlines 40 and 44, no alignment tolerance between wordlines 44 and 40 is necessary thus the distance between wordlines 40 and 44 may be the minimum lithography dimension allowed by the lithography system used. Bitline 66 is then deposited on the surface of silicon dioxide 64. Of course, standard via formation may be used to contact diffusion 56, but this increases the array size. Bitline 66 may be any suitable conductive material such as polycrystalline silicon, tungsten, titanium tungsten or others. In the embodiment where diffusion 56 is omitted, a highly doped contact region is formed in the contact by diffusion of dopants from polycrystalline silicon layer 62.

Figure 4 is a plan view of an array of the DRAM cells shown in Figure 1. Each of the wordlines is designated 40-1 through 40-7 and each of the bitlines is designated 60-1 through 60-4. Capacitors are labeled 13-X-Y. The X designates the bitline which is connected through the pass transistor to the capacitor. The Y designates the wordline which controls the conductivity of the transistor connected to the capacitor. Contact points 70 are designated. For example, on memory cell 68 which has capacitor 13-2-4, the signal on wordline 40-4 controls access to the capacitor and the signal on bitline 66-2 is stored on capacitor 13-2-4 when a high voltage signal is placed on wordline 40-4.

Because of the structure of capacitor 13-2-4, wordline 40-4 is not critically aligned to capacitor 13-2-4. Because the moat region is allowed to extend up onto capacitor 13-2-4 and because storage diffusion 22 provides a source/drain region if wordline 40-4 extends onto capacitor 13-2-4, no alignment tolerance is required between capacitor 13-2-4 and wordline 40-4. However, because it is desirable to have the operation of the lightly doped drain between capacitor 13-2-4 and wordline 40-4, a spacing of approximately 0.1 micron for the thickness of storage diffusion 22 and an additional thickness of 2 alignment tolerances (approximately 0.1 micron) is patterned between capacitor 13-2-4 and wordline 40-4.

Although Figure 4 shows capacitors 13-X-Y as

square openings, it has been determined that it is best to provide rounded contours for the openings for the capacitors. With rounded corners, intracapacitor high electric fields can be avoided and closer spacing between capacitors 13-X-Y may be utilized successfully. In addition, an additional implant of boron ions along with the angled ion implantation shown in Figure 3B provides an envelope of heavily doped P type region around storage diffusion 22. This provides an even greater margin of leakage prevention and allows even denser packing between capacitor 13-X-Y. Previous common knowledge had indicated that the minimum spacing between diffused storage node trench capacitors was about 1 micron. This was caused by the track-off between high substrate doping to prevent leakage and low substrate doping for high breakdown voltage level. Computer synthesis has shown that a density as close as 0.5 microns may be utilized with the field plate scheme as shown in this embodiment. The layout of Figure 4 provides a minimum spacing between capacitors of approximately 0.8 microns. Given alignment tolerances and 0.6 micron lithography techniques, a minimum spacing of 0.6 microns would then be achieved. Data indicates that this would be acceptable and a cell size of  $1.5 \times 2.6$  microns may be achieved.

Although the structure of Figure 1 uses a trench capacitor cell, the field plate structure shown in Figure 1 may successfully be utilized with the planar cell as shown in Figure 5. Field plate 128 corresponds to field plate 28 shown in Figure 1. Rather than depositing polycrystalline silicon into a trench, field plate 128 is formed on the surface of substrate 110 over storage diffusions 122 which are formed by patterned ion implantation. The remaining structures shown in Figure 5 correspond to the numerically indicated structures with the addition of 100 shown in Figure 1 and are formed using the same techniques. Thus, the self-aligned features of the bitline contact and the moat region to the field plate region are achieved using a planar capacitor.

Figure 6 is an electrical schematic diagram showing the electrical operation of the memory cell shown in Figure 5.

Figure 7 shows the plan view of selected structures of the memory cell of Figure 5 which correspond to the layout structure of Figure 3I. Thus, the self-aligned structure in manufacturing techniques are not limited to the use of trench capacitors and may be successfully used with other storage capacitor techniques and other circuit structures. For example, a stacked capacitor structure may be formed extending from the source region adjacent to capacitor 122 onto the surface of wordline 140 and field plate 128.

Figure 8 is a side view schematic diagram of

another embodiment of the present invention including a poly to poly capacitor 213. Wordline 260 controls conduction between source/drains 268 thus comprising transfer transistor 211. Source/drain 268 and contact diffusion 248 are both N-type diffusions thus comprising a conductive unit. When data is applied via bitline 272 through transfer transistor 211 to contact point 248, current passes through polycrystalline silicon plug 246 to storage plate 228. Storage plate 228 forms the capacitor between storage plate 228 and field plate 238 across dielectric 232.

Figure 9 is an electrical schematic diagram showing the electrical operation of the DRAM cell shown in Figure 8. Corresponding reference numbers in Figure 9 correspond to the components shown in Figure 8.

Figures 10A through 10Q are schematic diagrams showing the processing steps for fabricating the memory cell shown in Figure 8. Substrate 210 is a crystalline silicon substrate doped to P-type to a conductivity of approximately 0.9 ohm centimeters. Silicon dioxide layer 212 is formed on the surface of substrate 210 by thermal oxidation in an oxygen ambient at a temperature of approximately 950 °C for approximately 50 minutes to provide a silicon dioxide layer of approximately 350 Angstroms. Silicon nitride layer 214 is formed by low pressure chemical vapor deposition to a thickness of approximately 1300 Angstroms. Silicon dioxide layer 216 is silicon dioxide deposited using chemical vapor deposition to a thickness of approximately 5000 Angstroms and hardened to provide a hardmask for etching of trenches 218 and 220 were indicated in Figure 10A. A photoresist pattern (not shown) is then formed on the surface of silicon dioxide layer 216 and used to etch silicon dioxide layer 216, silicon nitride layer 214 and silicon dioxide layer 212 to provide openings 218 and 220 as shown in Figure 10A.

Trenches 218 and 220 are formed in substrate 210 using the etching techniques described in Douglas, et al., supra. A thin silicon dioxide layer is then formed on the walls of trenches 218 and 220 using thermal oxidation in a steam ambient at approximately 900 °C for approximately 10 minutes to a thickness of 250 Angstroms. A layer of silicon dioxide is then deposited in silane to a thickness of approximately 750 Angstroms on the surface of the silicon dioxide layer to provide composite silicon dioxide layer 222 as shown in Figure 10B. A layer of in situ doped polycrystalline silicon 224 is then deposited using chemical vapor deposition to a thickness of approximately 1000 Angstroms. A layer of TEOS silicon dioxide 226 is then deposited using chemical vapor deposition to a thickness of approximately 500 Angstroms. A layer of photoresist 228 is then deposited to a thickness of approxi-

mately 10,000 Angstroms to provide the structure shown in Figure 10B. Photoresist layer 228 is then exposed to light overall, without the use of a mask. The wavelength, intensity and time of exposure are chosen so that the top layer of photoresist layer 228 is exposed while the portion of photoresist layer 228 in trenches 218 and 220 is unexposed. The exposed photoresist is then removed using common developing techniques to leave the remainder of photoresist layer 228 as shown in Figure 10C.

Silicon dioxide layer 226 is then etched using  $C_2F_6/CHF_3$  plasma. Polycrystalline silicon layer 224 is then etched using  $3F_6$  plasma. The remaining portions of polycrystalline silicon layer 224 form polycrystalline silicon plate 228 and polycrystalline silicon plate 230 as shown in Figure 10D. The remainder of photoresist 229 and silicon dioxide layer 226 are then removed using wet chemical etching techniques leaving the structure of Figure 10E. A layer of silicon nitride is then deposited using low chemical vapor deposition to provide silicon nitride layer 232 as shown in Figure 10F. A layer of polycrystalline silicon is then deposited having a thickness of approximately 6000 Angstroms to completely fill trenches 218 and 220 as shown in Figure 10G. Polycrystalline silicon layer 238 will form field plate 238 after etching as described with regard to Figure 10H.

A Layer of photoresist 239 is then deposited and patterned on the surface of polycrystalline silicon layer 238 as shown in Figure 10H. Polycrystalline silicon layer 238 is then etched using a combination anisotropic and isotropic etch to provide sloped sidewalls and thus to provide the structure shown in Figure 10H. Silicon nitride layer 232, silicon dioxide layer 222 and silicon nitride layer 214 are then removed using anisotropic etching techniques such as reactive ion etching in  $C_2F_6/CHF_3$  plasma. Thus the structure of Figure 10H remains.

The structure of Figure 10H is then subjected to an isotropic silicon dioxide etch such as wet chemical etching in hydrofluoric acid to remove the top portion of silicon dioxide layer 221 and to remove a portion of the silicon dioxide layer 221 between substrate 210 and plates 228 and 230 to provide openings 240 as shown in Figure 10I. Photoresist layer 239 is then removed using common photoresist removal techniques.

A layer of polycrystalline silicon 242 is then deposited on the structure of Figure 10I to provide a thin polycrystalline silicon layer overall and to fill openings 240 as shown in Figure 10J. The structure of Figure 10J is then subjected to an isotropic etch such as carbon tetrafluoride plasma to remove the top portion of polycrystalline silicon layer 242.

A portion of polycrystalline silicon layer 242 in



openings 240 will remain to form polycrystalline silicon plugs 246 as shown in Figure 10K. Dopant atoms will diffuse from storage plates 228 and 230 to form diffusions 248. This technique for forming the contacts from diffusions 248 to plates 228 and 230 is shown in copending application Serial No. 122,604, which is assigned to the assignee of this application and which is hereby incorporated by reference. The resulting structure is then thermally oxidized to form silicon dioxide layer 244 as shown in Figure 10K. In an alternative embodiment, silicon nitride layer 214 and silicon dioxide layer 212 remain at this step and are used as an oxidation mask to protect the moat region while polycrystalline silicon layer 238 is oxidized. Silicon nitride layer 214 and silicon dioxide layer 212 are then removed, and a second thermal oxidation step is used to form the portion of silicon dioxide layer 244 on the moat. This process allows greater control of the relative thickness of the two portions of silicon dioxide layer 244.

A layer of silicon nitride (not shown) is then formed to a thickness of approximately 1000 Angstroms on the surface of the structure of Figure 10K and anisotropically etched to provide silicon nitride sidewall layers 250 as shown in Figure 10L. Silicon nitride sidewall layers 250 provide sealing of the corner of plates 232 and help prevent the formation of conductive filaments on the sides of silicon dioxide layer 244 during subsequent deposition and etching of conductive layers.

A layer of polycrystalline silicon 252 is then formed on the surface of the structure of Figure 10L to a thickness of approximately 5000 Angstroms. Polycrystalline silicon layer 252 is doped to a conductivity of approximately 0.005 ohm-centimeters by insitu doping. A layer of TEOS silicon dioxide 254 is then formed on the surface of polycrystalline silicon layer 252 to a thickness of approximately 2500 Angstroms. A layer of patterned photoresist (not shown) is then used to etch polycrystalline silicon layer 252 and silicon dioxide layer 254 to provide wordlines 256, 258, 260, 262 and 264 as shown in Figure 10N.

Figure 10O is a plan view of the resulting structure showing the moat region as substrate 210. Note that the opening extends onto the surface of the capacitors formed in trenches 218 and 220. This overlap allows for misalignments and allows for optimal spacing of the resulting transistor without the additional alignment spaces between trench 218 and wordline 260, for example. Because no alignment spacing is required between trench 218 and wordline 260, no additional diffusions are required and an absolute minimum spacing may be provide between wordline 260 and trench 218.

The structure of Figure 10N is then subjected to an ion implantation of phosphorous or arsenic

ions having an energy of approximately 60 kiloelectron volts and a density of approximately  $4 \times 10^{13}$  ions per centimeter<sup>2</sup>. This forms lightly doped source/drain regions 266 as shown in Figure 10P. A layer of silicon dioxide is then deposited to a thickness of approximately 1500 Angstroms using chemical vapor deposition and is then etched using anisotropic etching to provide silicon dioxide sidewall layers 267 as shown in Figure 10Q. The structure of Figure 10Q is then subjected to an ion implantation of arsenic ions having an energy of approximately 150 kiloelectron volts and a density of approximately  $3 \times 10^{15}$  ions per centimeter<sup>2</sup>. Alternatively, the lightly doped regions 266 may be omitted and a double implantation after the formation of sidewall oxide layers 267 may be used using an arsenic ion implantation of arsenic ions having an energy of approximately 150 kiloelectron volts and a density of approximately  $3 \times 10^{15}$  ions per centimeter<sup>2</sup> plus a phosphorous ion implantation of phosphorous ions in an energy of approximately 85 kiloelectron volts in a density of approximately  $4 \times 10^{14}$  ions per centimeter<sup>2</sup>. Because of the greater diffusivity of phosphorous atoms in silicon, lightly doped drain regions are formed surrounding source/drain regions 268 thus providing a substitute for lightly doped regions 266 as shown in Figure 10Q.

Because the moat opening overlapped the capacitor region, source/drain region 268 between wordline 260 and diffused region 248 provides a conductive connection for transistor 211 as shown in Figure 8. Even with misalignment, a transistor using doped region 248 as a source/drain will be formed thus providing a functioning pass transistor. This structure allows for misalignment and thus alignment tolerances may be omitted between wordline 216 and capacitor 213.

A layer of boron phosphorous silicon dioxide is then deposited to a thickness of approximately 2000 Angstroms. This layer remains in the undensified state and a resist pattern (not shown) is formed on the surface of silicon dioxide layer 270. Silicon dioxide layer 270 is then etched in a solution of 10% hydrofluoric acid for approximately 15 seconds. A quick reactive ion etch using carbon tetrafluoride is used to remove silicon dioxide layer 251 above source/drain diffusion 268. A layer of polycrystalline silicon 272 is then deposited to a thickness of approximately 3500 Angstroms and doped in situ to provide a conductivity of approximately 40 ohms per centimeter<sup>2</sup>. Because TEOS silicon dioxide layers 234 and sidewall silicon dioxide layers 267 are resistant to the 10% hydrofluoric acid etch, the contact of polycrystalline silicon layer 272 is aligned to wordlines 262 and 260 and is automatically self-aligned. Thus, no alignment tolerance is required for the formation of the bitline

contact 271 to source/drain diffusion 268. Because no alignment tolerances are required, a denser array may be formed.

Figure 11 is a plan view of a memory array using the memory cell of Figure 8. The layout of Figure 11 is similar to that of Figure 9 and because of the use of similar self-aligning techniques and overlap between the moat region and the capacitor region, similar layout providing optimal density is provided. Therefore, memory cell 274 as shown in Figure 11 may be formed having an area of 1.5 microns x 2.6 microns using .6 micron rules with .1 micron alignment tolerances.

Although specific embodiments of the present invention are herein described, they are not to be construed as limiting the scope of the present invention. Other embodiments will become clear to those skilled in the art in light of the teachings of this specification. For example, although the embodiments show the use of crystalline silicon, other semiconductor materials such as gallium arsenide may be used. In addition, although the manufacturing techniques used herein are described with regard to the fabrication of DRAM cells, the techniques used herein may have wide applicability in other integrated circuit structures. For example, formation of self-aligned transistors to field plate isolation systems may have wide applicability in other device structures. The present invention is only limited by the claims appended hereto.

## Claims

1. A process for fabricating an integrated circuit device comprising the steps of:  
forming selected devices in first regions of a substrate, said devices having a first edge for conductive connection to subsequently formed devices;  
forming an insulating layer overall on said substrate;  
forming a conductive layer overall on said insulating layer;  
forming moat regions through said conductive field plate by etching openings in said field plate;  
forming an insulating layer over said field plate;  
depositing and patterning a conductive layer to provide a gate overlying said moat region; and  
implanting dopant ions into said substrate using said gate and said conductive field plate as an ion implantation mask, the doped regions formed by said implanting being in conductive contact with said first edge.

2. A process as in Claim 1 wherein said moat region overlies said selected device.

3. A process as in Claim 1 wherein said selected device is a capacitor.

4. A process as in Claim 1 wherein said gate forms

a portion of an extended conductive line.

5. A process as in Claim 3 wherein said capacitor is formed in a trench in said substrate.

6. A process as in Claim 5 wherein said capacitor is formed using the steps of:

forming said trench in said substrate;

introducing dopant atoms to the surfaces of said trench to form a doped storage region;

forming an insulating layer on the surfaces of said trench; and

filling the remainder of said trench with a conductive material, said conductive material being in conductive contact with said conductive layer.

7. A process as in Claim 5 wherein said capacitor is formed using the steps of:

forming said trench in said substrate;

forming a first insulating layer on the surfaces of said trench;

forming a first conductive layer on said first insulating layer;

forming a conductive connection from a doped region formed in said substrate to said first conductive layer, said doped region serving as said first edge;

forming a second insulating layer on said first conductive layer; and

filling the remainder of said trench with a conductive material, said conductive material being in conductive contact with said conductive layer.

8. An integrated circuit device comprising:  
a conductive field plate formed on the surface of a substrate;

a moat opening formed in said field plate;

a gate formed on said substrate in said moat opening;

diffused regions formed in said substrate by introducing dopant atoms into said substrate using said gate and said field plate as a doping mask, at least one of said diffused regions being in conductive contact with selected devices in said substrate.

9. A device as in Claim 8 wherein said moat region overlies said selected device.

10. A device as in Claim 8 further comprising an insulating layer between said field plate and said substrate.

11. A device as in Claim 8 wherein said field plate comprises a polycrystalline silicon layer.

12. A device as in Claim 8 wherein a continuous insulating layer is formed by thermally oxidizing said substrate exposed by said moat opening and said field plate.

13. A device as in Claim 8 wherein said selected device is a capacitor.

14. A device as in Claim 13 wherein said capacitor is formed in a trench.

15. A device as in Claim 14 wherein said capacitor comprises:

a diffused region surrounding said trench, said dif-

fuse region being in conductive contact with one of said said diffused regions in said moat region;  
an insulating layer formed on the walls of said trench; and

conductive material filling the remainder of said trench, said conductive material being in conductive contact with said field plate.

16. A device as in Claim 14 wherein said capacitor comprises:

a first insulating layer formed on the walls of said trench; and

a first conductive layer formed on said first insulating layer, said first conductive layer being in electrical contact with one of said diffused regions in said moat;

a second insulating layer formed on said first conductive layer; and

conductive material filling the remainder of said trench, said conductive material being in conductive contact with said field plate.

17. A method for forming an integrated circuit, comprising the steps of:

providing a contact point on the surface of a substrate;

forming a first layer on either side of said contact point;

forming a protective layer on said first layers;

forming an interlevel insulating layer overall;

forming a pattern larger than said contact point on said interlevel insulating layer;

etching said interlevel insulating layer using said pattern as a mask and said protective layer as an etch stop; and

anisotropically etching said protective layer to expose said contact point.

18. A method as in Claim 17 wherein said contact point is a diffusion formed in said substrate.

19. A method as in Claim 17 wherein said contact point is a combined drain of two transistors and said first layer is patterned to form a gate of one transistor on one side of said contact point and another gate of the other transistor on the opposite side of said contact point.

20. A method for forming an array of memory cells, comprising the steps of:

forming a plurality of memory cells in a substrate, each of said memory cells being connected to a bitline and a word line;

providing a bitline contact point on the surface of a substrate for a pair of memory cells;

forming a plurality of word lines on said substrate, one of said word lines serving as a gate of a transistor of one memory cell of said pair of memory cells and an adjacent word line serving as a gate of a transistor for the other memory cell transistor of said pair of memory cells, said word lines being formed on either side of said bitline contact point;

forming a protective layer on said word lines layers;

forming an interlevel insulating layer overall;

forming a pattern larger than said bitline contact point on said interlevel insulating layer;

etching said interlevel insulating layer using said pattern as a mask and said protective layer as a mask and etch stop layer; and

anisotropically etching said protective layer to expose said bitline contact point; and

forming a plurality of bit lines on said interlevel insulating layer said bit lines being in electrical contact with said exposed bit line contact point.

21. A method for forming a device in a trench comprising the steps of:

forming a trench in a substrate;

depositing a layer of material overall;

depositing a layer of photosensitive material so that the remainder of said trench not occupied by said layer of material is filled and said layer of photosensitive material has a substantially planar top surface;

exposing said photosensitive to light sufficient to penetrate said photosensitive material except for the portion of said photosensitive material in said trench;

removing and exposing photosensitive material; and

etching said material using the photosensitive material remaining in said trench as an etch mask.

22. A method as in Claim 21 wherein said photosensitive material is photoresist.

23. A method as in Claim 21 wherein said material is a layer of conductive material.

24. A method as in Claim 23 wherein said remaining portion of said material serves as a plate of a capacitor.

25. An array of memory cells comprising:

a plurality of memory cells formed in a regular array on a substrate, each cell comprising:

a trench formed in said substrate, said trench having no abrupt corners;

a diffused region surrounding said trench;

an insulator formed on the surfaces of said trench;

conductive material formed on the surface of said insulator; and

a transistor having at least one source/drain in conductive contact with said diffused region; wherein trenches of adjacent memory cells have a minimum spacing from the surface of the trenches of between 0.5 and 1.0 microns.

26. An array as in Claim 25 wherein said substrate is silicon.

27. An array as Claim 25 wherein said substrate is doped P type and said diffused region is doped N type.

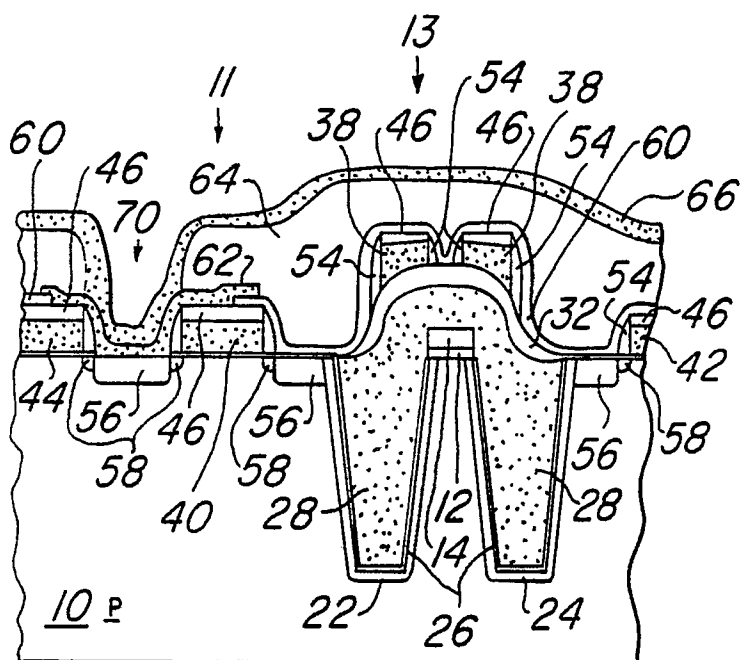


Fig. 1

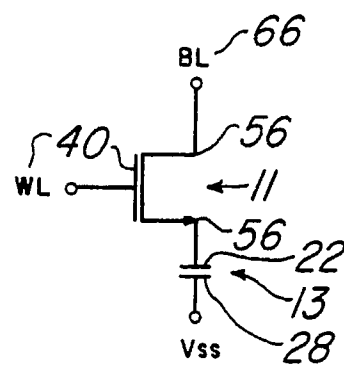


Fig. 2

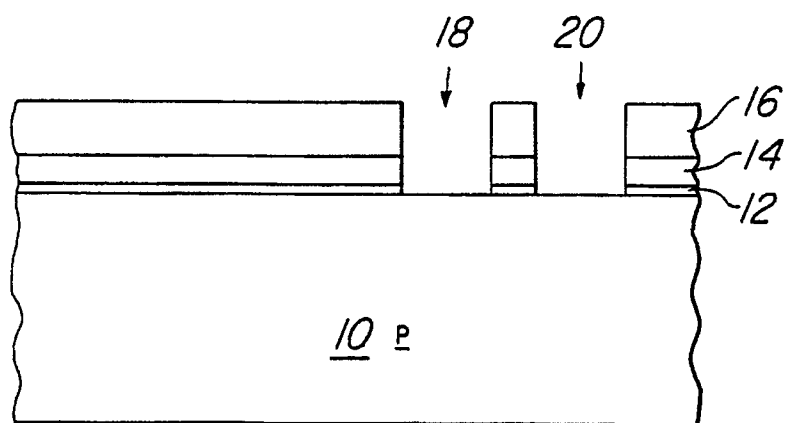


Fig. 3A

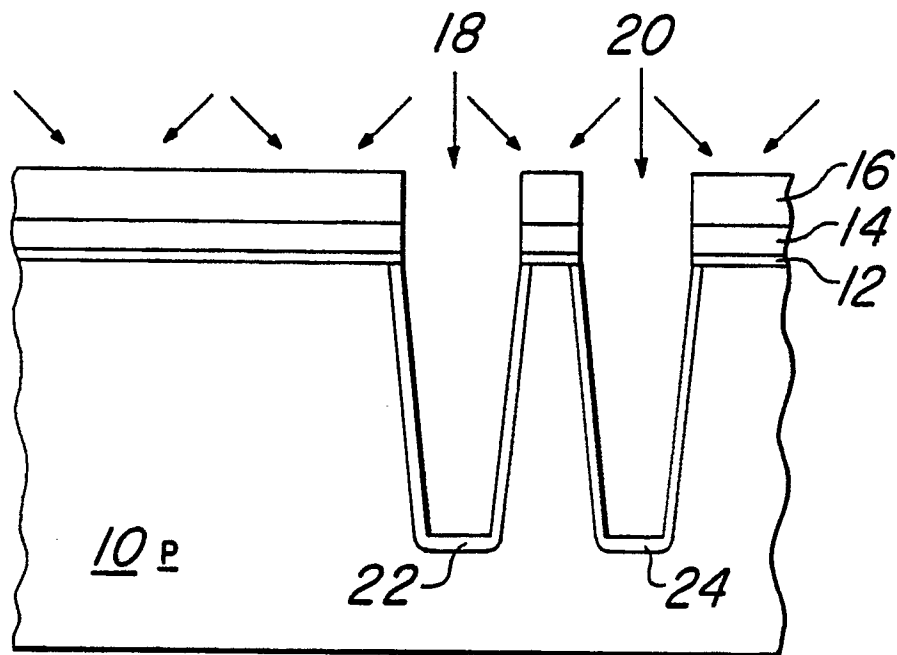


Fig. 3B

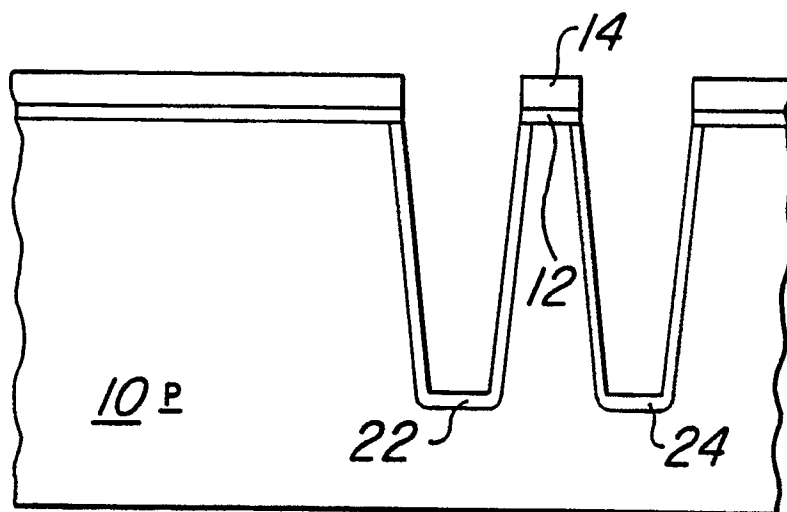


Fig. 3C

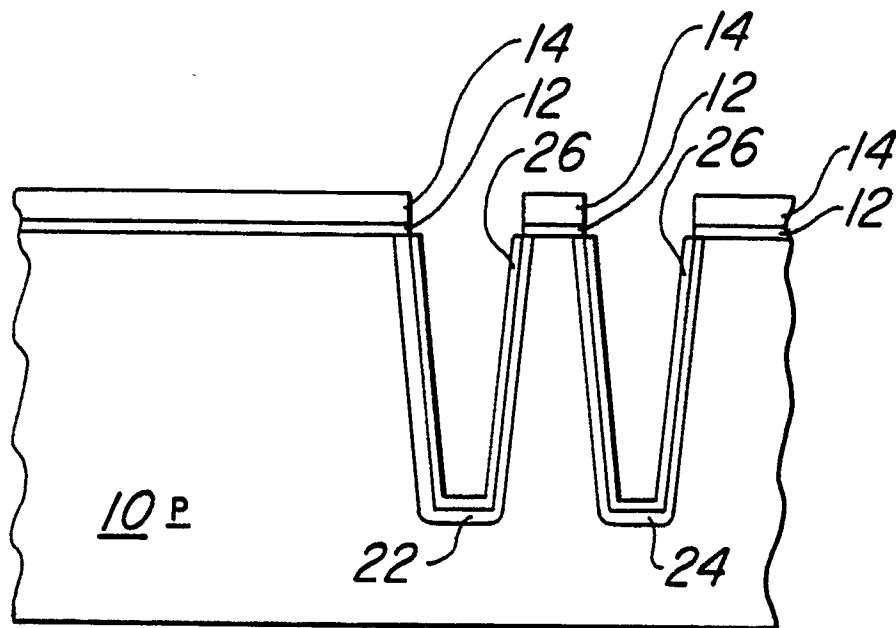


Fig. 3D

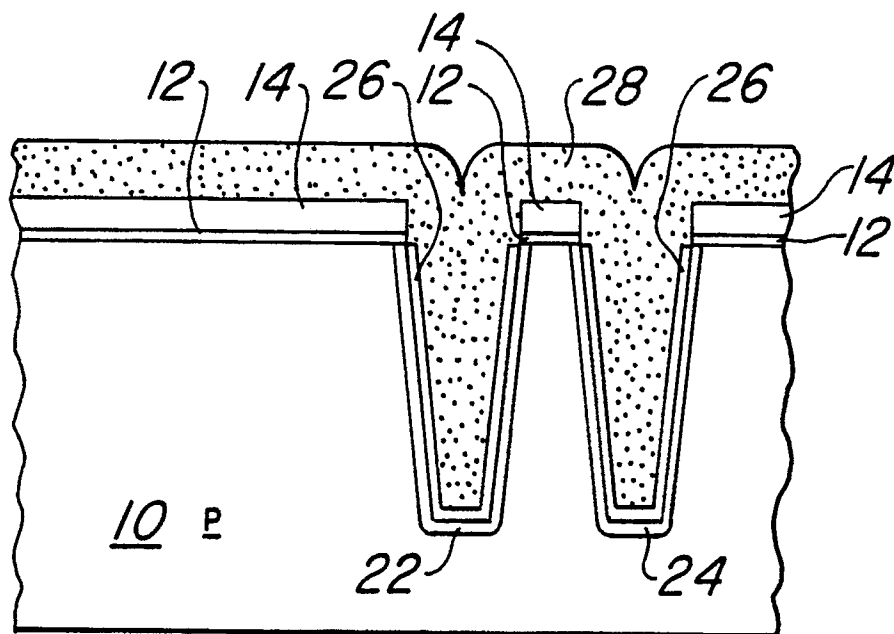


Fig. 3E

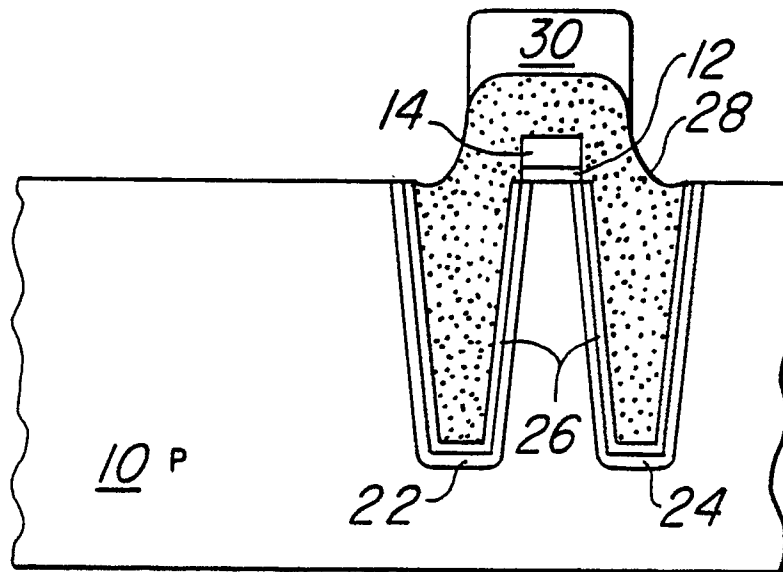


Fig. 3F

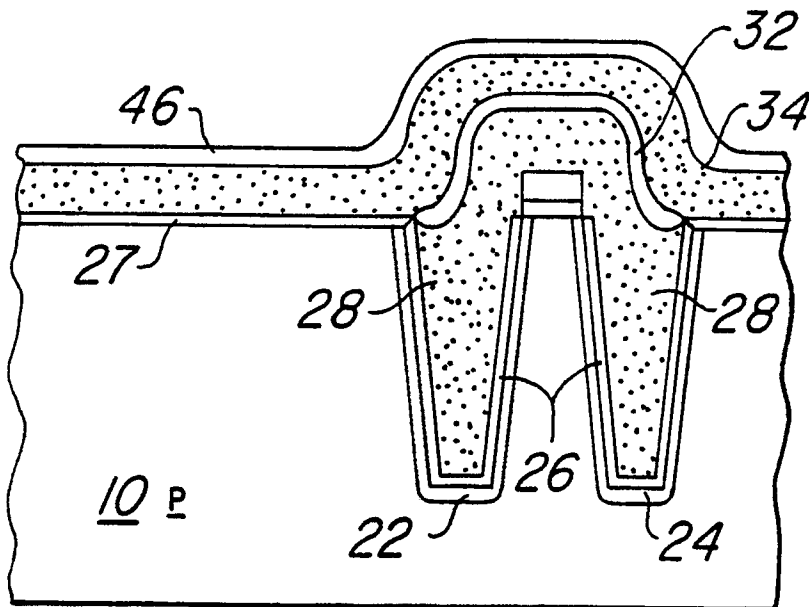


Fig. 3G

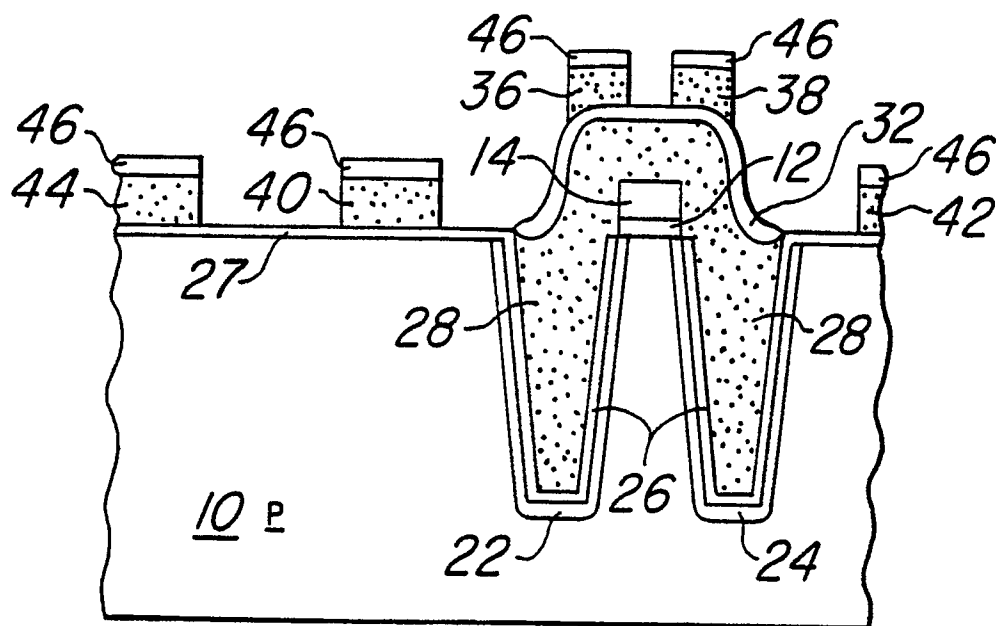


Fig. 3H

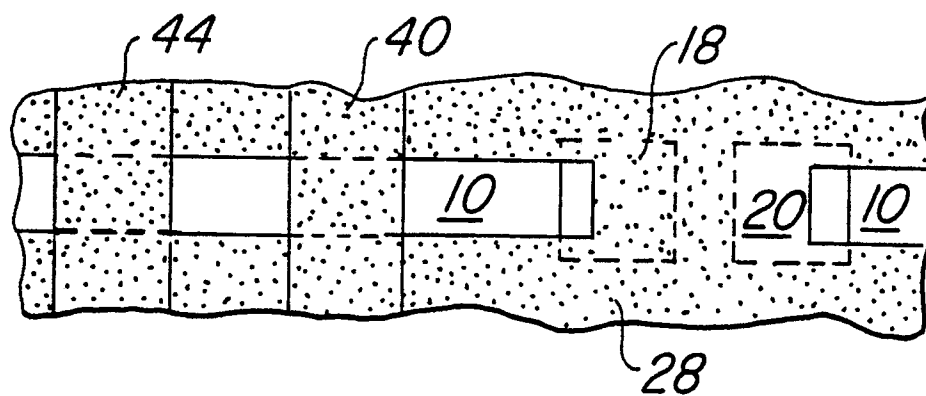


Fig. 3I



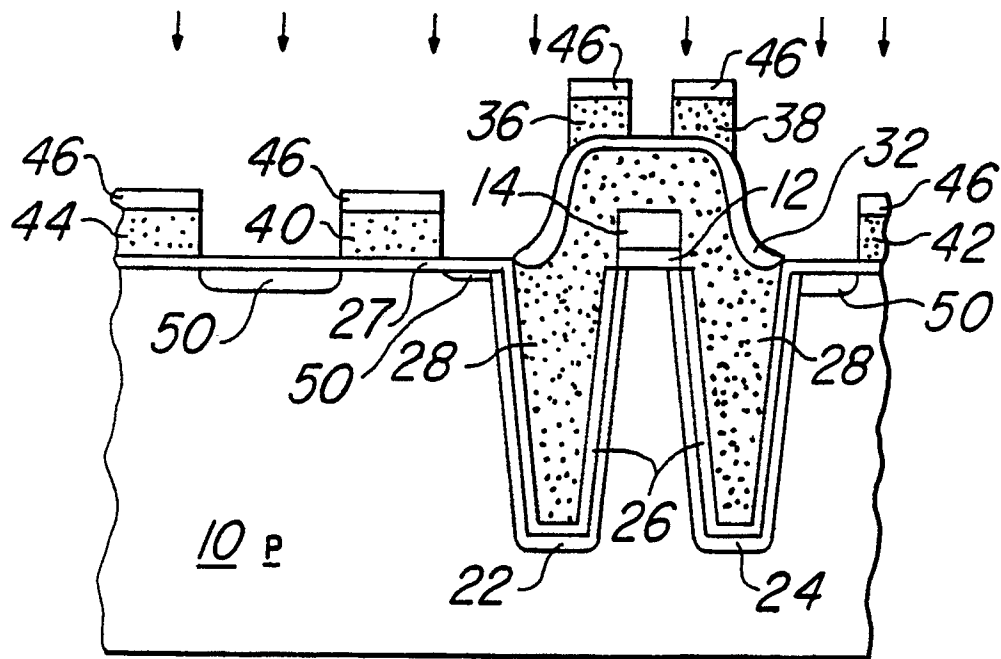


Fig. 3J

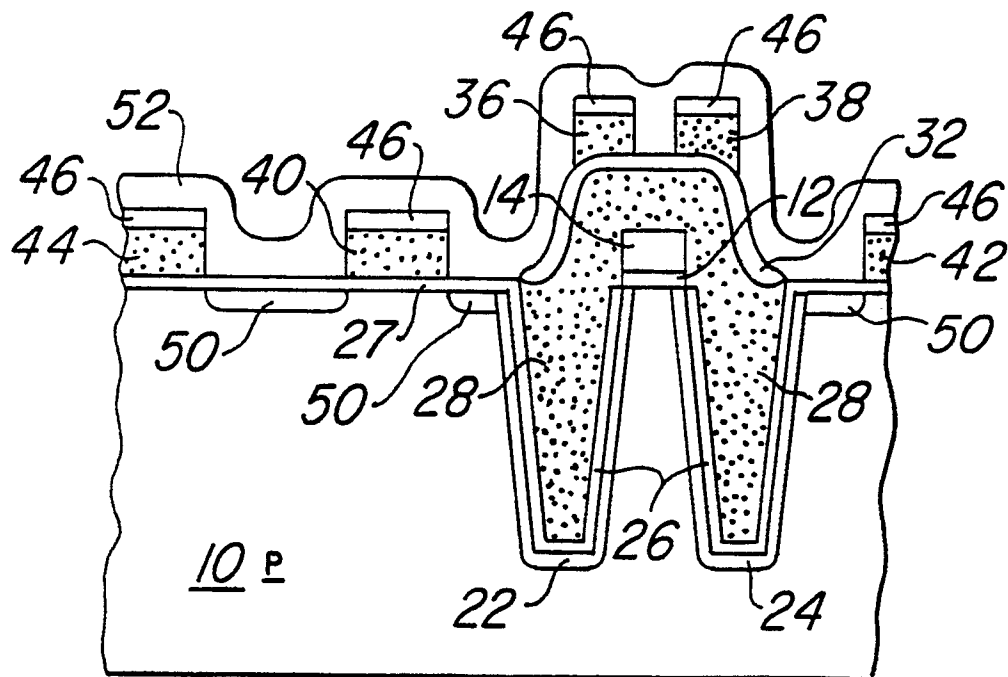


Fig. 3K

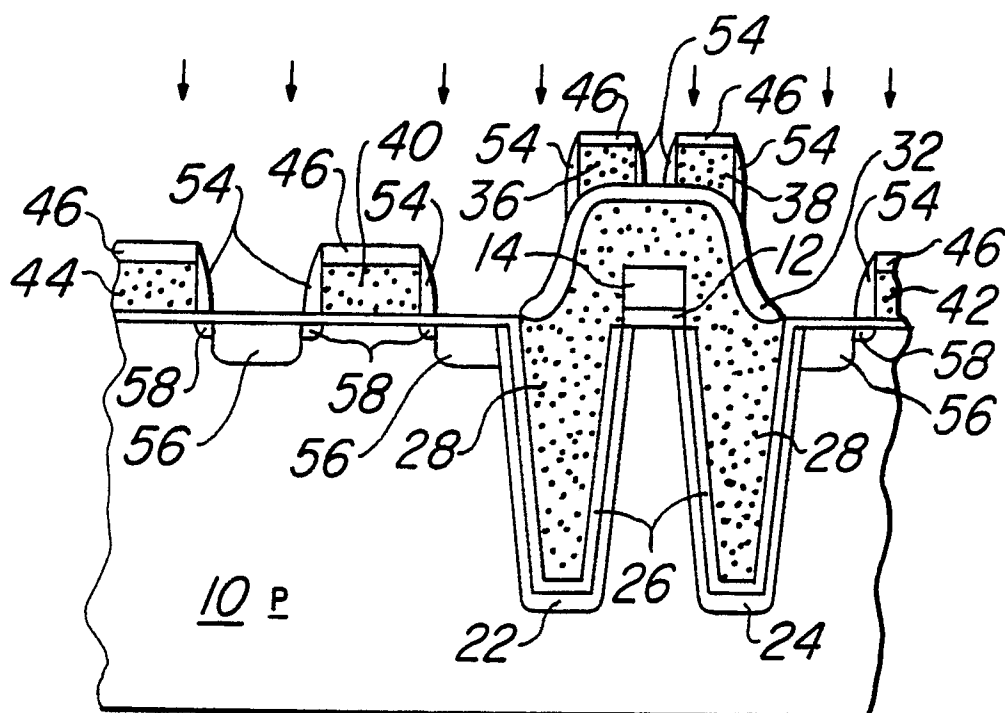


Fig. 3L

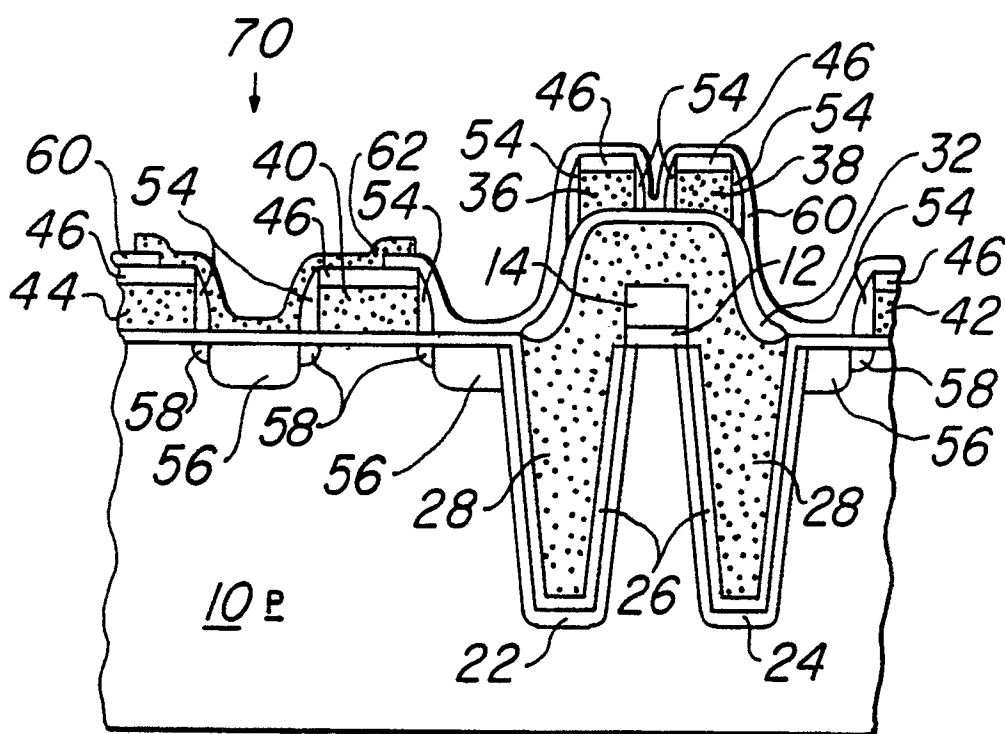


Fig. 3M

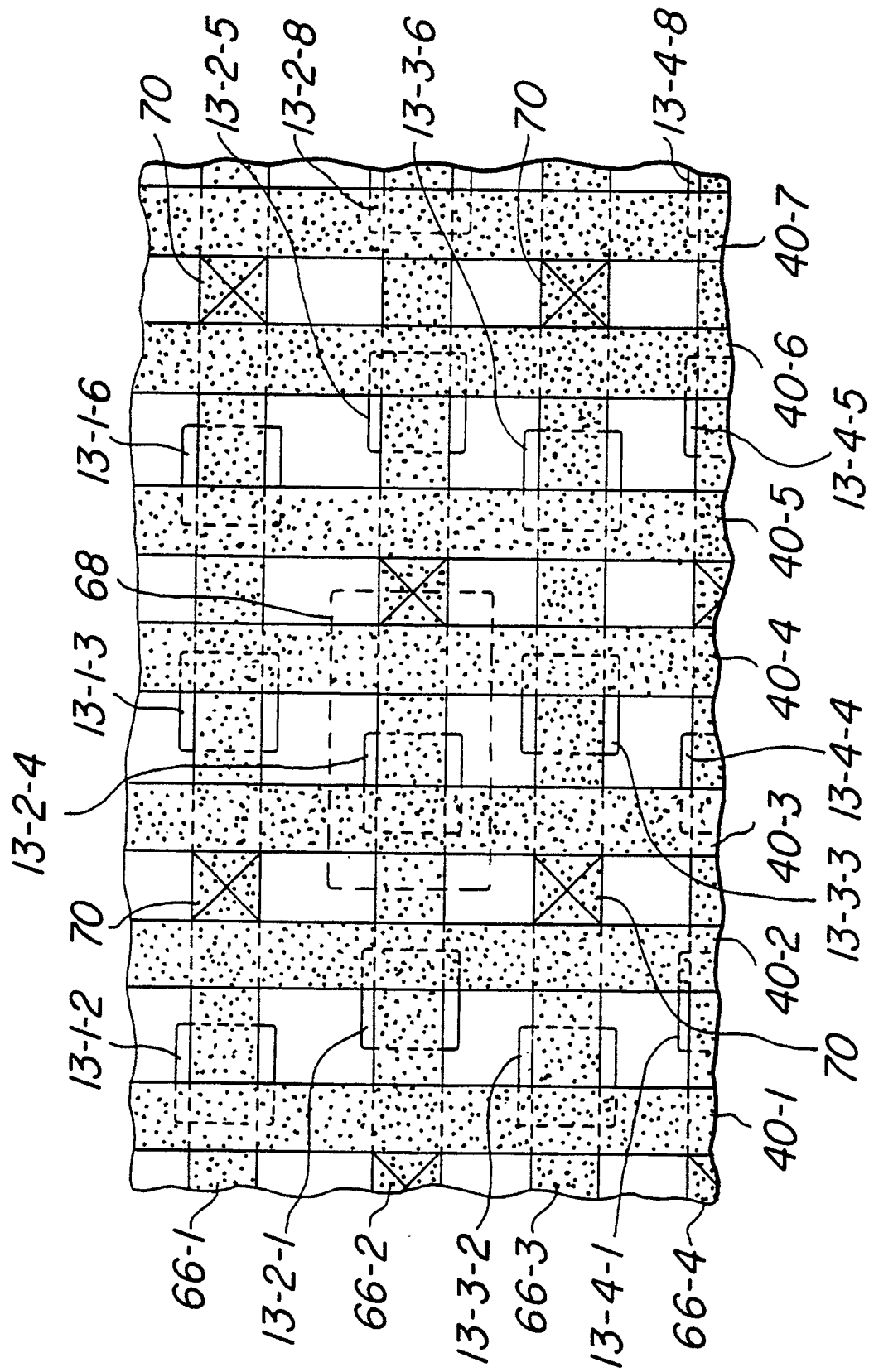


Fig. 4

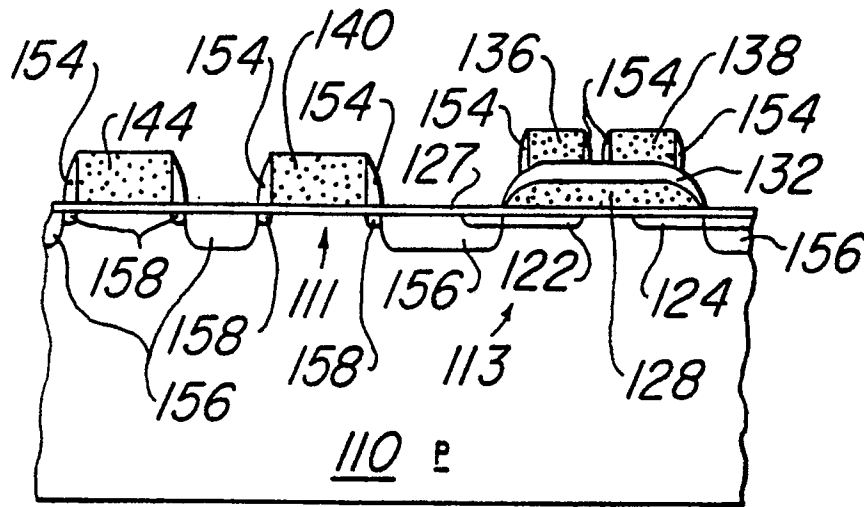


Fig. 5

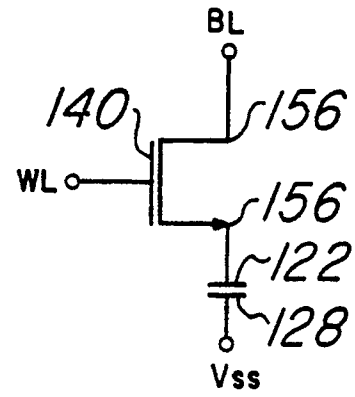


Fig. 6

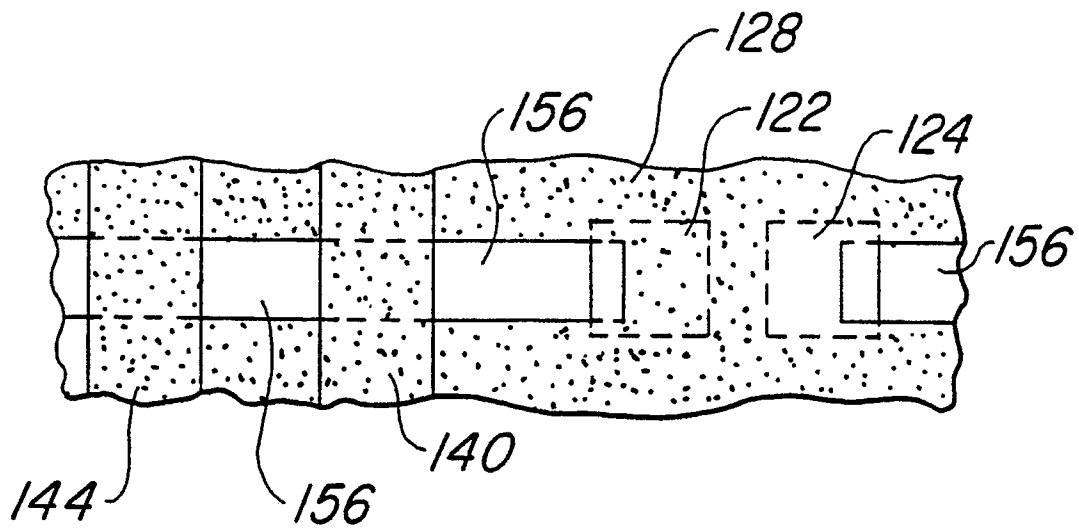


Fig. 7

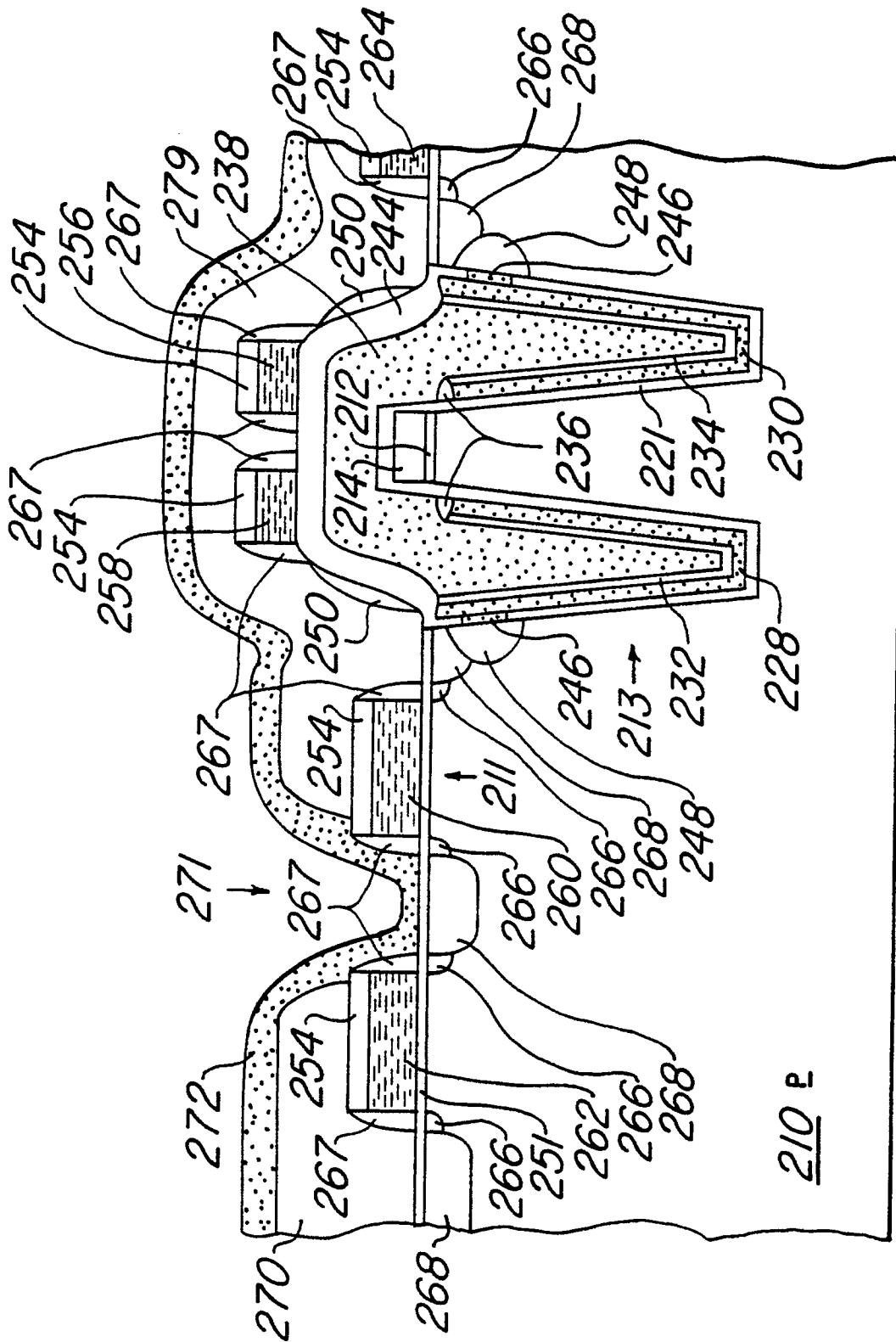


Fig. 8

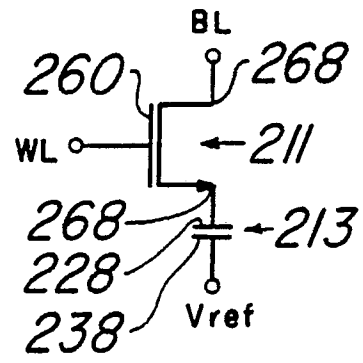


Fig. 9

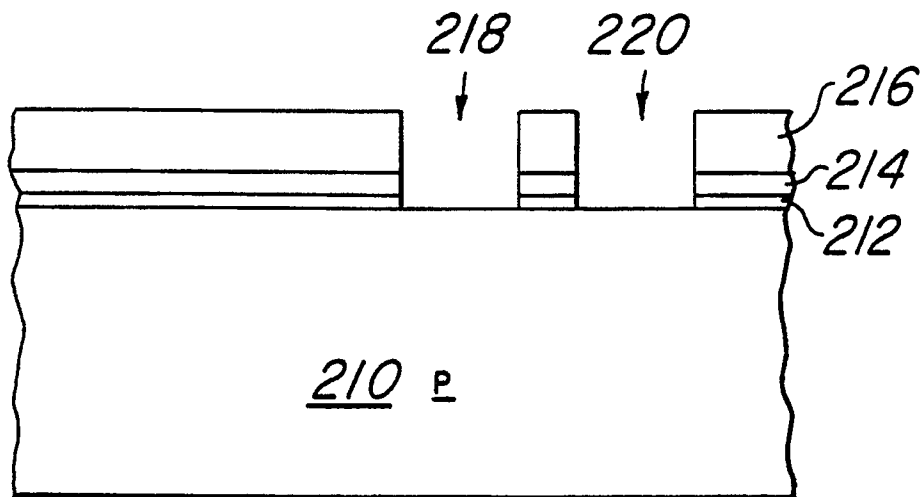


Fig. 10A

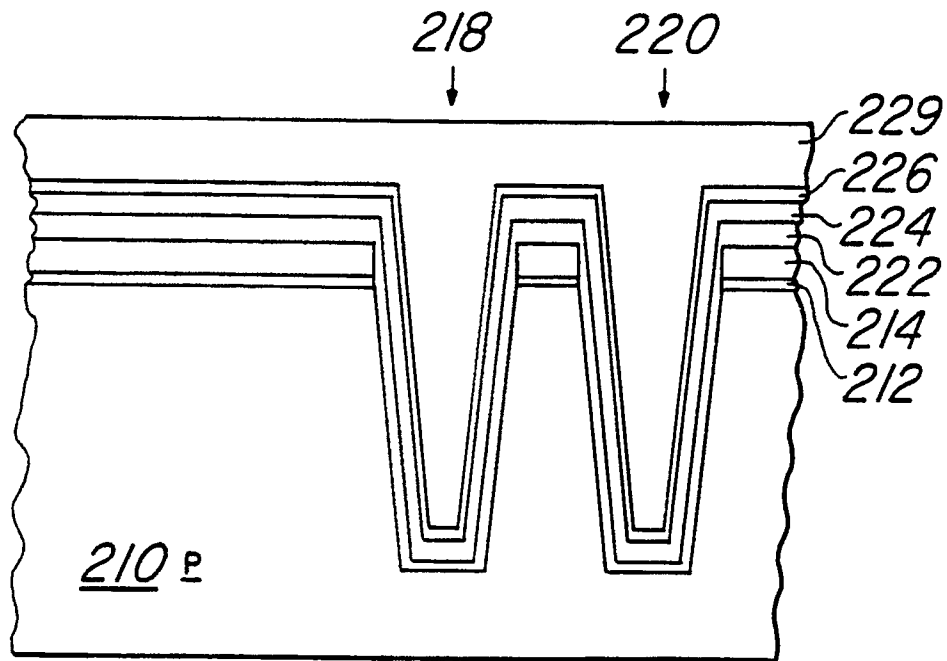


Fig. 10B

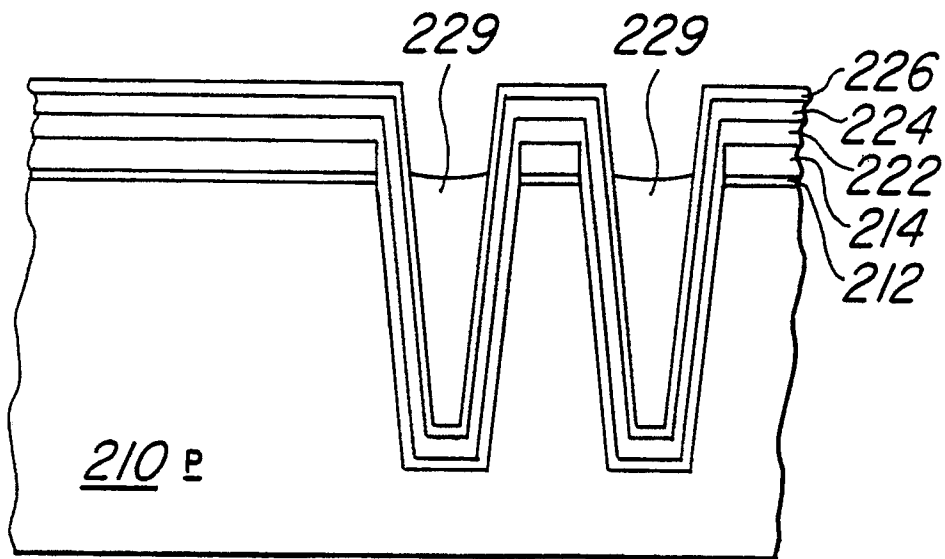
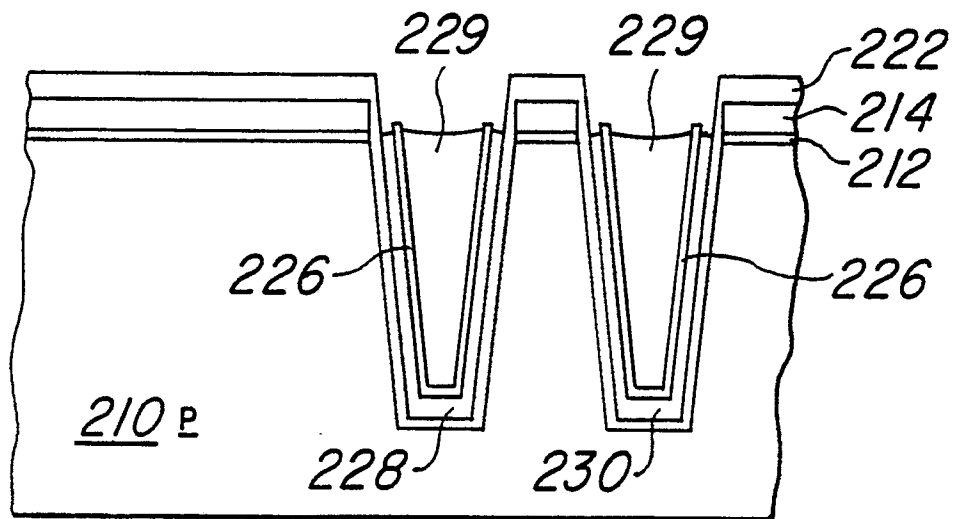
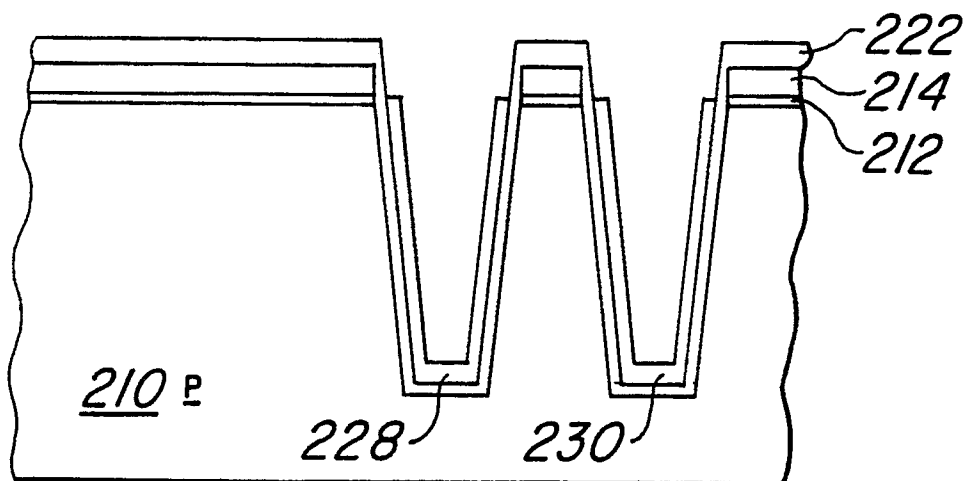


Fig. 10C



*Fig. 10D*



*Fig. 10E*



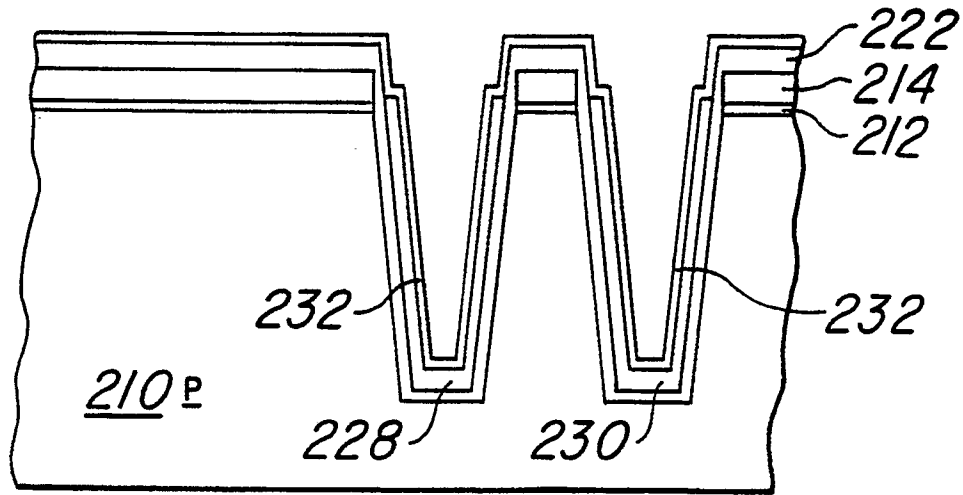


Fig. 10F

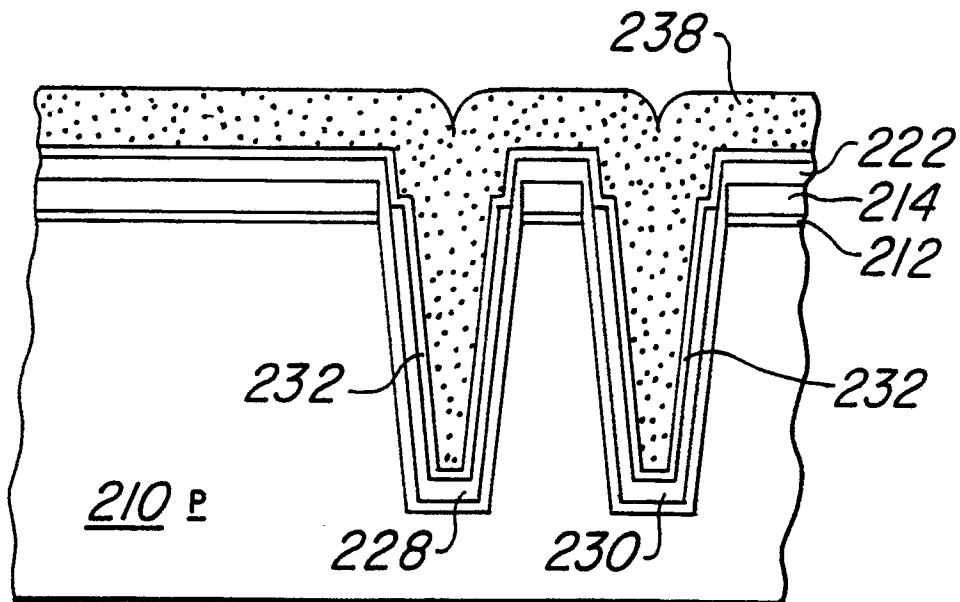


Fig. 10G

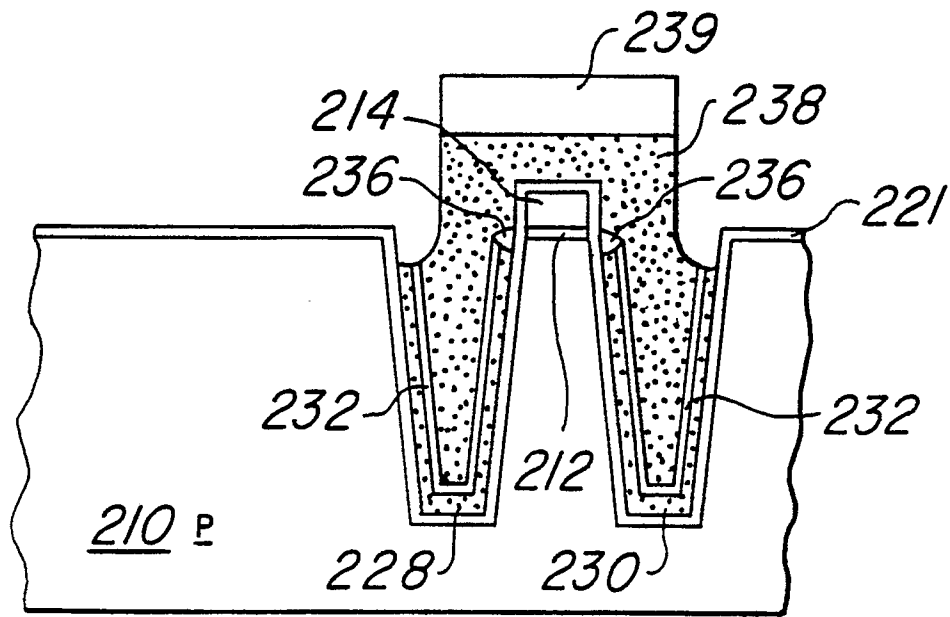


Fig. 10H

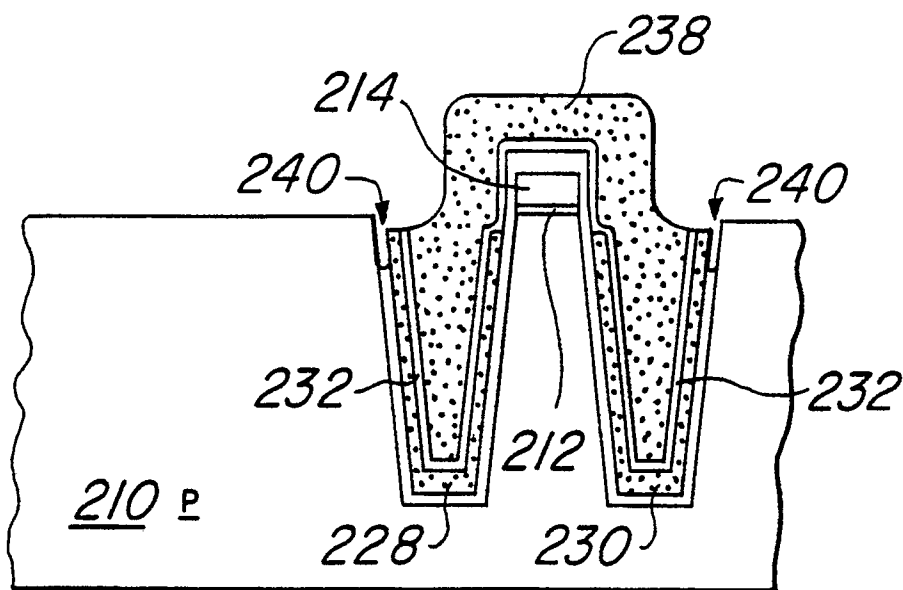


Fig. 10I

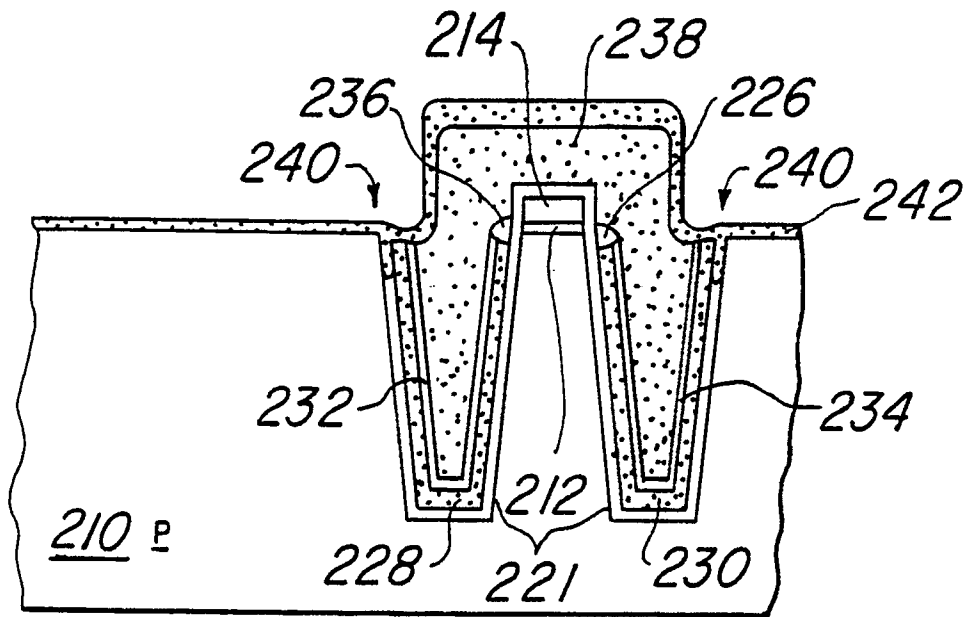


Fig. 10J

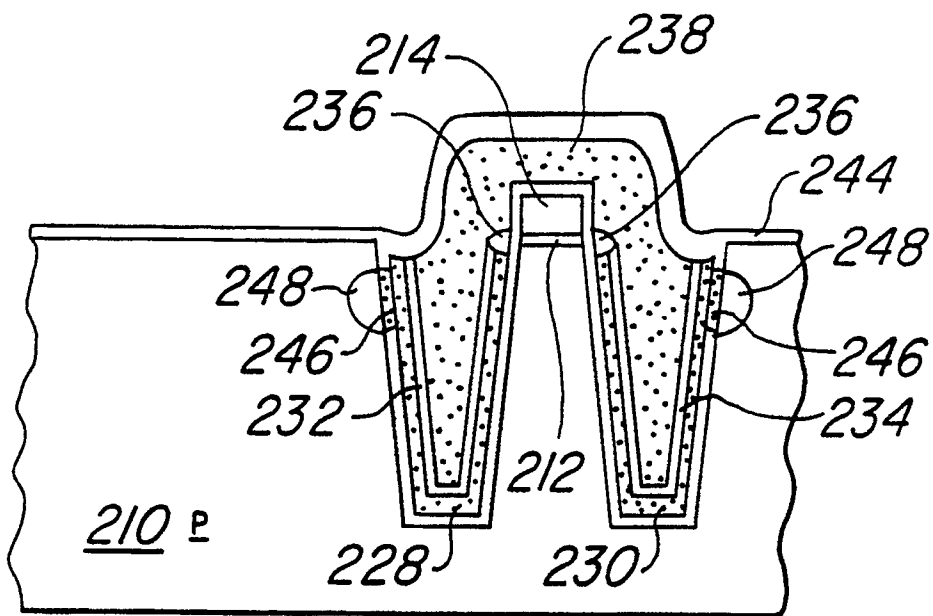


Fig. 10K

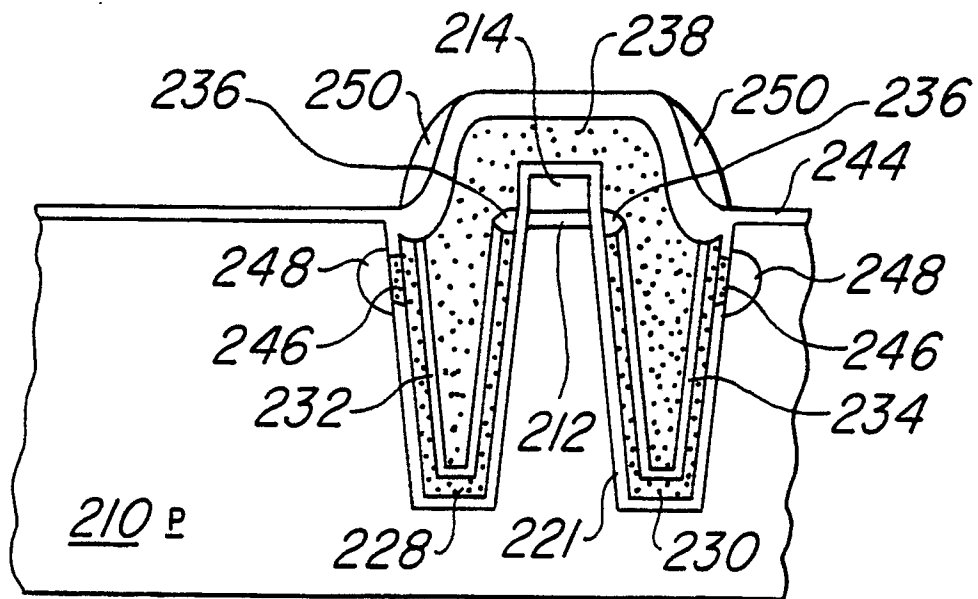


Fig. 10L

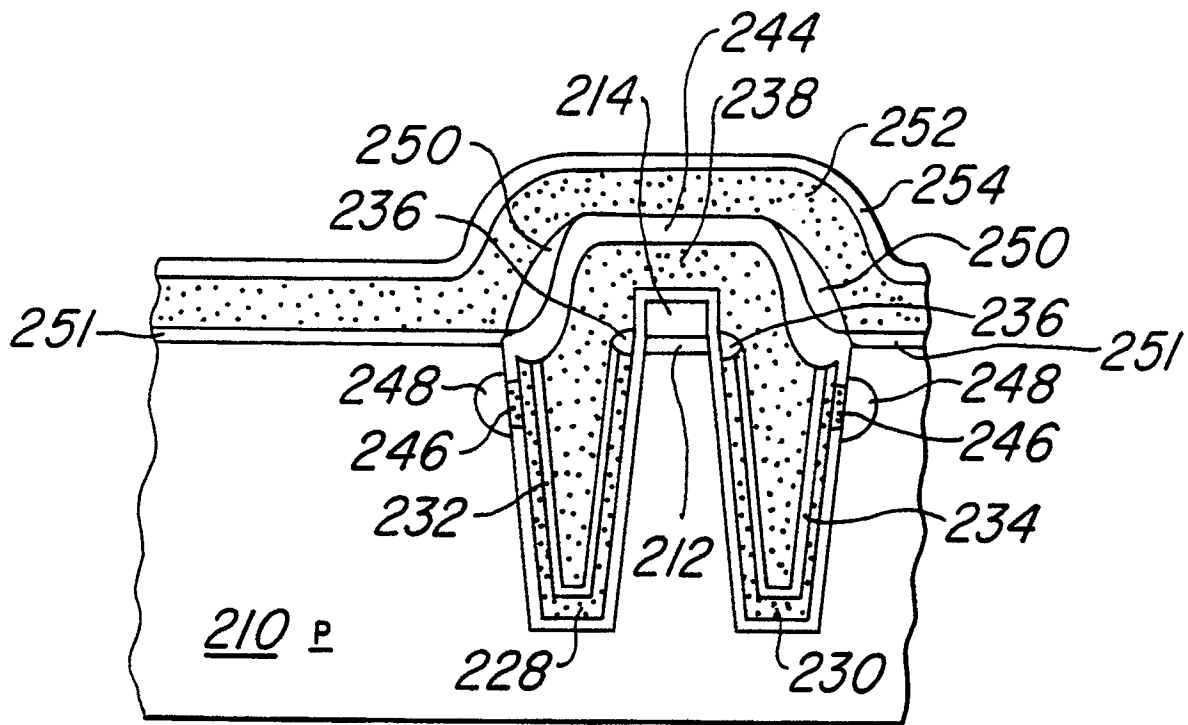


Fig. 10M

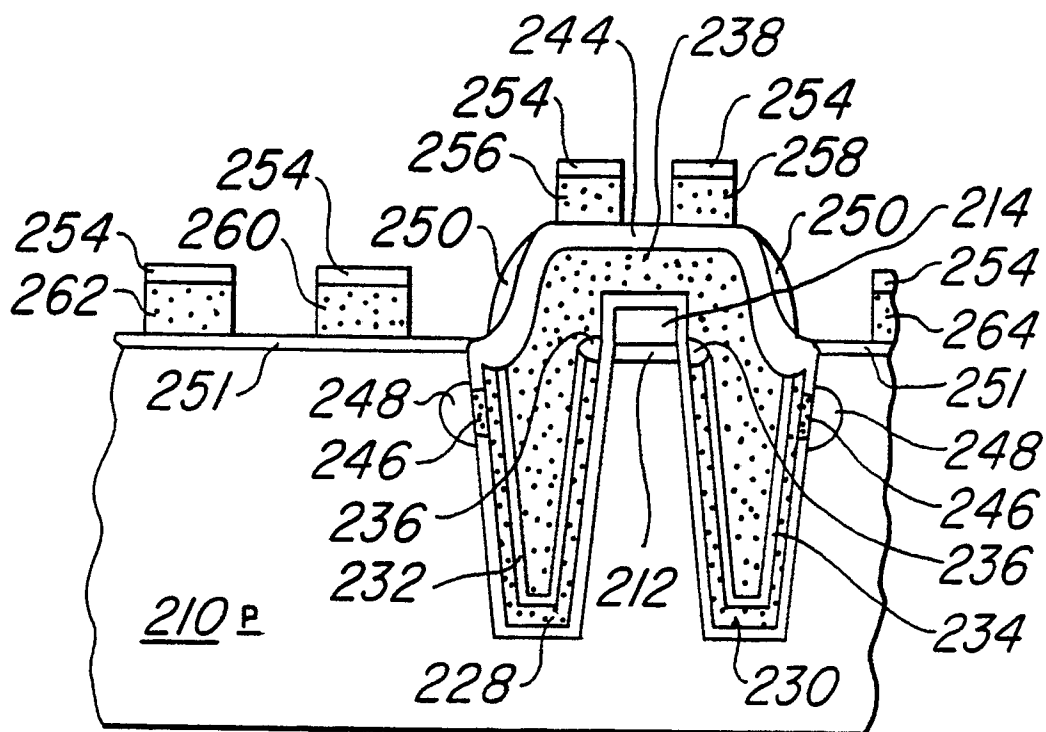


Fig. 10N

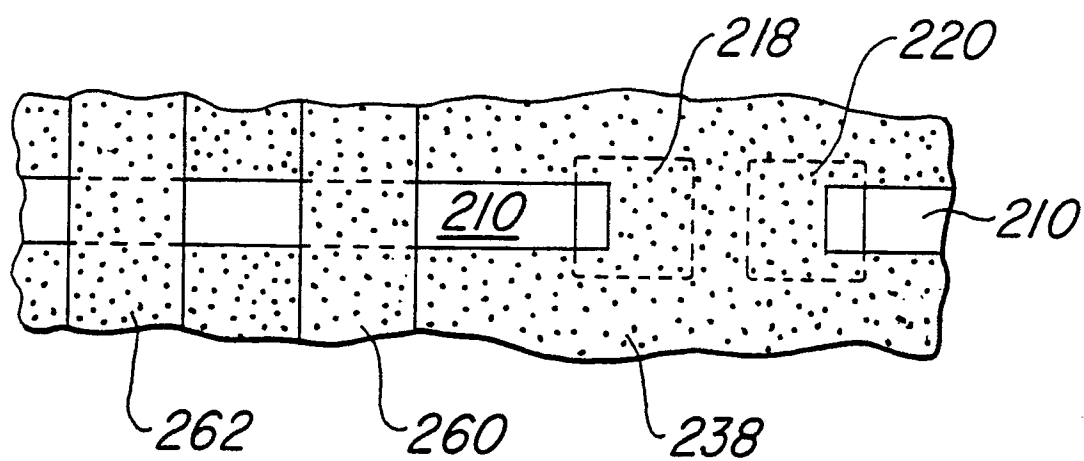


Fig. 10O

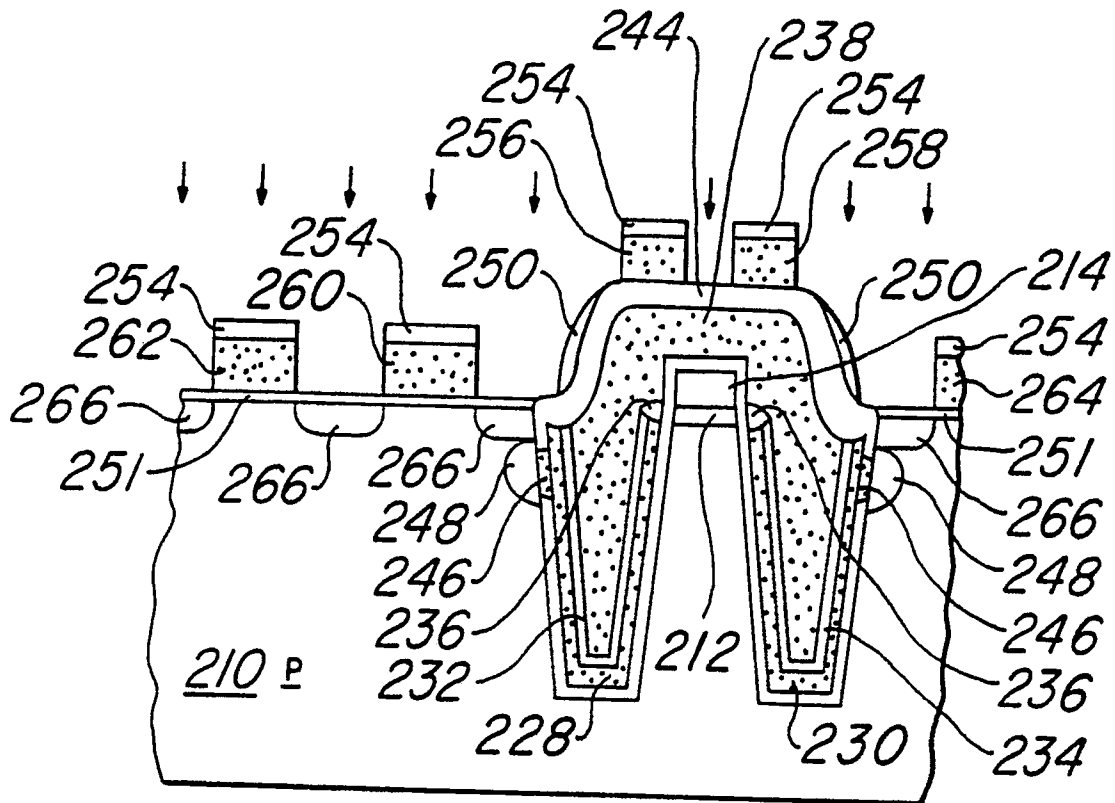


Fig. 10 P

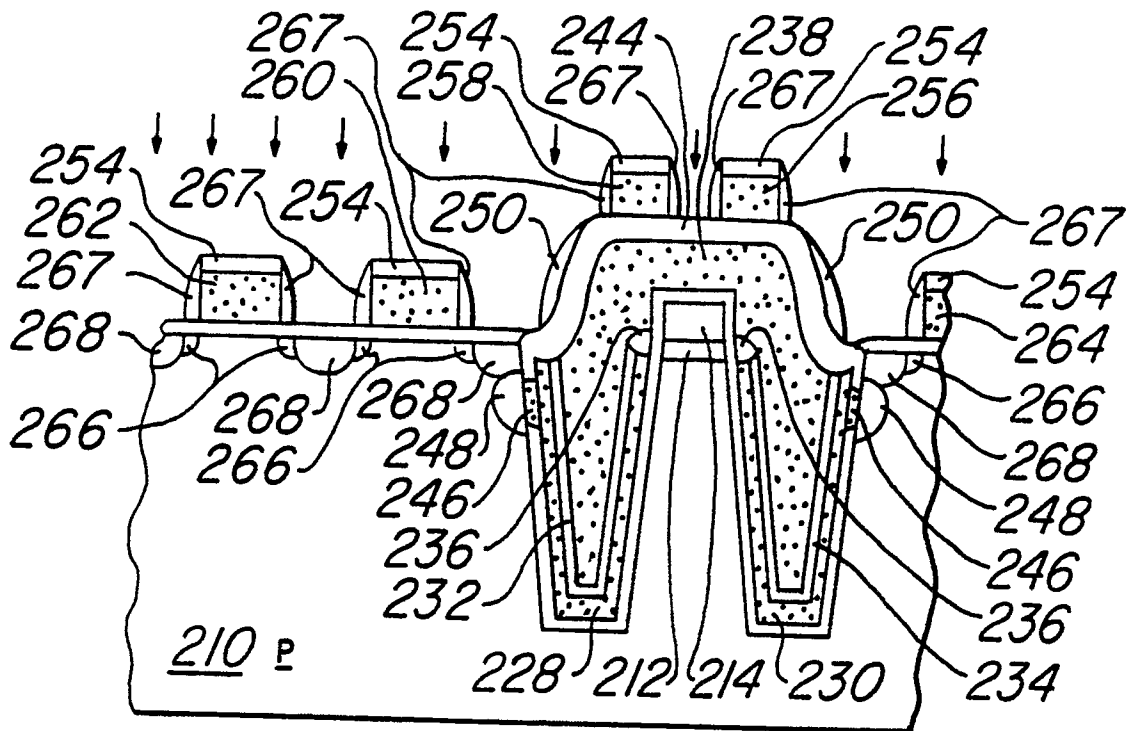


Fig. 10 Q

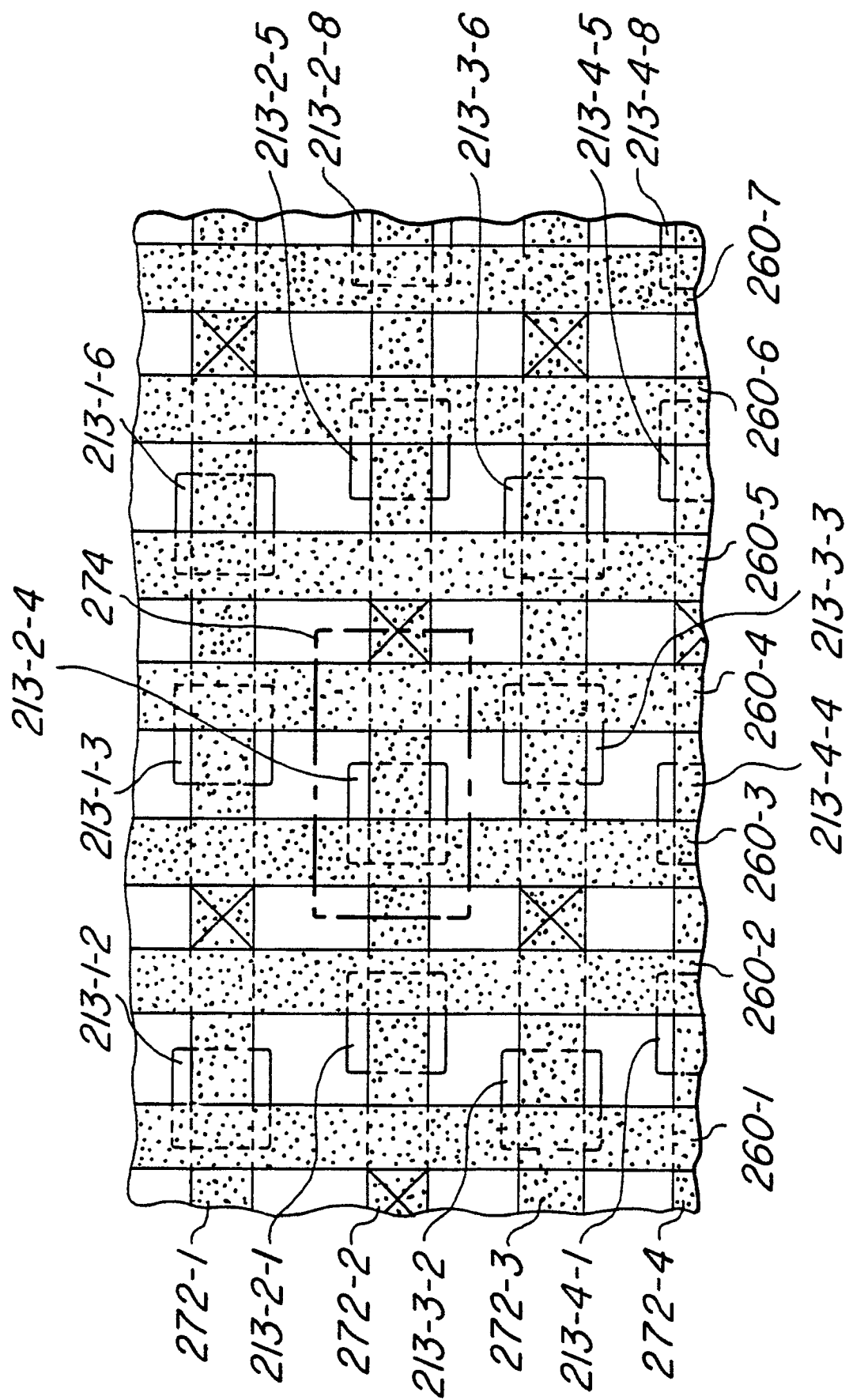


Fig. 11