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(54) Non-volatile semiconductor memory device having an improved testing mode of operation and method of forming checkerwise test pattern in memory cell array.

(57) An EEPROM device comprises a memory cell array (3) having a plurality of non-volatile memory cells (3-1 to 3-256) respectively disposed at locations de fined by word lines (W0 to W31) and bit lines (BL0 to BL7) and memorizing pieces of data information in a rewriteable manner, respectively, a row address decoder circuit (1) responsive to an address signal indicative of a row address for selectively activating one of the word lines, a column address decoder circuit (2) responsive to an address signal indicative of a column address for selecting one of the bit lines, and a data control unit (4 to 9) selectively carrying out erasing, write-in and read-out operations on one of the non-volatile memory cells, in which tle row address decoder circuit is further operative to concurrently activate every second word line in the presence of the row address signal indicative of a first state and to concurrently activate another group of the word lines in the presence of the row address signal indicative of a second state in a testing mode of operation, and in which the data control unit carries out the erase and write-in operations on a plurality of the non-volatile memory cells coupled to the word lines to be activated in the testing mode of operation.

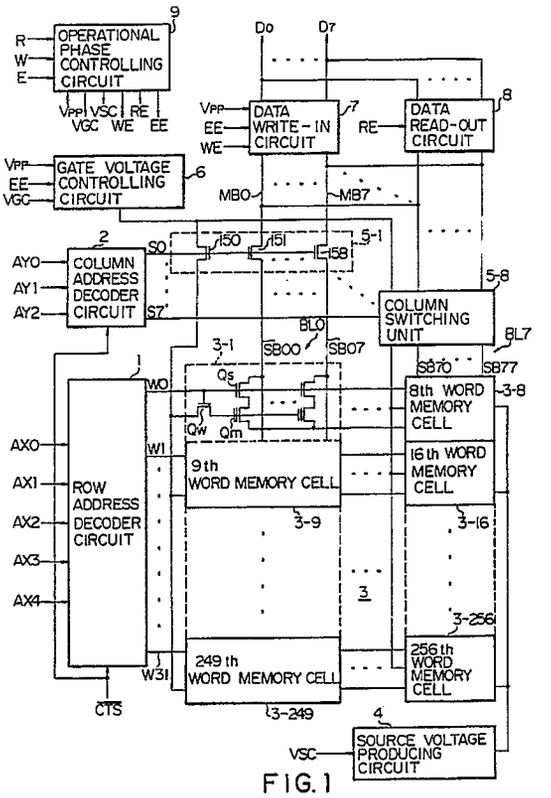

FIG. 1

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EUROPEAN SEARCH REPORT

Application Number

EP 90 11 4519

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 223 188 (FUJITSU LIMITED)	2	G 11 C 29/00
Y	EP-A-0 223 188 (* the whole document *)	1	
Y	PROCEEDINGS OF THE 1986 IEEE INTERNATIONAL TEST CONFERENCE 8 September 1986, PHILADELPHIA, U.S. pages 830 - 839; K.T. LE ET AL.: 'A Novel Approach for Testing Memories Using a Built-in Self Testing Technique' * page 832, left column, line 29 - line 45; figures 6,7; tables 3,4 * *	1	
A	INTEGRATION, THE VLSI JOURNAL. vol. 2, no. 4, December 1984, AMSTERDAM NL pages 309 - 330; K.K. SALUJA ET AL.: 'Testable Design of Large Random Access Memories' * page 313, line 33 - page 316, line 10 * * * page 321, line 1 - page 322, line 6 * * * page 324, line 14 - page 325, line 2 * *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	18 October 91	HERREMAN,G.L.O.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

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