(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 410 777 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **90308245.1**

(51) Int. Cl.5: **G09G 1/16**

(22) Date of filing: **27.07.90**

(30) Priority: **28.07.89 US 387567**
28.07.89 US 387568

(43) Date of publication of application:
30.01.91 Bulletin 91/05

(84) Designated Contracting States:
DE FR GB IT NL

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(54) Video graphics display memory swizzle logic circuit and method.

(57) There is disclosed a circuit and method of operation which controls the reordering of data as it is transferred to control a memory (200). The data to be reordered is presented such that the ordinate bit position within a data word is uniquely associated with a particular input to a data bus (20). The bus inputs, however, are connected to the VRAM (200) in an arrangement contrary to the desired ordinate association with the compressed data word. A single swizzle logic circuit (32) operates to allow graphic compressed data to be reordered for presentation to the block-write inputs of a VRAM (200-207) regardless of the VRAM or pixel size. The circuit (32) relies upon properly expanding the compressed data prior to the actual reordering of the ordinate positions of the data bits.

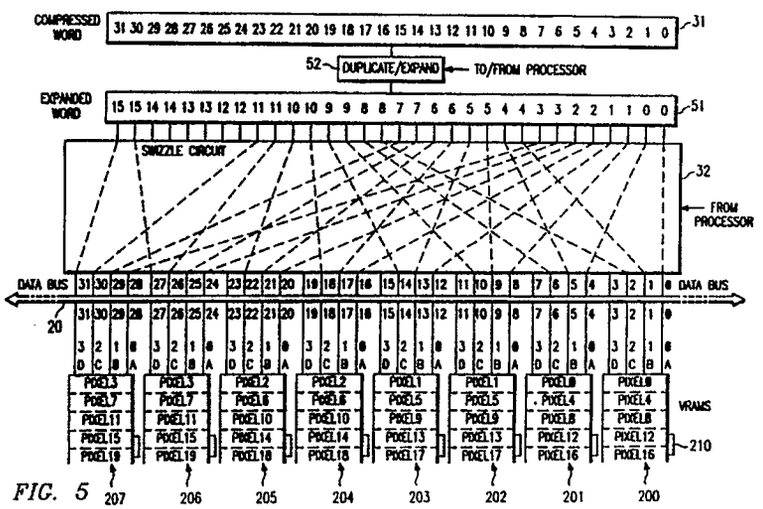

FIG. 5

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VIDEO GRAPHICS DISPLAY MEMORY SWIZZLE LOGIC CIRCUIT AND METHOD

TECHNICAL FIELD OF THE INVENTION

This invention relates to block-write graphic control data memory write systems and more particularly to an arrangement which allows for the economical reordering of data prior to controlling the block-write function.

BACKGROUND OF THE INVENTION

Microprocessors intended for graphics applications must be able to move pixel information between memory bit maps as quickly as possible. In situations where many pixels must be transferred to a bit map, the transfer may be speeded up by using a block-write feature. Typically, a block-write is created by associating a color register with each VRAM, filling the color register with bits to determine the desired color value of selected portions of the VRAM, and then using both the address bits of the VRAM as well as the data bus input to the VRAM to determine the locations within the VRAM where the color represented by the value in the color register will appear. This technique does not burden the data bus with multiple copies of the same pixel value and thus increases the available memory bandwidth, again speeding up data transfers.

The simplest application where the block-write can be used to advantage is the fill, which transfers the same pixel value into a defined area of memory. Also, some forms of data expansion are well suited to the application of block-write techniques. Thus, when a bit map is stored in compressed form the 1's and 0's can represent the presence or absence of a pixel and block-writes can be used to decompress the bit map. Typically, this sort of expansion is applied to character fonts which are often stored in compressed form to save memory.

Problems arise because memory accesses must be made in regular mode and in block-write mode via the same bus and they must be consistent such that data written (or read) in one mode must be able to be read (or written) in the other mode. This is a problem, since before data can be written to VRAMs in block-write mode, the bit order of the compressed representation of the data must be manipulated or swizzled relative to the regular mode access. This bit order change is necessary because typically the compressed data is stored with one bit representing each multibit display pixel in a specific order. The storage of these bits is serial with each bit representing a corresponding display point. For example, the first bit (bit 0) would represent pixel position one. The second bit (bit 1) would represent pixel position two and the third bit (bit 2) would represent pixel position three. Thus, the bits on the bus, in this example would represent the pixel positions one for one, such that bus bit position zero would contain data for the first pixel, while bus position three would contain data for the fourth pixel. However, because of the physical arrangement of the VRAMs where successive pixels are stored in different VRAM chips (or Units), the data must be reordered before presentation to the VRAMS. Consider the case where the VRAMS are four bits wide (four planes) with a 32 bit wide data bus. The data bus would have bus positions 0-3 connected to the first VRAM which in turn can control bits 0-3 of the first pixel in a normal write situation. Without swizzling, the compressed data in bus bit position 1 (the second position) which should be destined to control the second pixel will end up being communicated to the second input of the first VRAM, which with a normal access be associated with the ninth pixel and not the required second pixel. Thus, a bit order rearrangement is necessary when functioning in the block-write mode.

A further problem is encountered since the nature of a data swizzle depends on the size of the pixel. Several different swizzles must be made to accommodate a broad range of pixel sizes and VRAM configurations. Thus, it is fair to say that the block-write mode of the video RAMs can only be reasonably used for filling areas in exact multiples of the block size. The nature of the VRAM's block-write function results in a scrambled writing to the pixels within a block unless some data reordering is accomplished.

Accordingly, a need exists in the art for a swizzle arrangement which allows for the efficient manipulation of data so as to accomplish block-writes in an economical manner.

A further need exists in the art for swizzle logic which can be used for any size pixel or VRAM configuration.

A further need exists in the art to design a system using the block write mode that can correctly and efficiently control the writing down to each pixel within the block as well. Further, there is a need for such a system that can be applied for different numbers of color planes.

SUMMARY OF THE INVENTION

There is designed a swizzle arrangement which can be utilized for many different size pixels. This

circuit takes advantage of the recognition that the need for swizzling occurs because during a block-write access the bits of the data stream directed at the VRAMs are accessing different pixel locations than they would be under normal write conditions if not swizzled. This difference can be thought of as a reordering in the bit stream caused by the fact, as discussed above, that each VRAM handles one pixel (or a part of one pixel) with the pixel having four (or more) bits.

Assuming that each pixel has four bits, and assuming that each VRAM has four data input paths (one for each bit of the pixel), there would be a separation, or reordering, of four bit positions between the compressed data and the actual input to the VRAMs. This reordering is performed by a swizzle circuit.

Thus compressed bus bit 0 goes to post swizzle position 0, while bus bit 1 goes to post swizzle position 4. Likewise, compressed bus bit 2 goes to post swizzle position 8 and compressed bus bit 3 goes to post swizzle position 12. This continues for 7 compressed bit positions with compressed bit 7 going to post swizzle position 28. The next compressed bit, bit 8, goes to post-swizzle position 1, while compressed bit 9 goes to post-swizzle position 5. This discontinuous sequence continues for the full bus width.

In the situation where the pixel size is 8 bits, two four bit wide VRAMs would be required, each holding one-half of the eight bit pixel. In this situation, then, the expansion requires a different algorithm, namely the reordering of the ordinate position of the compressed bits by 8 positions. It is recognized that all VRAMs comprising the same pixel must be provided the same identical control signal. Thus, for a 2 VRAM pixel (for example, 8 bits) two positions of the bus must reflect the same compressed bit value.

There are two options for performing the swizzle. One is to create a larger, i.e. 64 lead, bus. This requires additional or larger VRAMs and more circuitry for controlling the bus. The other option is to have a different swizzle pattern in the swizzle circuit. In both cases the compressed data must control more than one VRAM if the pixel is contained in more than one VRAM.

The memory addressing must be adjusted to correspond to the larger amount of data being written to the VRAM when performing a series of block-write accesses (such as filling a large screen area). Effectively, the 4 data bits going to a VRAM are expanded internally by a factor of 4 in the block-write mode. Thus a 32-bit data bus is expanded to 128 bits inside the VRAMs in block-write mode. Therefore, to efficiently step from one addressable location to the next adjacent one requires that the address be incremented/decremented (depending on direction) by 128 (in terms of the bit address) rather than 32 as would be done in regular addressing.

The swizzle operation in one embodiment could be realized by the proper connection of a multiplexer function for each given bit position. The multiplexing would select between the normal (or straight pass) mode and one or more swizzle functions as needed.

It is a technical advantage of this invention to provide a mechanism for writing pixels to a memory array both in normal mode as well as block write mode in a consistent manner.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and further advantages thereof, reference is now made to the following Detailed Description, taken in conjunction with the accompanying Drawings, in which:

FIGURE 1 shows a stylized view of a VRAM memory;

FIGURE 2 shows a VRAM memory connection to a data bus;

FIGURE 3 shows a swizzle circuit connected to the data bus;

FIGURES 4 and 5 show partial connections for alternate swizzle circuits;

FIGURE 6 shows a four position expansion;

FIGURE 7 shows the swizzle circuit cross-connections for all situations;

FIGURE 8 shows one embodiment of a swizzle circuit; and

FIGURE 9 shows an embodiment of a swizzle circuit used for several different memory configurations.

DETAILED DESCRIPTION OF THE INVENTION

Turning now to FIGURE 1, a brief discussion of the memory structure of a typical graphics memory system is in order before progressing to the actual detailed description of the functioning of the embodiment of this invention. While there are many memory structures and systems which could be used, in the preferred embodiment it is typical to use a structure such as shown in FIGURE 1 which uses eight VRAM memories 200, 201, etc. in an array. Each VRAM memory or unit has a 4 bit data port which can be treated as having planes 11, 12, 13 and 14. The construction of each plane is such that a single data lead is used to write information to that plane. These leads are labeled 0, 1, 2, and 3 for each plane. In a system that uses a 32 bit data bus, such as data bus 20, there would be 8

VRAM memories (two of which are shown in FIGURE 1) each memory having four data leads connected to the data bus.

Thus, for a 32 bit data bus VRAM memory 200 would have its four data leads connected to data bus leads 0, 1, 2, 3, respectively. Likewise, VRAM memory 201 would have its four leads 0, 1, 2, 3 connected to data bus leads 4, 5, 6, 7, respectively. This continues for the remaining six VRAM's such that the last VRAM has its leads connected to leads 28, 29, 30, 31 of bus 20. The full set of connections is shown in FIGURE 2.

Continuing with FIGURE 1, the memories are arranged such that the pixel information for the graphics display is stored serially across the planes in the same row. Assuming a four bit per pixel system, then successive pixels are stored in successive VRAMs. In such a situation pixel 0 would be in VRAM 200, and pixel 1 would be in VRAM 201. The pixel storage for pixels 2 through 7 are not shown in FIGURE 1 but are shown in FIGURE 2. The pixel information for pixel 8 then would be stored in VRAM 200, still in row 1 but in column 2 thereof. The reason for this arrangement of pixel information will be more fully appreciated from an understanding of how information is retrieved from the memory.

Continuing with FIGURE 1, each VRAM plane has a serial register 16 for shifting out information from a row of memory. The outputs from these registers are connected to data out bus 15 in the same manner as the data input leads are connected to the data input bus. Thus, data from a row of memory, say row 1, would be moved into register 16. This would occur for each plane of the eight memory array.

Looking at data output bus 15 at an instant of time, the first bit in each shift register would be on the bus. Thus assuming row 1 was being outputted to the bus, the bus would have on its lead 0 the row 1 bit A1 of memory 200. output bus 15 lead 1 would have on it row 1, bit B1; lead 2 would have row I, bit C1; and lead 3 would have on it row 1, bit D1. These bits would be followed by memory 201 row 1 bits, A1, B1, C1, D1 on leads 4, 5, 6, 7, respectively. Thus, at a first instant of time, data out bus 15 would have on it the four bits forming pixel 0 followed by the four bits forming pixel 1, followed by the four bits forming pixel 2. This would continue until the 32 bits forming the 8 pixels 0-7 were on the consecutive leads of data out bus 15. These bits would be supplied to the graphics display and the shift registers would all shift one position providing the bus with pixel information for the next 8 pixels, namely pixels 8 through 15. This shifting would then continue until the entire line was shifted out and then a new line would be selected for loading into the output register.

Up to this point we have assumed that the bit information per pixel is 4 bits. If the pixel information were to be, say 8 bits, then two 4 bit wide VRAMs would have to be used for each pixel. This would change the bit patterns somewhat. This aspect of the invention will be discussed in further detail hereinafter. Also, it should be noted that memory sizes and structures continue to vary and the size and structure shown are only for illustrative purposes and this invention can be used with many different memory configurations and with different pixel sizes.

It must be noted that the depiction of memory in FIGURES 2 through 5 is a one-dimensional representation of what is conceptually a three-dimensional array as shown in FIGURE 1. Therefore, from this point, on the term "row" refers to the set of pixels addressed at any one time from the bus.

Turning now to FIGURE 2, a full eight VRAM memory arrangement is shown with the information for controlling pixels 0-7 contained in the top row of VRAMs 200 through 207, while pixels 8 through 15 are in row 2, and pixels 16 through 23 are in row 3, and pixels 24 through 31 are in row 4. This arrangement continues for each additional row of memory.

For normal write operations to the VRAM memory, bits of data are received over data bus 20. The position of the information on the bus determines where the data is to be stored in the VRAMs. Thus, a bit on lead 0 of bus 20 goes onto lead 0 of VRAM 200. Assuming the address location of the first row of VRAM 200 has also been selected, that bit information would become associated with bit 0 of pixel 0. This is the well known traditional operation of graphics systems and details of this operation will not be undertaken here. It is sufficient for our understanding of this invention to note that a given data word, such as data word 21, has bits in ordinate position and these bits will be transferred directly to the proper bit positions within the VRAMs because of the physical connections and associations between the data bus and the VRAMs. Also note that information in ordinate positions 0-3 of data word 21 can go, via bus 20, to one of many pixels 0, 8, 16, 24, 32, etc. The actual storage location will depend upon other concurrent addressing to the VRAMs, all of which is not shown here but is well known in the art.

The method of presentation of data as described above requires 22 bits of data, and a full memory write cycle for each row (8 pixels). In some situations, for example, when a background color is to be painted on a screen, many pixels will have the same information written to them. The block-write method of loading a VRAM has been devised to handle this situation. This operation,

which is well known in the art, uses a special register on each VRAM, such as register 210 shown in conjunction with VRAM 200, which contains bits for transfer to selected pixel locations within memory. These bits are loaded prior to the start of any block-write operation.

During the block-write operation the memory is loaded in a manner different from normal loading. The four data input leads are used, but this time each bit controls the transfer of the special register bits to a particular memory row in that VRAM. For example, in VRAM 200 assume it is desired to load pixels 0, 8 and 24 with the bits from register 210 while leaving pixel 16 unchanged. In this situation, leads 0, 1, 3 would have logical 1's thereon while lead 2 would contain a logical 0. This same situation would prevail for the entire 32 bit bus in that the ordinate position of the bits would determine whether or not information is to be transferred into a corresponding pixel in a corresponding VRAM memory row. This, it will be appreciated, is different from the normal loading of data where the data itself comes from the data bus. For block-write operations, the data comes from the special registers associated with each VRAM and the bits on the data bus merely give on-off or load-not load control depending upon their position on the various leads of the bus.

The data word that controls this operation is then said to be in compressed format such that the ordinate position of each bit being either a 1 or 0 controls a function. Also it should be noted that 1 and 0 representing on and off, respectively, is merely illustrative and the reverse may be true also.

Turning now to FIGURE 3, it will be seen that compressed data word 31 has ordinate positions 0-31 which must be presented to the VRAMs to control various pixels in accordance with the ordinate position of the data in the word. Thus, pixel 0 is to be controlled by compressed data bit 0, while pixel 1 is to be controlled by compressed data bit 1. In this manner, compressed data bit 31 should then control pixel 31. This is easier said than done.

Pixel 0 is easy since it is controlled by lead 0 of VRAM 200 which is connected to compressed bit 0. However, the bit in position 1 of compressed data word 39 begins the problem. In FIGURE 2 this non-compressed bit is connected to pin 1 of VRAM 200. However, as discussed above, the bit in compressed data ordinate position 1 is used to control the writing of information from the special register into pixel 1. Pixel 1 is controlled, in turn, by a 1 or 0 on lead 1 of VRAM 201. This lead, in turn, is connected to lead 4 of bus 20. A comparison of FIGURES 2 and 3 will show that in one situation bit position 1 of the input data word goes to lead 1 of bus 20 while in the other situation it goes to lead 4. Thus, clearly a reordering of bits is necessary when compressed words are used to control data transfer in the block-write mode.

This reordering is accomplished by swizzle circuit 32 which is interposed between the compressed data input and the actual data bus. Swizzle circuit 32 is controlled by the processor to allow data to flow straight through, as would be the situation for FIGURE 2, or to reorder the leads in a certain pattern as is required for FIGURE 3. This arrangement does not require processor time to rearrange information, but rather establishes a pattern based on the physical structure of the memory bus arrangement and calls upon that structure whenever a block-write operation is invoked.

The swizzle circuit could be hard wired or could be software controlled within or outside of the processor.

Now let us assume that instead of four bits per pixel it is desired to use eight bits per pixel and retain a 32-bit data bus. Also let us assume that we continue using VRAMs having four planes per unit as discussed with respect to FIGURE 1. In such a situation the reordering of the bits from the compressed word would be different than it was when only four bits per pixel were used. This can easily be seen in FIGURE 4 where VRAMSs 200 and 201 now both contain pixel 1 information, while VRAMs 202,203 contain pixel 1 information.

It follows then that while again compressed data bit 0 continues to be associated with lead 0 of VRAM 200, all the other ordinate positions of the compressed word are associated with different leads of the bus. Take for example compressed word ordinate position 2. In FIGURE 3, compressed data word ordinate position 2 is associated with pixel 2 and bus lead 8. However, in FIGURE 4 the association is with bus lead 16. This then argues for a separate swizzle for systems where there is different pixel configurations. Also, since half of each pixel is contained in a separate VRAM, both halves are controlled by the same compressed data control bit. Thus, each compressed data control bit must be duplicated once for each additional VRAM which contains part of a given pixel. This also argues different swizzles for each pixel configuration.

From FIGURE 4 it is clear that because each bit of the compressed word connects to two VRAM inputs that only 16 bits of the compressed word will control all of the VRAMs in a 32 bit bus configuration. The first system for solving this problem is to maintain the 32 bit bus and take two bus cycles to use both halves of the 32 bit compressed word. The other option is to use all 32 bits of the compressed word which expands the data bus to 64 bits.

FIGURE 9 shows a schematic diagram of how a simple multiplexer would achieve the required swizzle for output bits 0, 1, and 2 for supporting the 4 plane and 8 plane modes of the preferred embodiment. In normal mode the multiplexer function simply passes the corresponding bit position from input to output (i.e. 0 to 0, 1 to 1, and 2 to 2). For the 4 plane mode selection, the input to output connections are made as outlined in FIGURE 4 (0 to 0, 8 to 1, 16 to 2). For the 8 plane selection, the connections are made as outlined in FIGURE 5 (0 to 0, 0 to 4, 8 to 2). Of course, other multiplexer functions could be made to support other numbers of planes and different bus organizations.

While in the preferred embodiment, the swizzle function is performed by multiplexer hardware function, other means such as a software based table lookup method could be used to perform the swizzle.

Turning to FIGURE 5, it is seen that expanding the compressed word by duplicating each bit corresponding to the number of VRAMs used per pixel will result in the ability to use the same swizzle circuit for different memory/pixel configurations. This solution, as performed by duplicating/expansion circuit 52 has the effect of also activating both VRAMs of a given pixel, since the color information must be provided to all pixel bits even when these bits are positioned within two VRAMs.

The essence of the operation is the fact that the duplication and expansion occurs prior to the swizzle operation, thereby allowing the same swizzle configuration for both operations. In typical operations the same configuration would be used for any given system and thus only one determination of duplication/expansion need be made. However, situations may arise where more than one VRAM system configuration is controlled by the same processor, and thus dynamic control can be required. This can easily be achieved by arranging duplicate/expansion circuit 52 to function under control of the system processor on a case by case basis.

Duplicate/expansion circuit 52 can be any type of register circuit or processor that can reorder and pad numbers. This can be operated by microcode under control of the main processor or by a special processor or can be performed by a host processor if desired. The function performed by circuit 52 is mathmatical in nature and thus one skilled in the art can easily devise many arrangements to perform the desired function.

Circuit 52 can be system adaptable to change the duplicating and expansion function on a dynamic basis in response to received data or in response to a flag in a register to allow for changing pixel/memory configurations. Thus, for a pixel size of 16 bits and a VRAM of the same size as shown in FIGURE 1, namely four bits, four VRAMS would be used for each pixel and thus the expansion would be by four bits. In this situation, as shown in FIGURE 6, expanded word 61 would have the data from compressed bit ordinate position 0 expanded into ordinate positions 0, 1, 2, 3 of the expanded word. In this situation the data from compressed ordinate position 1 would be expanded into ordinate bit positions 4, 5, 6, 7, and so forth.

It can be seen from the chart in FIGURE 7 that the duplicated data at the inputs 0, 1, 2, 3 of the swizzle circuit go to outputs 0, 4, 8, 12. From FIGURE 4 it can be seen that these outputs go to VRAMS 200,201,202,203 which are the four VRAMS which would hold pixel 0 if that pixel were to be 16 bits long.

The compressed word is provided in a register such that it can be rotated through all 32 bits for any given memory clock cycle regardless of how many bits are expanded. This allows for continuous system operation without regard to pixel size. This also allows for total flexibility of memory storage to allow for starting and stopping at any given pixel boundary.

FIGURE 7 shows the input to output correspondence of swizzle circuit 32 when the swizzle circuit is in the swizzle modes It should be realized that each input has two possible outputs: the swizzle output, as shown, and the straight-through output, which is not shown. Of course, the straight-through output has input 0 connected to output 0, with input 1 connected to output 1, input 2 connected to output 2, and so forth. A switching circuit is used to switch between the straight-through arrangement of the swizzle circuit and the swizzle mode of the swizzle circuit. FIGURE s shows one embodiment of the swizzle circuit 32 where registers 0 and 1 are shown for positions 0 and 1.

As shown in FIGURE 8, the input bus has 32 leads, and the output bus also has 32 leads. Between these leads are a number of latches, two of which, 900 and 901, are shown. Each latch has a single input connected to an individual input bus lead and two outputs connected to the straight-through correspondence and to the swizzle correspondence in accordance with FIGURE 7. The latches load in a straightforward manner from information on the input bus upon the signal provided on the load lead. For the straight-through operation, a signal is provided on the REGULAR lead, and the outputs from the latches are clocked straight through the swizzle circuit with straight-through correspondence, as noted above. However, when swizzle circuit 32 is being utilized in the swizzle mode, the SWIZZLE lead is pulsed, and this serves to switch the outputs. For example, with

respect to latch 901, in the straight-through modes latch 901 is connected to lead 1 of the output bus. However, in the swizzle mode, as can be seen, another output from latch 1 is connected to lead 4 of the output bus. All of the latches of swizzle circuit 32 are wired with this correspondence such that the swizzle output lead of each latch is connected as shown in FIGURE 7 to the output bus lead. This arrangement allows for the selective control of swizzle circuit 32 in the straight-through mode or the swizzle mode, under control of the system processor.

The circuit shown in FIGURE 8 can be expanded to cover the multiple swizzles required for swizzle circuit 42. In this situation, an extra controlled output lead would extend from each latch to a different output. In this mode a second swizzle control signal would extend to control multiple outputs from each latch, the number of multiples being a function of the number of VRAMs containing the same pixel information.

While the circuit and method shown here has been described in terms of the block-write operation of a graphics processing system it can be used in numerous other situations where ordinate coordination is required for controlling physical adaptations. It should be noted that the circuitry, including the swizzle circuit and processor, could be integrated into a single chip.

While the discussion has referred to the block-write mode as it relates to VRAMs, it should be understood that the same type of memory operations could be added to memories not specifically intended to support video.

Although the present invention has been described with respect to a specific preferred embodiment thereof, various changes and modifications may be suggested by one skilled in the art, and it is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.

Claims

1. A graphic processing system comprising:
a plurality of memories for storage therein of data bits via data control leads, said memories addressable in a normal mode and in a block-write mode, said block-write mode controlled by data in a compressed data word;
multilead input and output buses, with data arriving on said input bus from an external source and presented from said leads of said input bus to said leads of said output bus;
connections between said output bus leads and said memory data control leads; and
reordering circuitry for allowing data to pass from said leads of said input bus to certain leads of said output bus when data is being presented to said memories in a normal manner and for allowing data to pass from said leads of said input bus to certain other leads of said output bus when data is being presented to said VRAM in a block-write manner from a compressed data word on said input bus.

2. The system set forth in Claim 1 wherein said reordering circuitry further includes circuitry for controlling a plurality of different input to output lead orderings.

3. The system set forth in claim 1 wherein said reordering circuitry is a multiplex circuit.

4. The system set forth in Claim 1 wherein said reordering circuitry includes a memory having a look-up table for the association of input leads to output leads.

5. The system set forth in claim 1 wherein said reordering circuitry includes circuitry for passing data from individual input leads to multiple output leads.

6. The system set forth in Claim 5 wherein said memories contain video display pixel data, and wherein said last-mentioned circuitry includes controlling a single pixel value split between more than one memory.

7. The system set forth in Claim 1 wherein said reordering circuitry is included all within a single chip.

8. A method of controlling memory access in a graphic processing system comprising:
a plurality of memories for storage therein of data bits via data control leads, said memories addressable in a normal mode and in a block-write mode, said block-write mode controlled by data in a compressed data word;
multi-lead input and output buses, with data arriving on said input bus from an external source and presented from said leads of said input bus to said leads of said output bus;
said method comprising the steps of establishing connections between said output bus leads and said memory data control leads;
passing data to said leads of said input bus to certain leads of said output bus when data is being presented to said memories in a normal manner; and
reordering data to pass from said leads of said input bus to certain other leads of said output bus when data is being presented to said VRAM in a block-write manner from a compressed data word on said input bus.

9. The method of Claim 8 wherein said reordering step further includes the step of controlling a plurality of different input to output lead orderings.

10. The method of Claim 8 wherein said reordering step includes accessing a memory having a look-up table for the association of input leads to output

leads.

11. The method of Claim 8 wherein said reordering step includes passing data from individual input leads to multiple output leads.

12. A circuit for reordering the bit positions of a compressed data word for presenting said bits of said data word to individual data paths of a data bus having b data paths thereon, said circuit comprising:

presentation circuitry for providing in sequence b bits of said compressed word, said bits for presentation to finite inputs of a series of memories, each memory having n data inputs, each input connected in sequence to said b data paths of said data bus;

such presentation being such that the ordinate positions of the first b/n data bits in said presentation circuitry are associated with a first data input of each of said n memories, and the ordinate positions of the second b/n data bits in said presentation circuitry are associated with a second data input of each of said n memories, and the ordinate positions of the third b/n data bits in said presentation circuitry are associated with a third data input of each of said n memories, and the ordinate positions of the fourth b/n data bits in said presentation circuitry are associated with a fourth data input of each of said n memories;

and wherein said circuit further comprises reordering circuitry for rearranging said bits of said compressed word during presentation of said bits to said b data bus connections so as to effectuate said associations.

13. The circuit set forth in Claim 12, wherein said presentation can be a plurality of different associations and wherein said reordering circuitry is adapted to controllably effectuate any selected one of said associations.

14. The circuitry set forth in Claim 13, wherein said reordering circuity is a multiplex circuit.

15. The circuitry set forth in Claim 13, wherein said reordering circuit includes a memory having a look-up table.

16. The circuitry set forth in Claim 13, wherein said reordering circuit includes bus expansion circuitry.

17. A system for adjusting bit positions of certain data before presentation of said data to a memory bank having a plurality of individual units of memory connectable together to form a bank, said data arriving on an input bus such that the ordinate position of said data on said bus corresponds on a one for one basis with said memory banks, and wherein said memory units are each connectable to a data bus in a prescribed manner, from the lowest to the highest regardless of the number of units forming a bank, said system comprising:

circuitry for reordering said bits from said ordinate position to conform to said connection of said memory units to said data bus when said memory banks comprise a single unit per bank; and

expansion circuitry operative prior to presentation to said reordering circuitry for duplicating the data from each ordinate position for each additional memory unit comprising a memory bank and adding the duplicated data to the next highest ordinate positions on said input bus.

18. The system set forth in Claim 17, wherein said expansion circuitry is operative from information received from time to time.

19. The system set forth in Claim 17, wherein a single pixel has individual bits stored in a plurality of said memory units.

20. The system set forth in Claim 17, wherein said reordering circuitry is a swizzle circuit having a plurality of inputs and a like plurality of outputs, said swizzle circuit comprising:

a like plurality of latches, each controlling one input and one or more outputs; and

circuitry for controlling which output any input is connected with at any instant of time.

21. A system for adjusting the bit position of certain data input bits to a graphics memory comprising a number of VRAMS during a block-write cycle of said graphics memory system, said block-write cycle characterized by establishing with respect to each VRAM a color register having color bits representative of a color to be written to selective pixel locations represented at address locations within said VRAM, said VRAM having a number of planes, each plane having one data input lead and where a number of said planes operate together to control one pixel, said address selection occurring as a joint selection via the normal address leads of said VRAM and a 1 or 0 data bit on said data input leads of each plane of said VRAM such that each data input lead controls a different pixel, said data input leads connected to said bus sequentially pixel by pixel;

said data input bits arriving such that the ordinate position of each said bit is operable for presentation of a 1 or 0 to said pixels in like ordinate order;

said system comprising expansion circuitry for duplicating all said data bits a number of times dependent upon the number of said VRAMS used for the control of said pixels, said expansion circuitry operating to expand said established data bits by adding said duplicated data bits in the next highest ordinate positions from the original data bits; and

logic circuitry for reordering said bits after expansion for presentation to control said block-write operation.

22. A system as set forth in Claim 21, wherein said logic circuitry is a swizzle circuit having a plurality of inputs as a like plurality of outputs, said swizzle circuit comprising:

a like plurality of latches, each controlling one input

and one or more outputs; and
circuitry for controlling which output any input is connected with at any instant of time.

23. The system set forth in claim 21, further including circuitry for determining the number of said VRAMs containing the same pixel information and for controlling said expansion circuitry in accordance with said determination.

24. The system set forth in Claim 20, wherein said expansion circuitry is arranged for controlling the expansion when said graphics memory is configured with any number of VRAMS controlling said pixels.

25. A circuit for reordering the bit positions of a compressed data word for presenting said bits of said data word to individual data leads of a data bus having b data leads thereon, said presentation being in a plurality of modes and said presentation including the presentation of b bits to said bus during any one memory write cycle, said circuit comprising:
presentation registers for holding in sequence said bits of a said compressed word for presentation to finite inputs of a series of memories, each memory having individual memory units, each unit having n data inputs, each input connected in sequence to said b data leads of said data bus;
such that in a first mode presentation the memory units function as distinct memories wherein the ordinate positions of the first b/n data bits in said presentation register are associated with a first data input of each of said memories, and the ordinate positions of the second b/n data bits in said presentation register are associated with a second data input of each of said n memories, and the ordinate position of the third b/n data bits in said presentation register are associated with a third data input of each of said memories, and the ordinate positions of the fourth b/n data bits in said presentation register are associated with a fourth data input of each of said memories;
and such that in a second mode presentation said memory units function as pairs wherein the ordinate positions of the first b/n/2 data bits in said presentation register are associated with the first data input of each of said memory pairs, and the ordinate positions of the second b/n/2 data bits in said presentation register are associated with a second data input of each of said memory pairs, and the ordinate positions of the third b/n/2 data bits in said presentation register are associated with the third data input of each of said memory pairs, and the ordinate position of the fourth b/n/2 data bits in said presentation register are associated with a fourth input of each of said memory pairs, and wherein said circuit further comprises:
expansion circuitry for duplicating in said presentation registers the data from any ordinate position of said b bit compressed data word into the next ordinate position in said register when said memories are in said second mode; and
reordering circuitry common to both said first and second modes for rearranging said bits of said word in said presentation registers during presentation of said bits to said b data bus connections so as to effectuate said associations.

26. The circuit set forth in Claim 25, wherein said circuit further includes circuitry for shifting said bits of said compressed word when said memories are in said second mode so that b bits cycle through said presentation registers.

27. An arrangement for adjusting the bit position of certain data bus input bits to a graphics VRAM during a block-write cycle of said VRAM, said block-write cycle characterized by establishing with respect to each VRAM a color register having color bits representative of a color to be written to selective ones of pixel locations represented at address locations within said VRAM, said VRAM having a number of memory units, each unit having a number of planes, each plane having one data input lead and where a number of said planes operate together to control one pixel, said address selection occurring as a joint selection via the normal address leads of said VRAM and a 1 or 0 data bit on said data input leads of each plane of said VRAM such that each data input lead controls a different pixel, said data input leads connected to said bus sequentially pixel by pixel;
circuitry for establishing data bits, the ordinate position of each said bit operable for presentation of a 1 or 0 to said pixels in like ordinate order; and
logic circuitry for reordering said established bits for controlling said block-write operation.

28. The arrangement set forth in Claim 20, wherein several of said memory units control a single pixel and wherein, for control purposes, the same ordinate position data bit is presented to each memory unit of said single pixel, and wherein said logic circuitry includes circuitry for expanding said data bits in accordance with the number of memory units containing a single pixel.

29. The arrangement set forth in Claim 21, wherein said logic circuitry is a multiplex circuit.

30. The arrangement set forth in claim 21, wherein said logic circuitry is a memory having a look-up table.

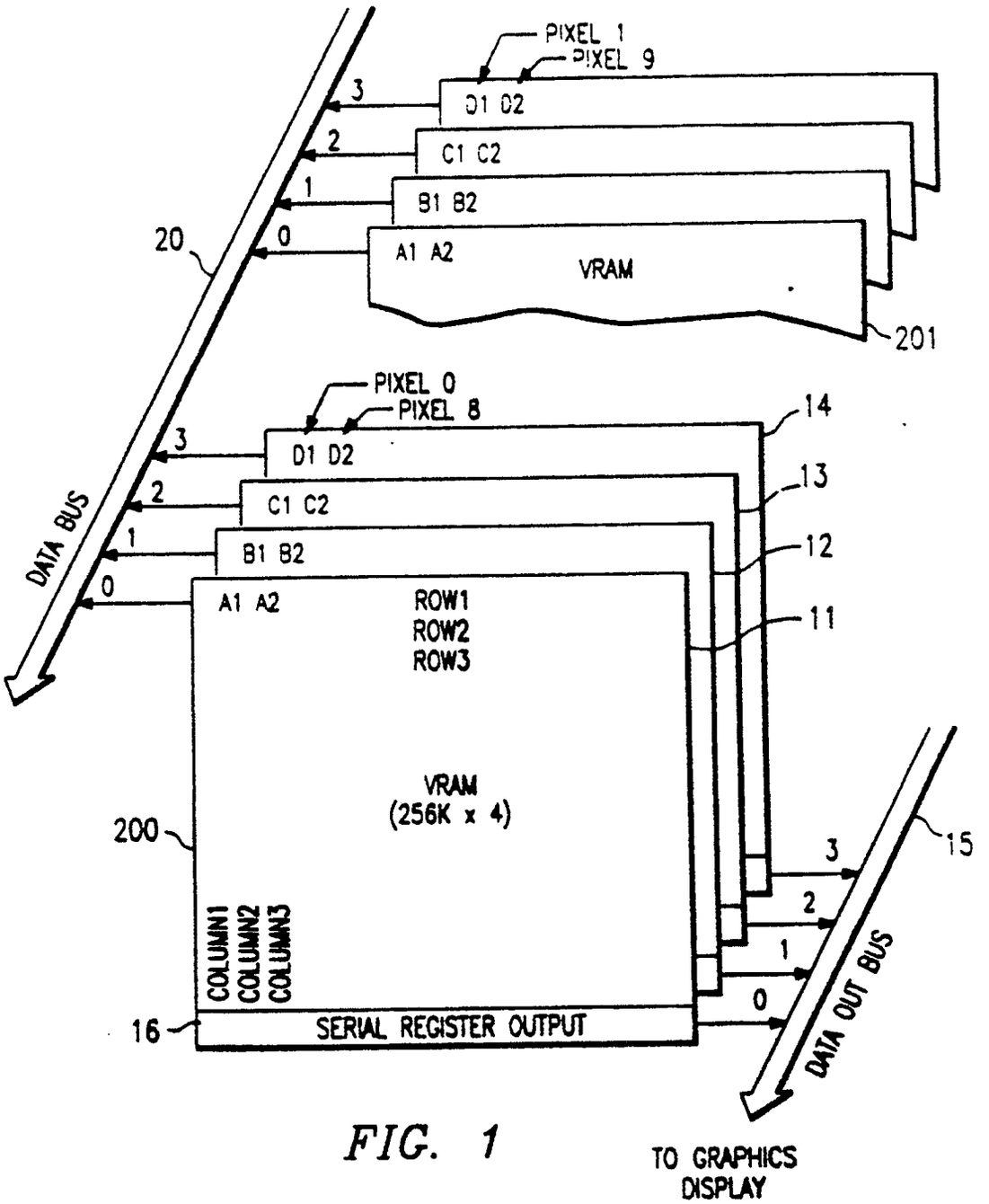

PIXEL 1
PIXEL 9
D1 D2
C1 C2
B1 B2
A1 A2
VRAM
201
20
PIXEL 0
PIXEL 8
14
13
12
11
DATA BUS
ROW1
ROW2
ROW3
VRAM
(256K x 4)
200
COLUMN1
COLUMN2
COLUMN3
16
SERIAL REGISTER OUTPUT
15
DATA OUT BUS
TO GRAPHICS
DISPLAY

FIG. 1

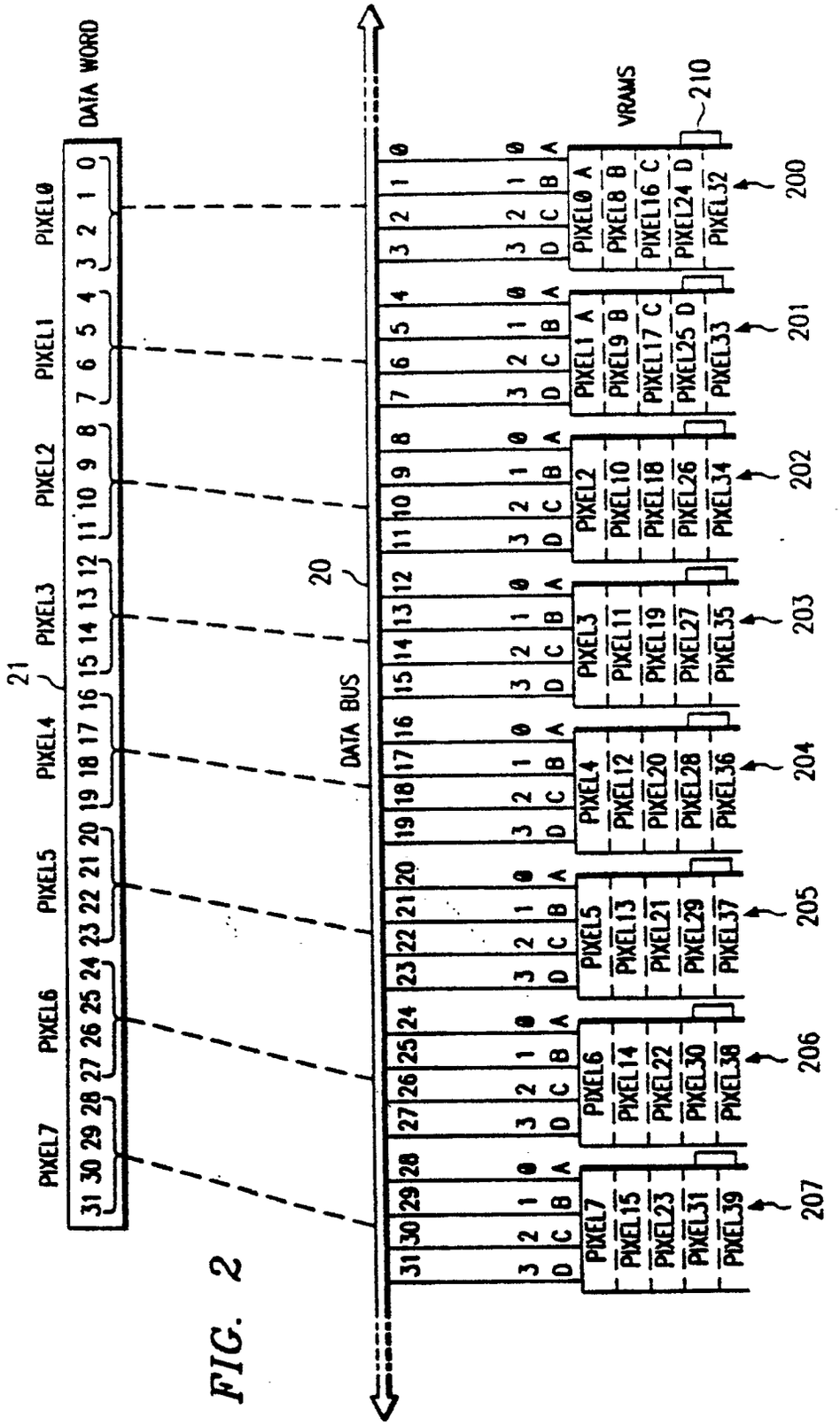

DATA WORD
PIXEL0
PIXEL1
PIXEL2
PIXEL3
PIXEL4
PIXEL5
PIXEL6
PIXEL7
21
20
DATA BUS
VRAMS
210
200
201
202
203
204
205
206
207

FIG. 2

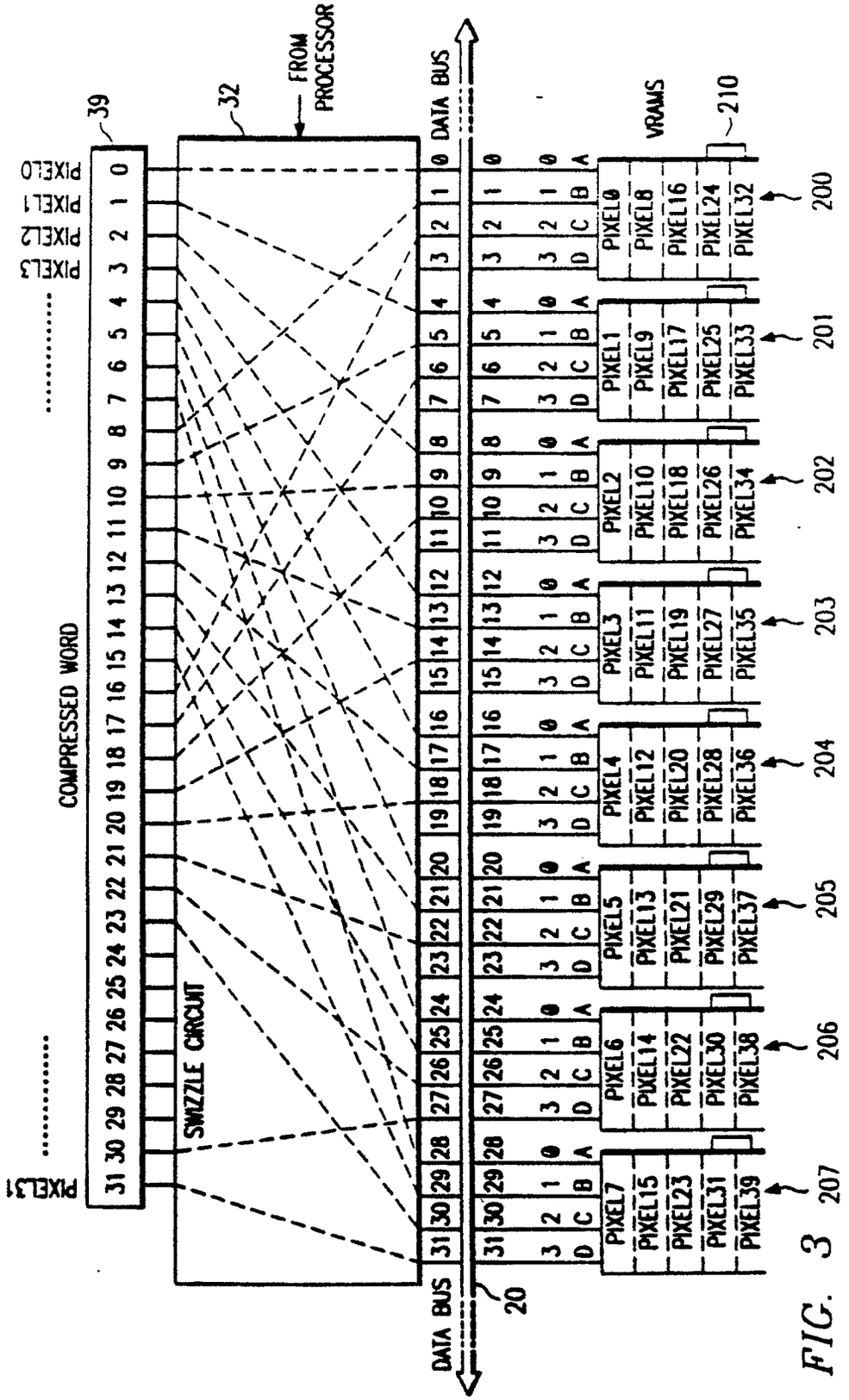

39
32
FROM PROCESSOR
DATA BUS
COMPRESSED WORD
PIXEL0
PIXEL1
PIXEL2
PIXEL3
PIXEL31
SWIZZLE CIRCUIT
VRAMS
210
20
200
201
202
203
204
205
206
207
PIXEL0
PIXEL8
PIXEL16
PIXEL24
PIXEL32
PIXEL1
PIXEL9
PIXEL17
PIXEL25
PIXEL33
PIXEL2
PIXEL10
PIXEL18
PIXEL26
PIXEL34
PIXEL3
PIXEL11
PIXEL19
PIXEL27
PIXEL35
PIXEL4
PIXEL12
PIXEL20
PIXEL28
PIXEL36
PIXEL5
PIXEL13
PIXEL21
PIXEL29
PIXEL37
PIXEL6
PIXEL14
PIXEL22
PIXEL30
PIXEL38
PIXEL7
PIXEL15
PIXEL23
PIXEL31
PIXEL39

FIG. 3

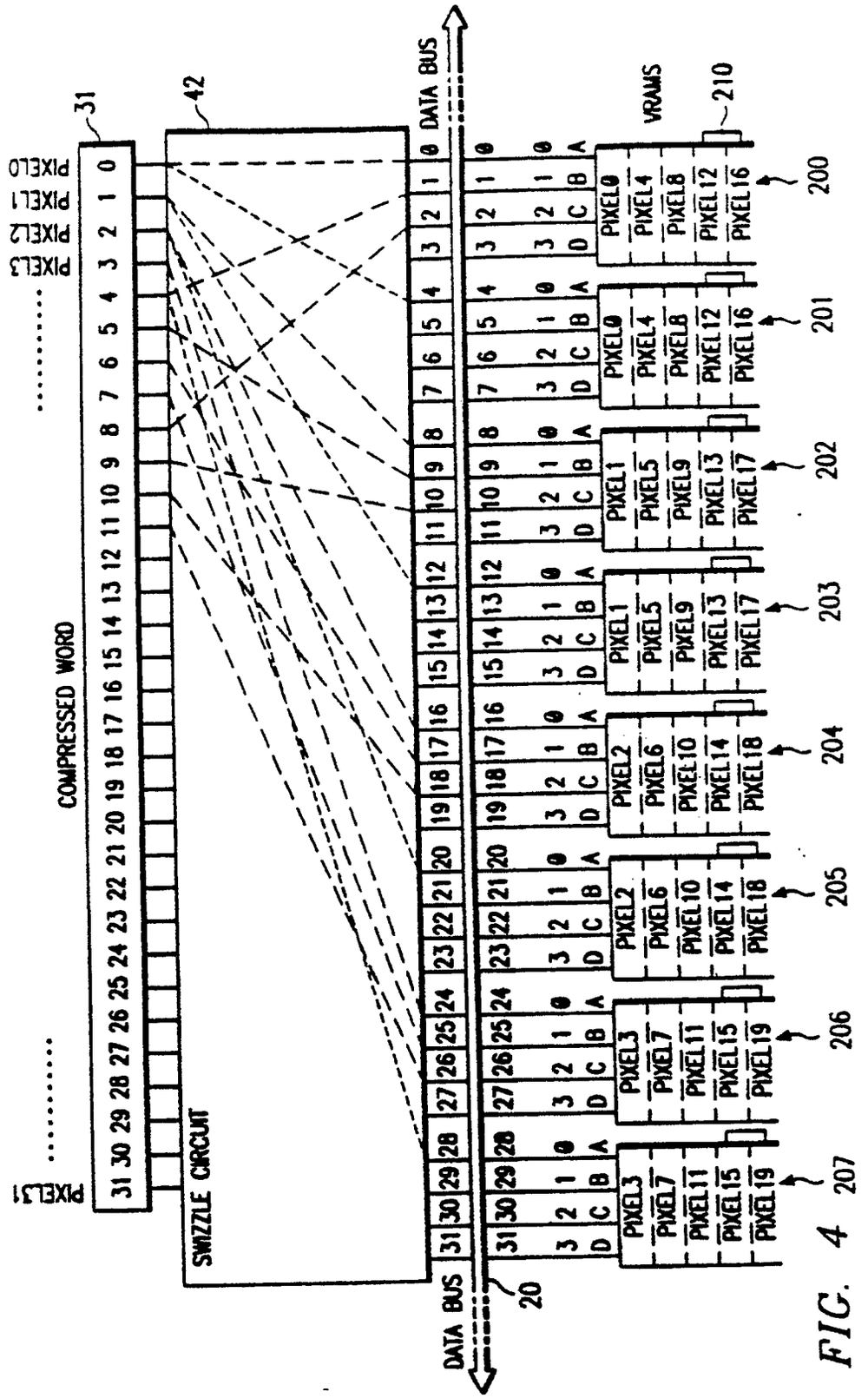

COMPRESSED WORD
31
PIXEL0
PIXEL1
PIXEL2
PIXEL3
PIXEL31
SWIZZLE CIRCUIT
42
DATA BUS
20
VRAMS
210
200
201
202
203
204
205
206
207

FIG. 4

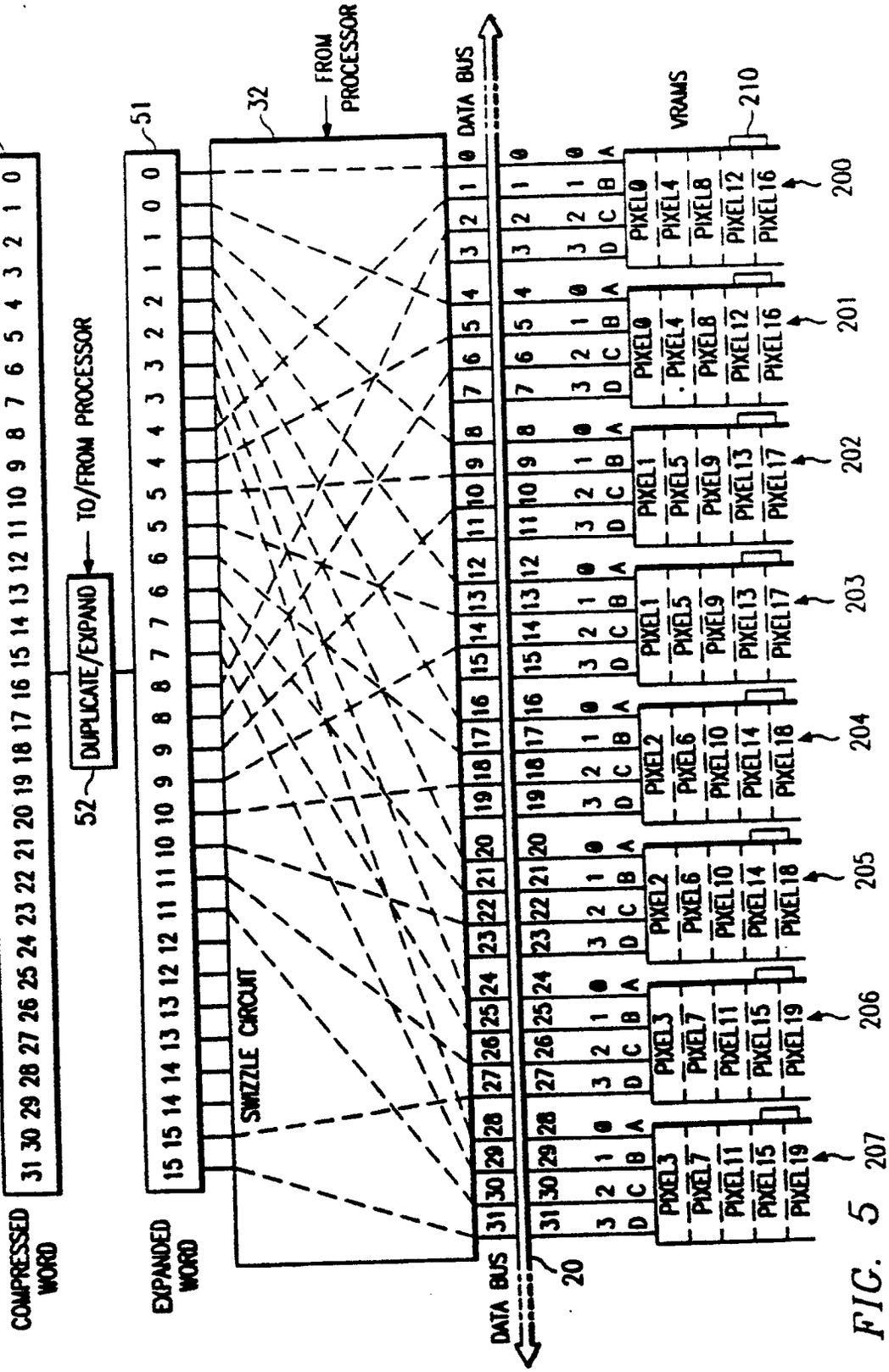
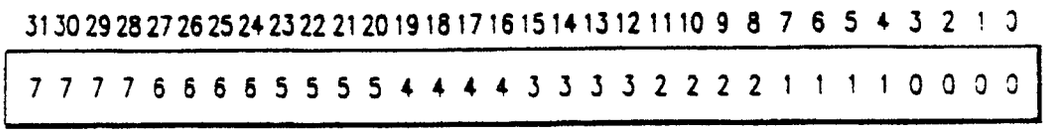

COMPRESSED WORD
31
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
52
DUPLICATE/EXPAND
TO/FROM PROCESSOR
EXPANDED WORD
51
15 15 14 13 13 12 12 11 11 10 10 9 9 8 8 7 7 6 6 5 5 4 4 3 3 2 2 1 1 0 0
SWIZZLE CIRCUIT
32
FROM PROCESSOR
DATA BUS
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
DATA BUS
20
VRAMS
210
200
201
202
203
204
205
206
207
PIXEL0 PIXEL4 PIXEL8 PIXEL12 PIXEL16
PIXEL1 PIXEL5 PIXEL9 PIXEL13 PIXEL17
PIXEL2 PIXEL6 PIXEL10 PIXEL14 PIXEL18
PIXEL3 PIXEL7 PIXEL11 PIXEL15 PIXEL19

FIG. 5

FIG. 6



SWIZZLE CORESPONDENCE

INPUT	OUTPUT
0	0
1	4
2	8
3	12
4	16
5	20
6	24
7	28
8	1
9	5
10	9
11	13
12	17
13	21
14	25
15	29
16	2
17	6
18	10
19	14
20	18
21	22
22	26
23	30
24	3
25	7
26	11
27	15
28	19
29	23
30	27
31	31

FIG. 7

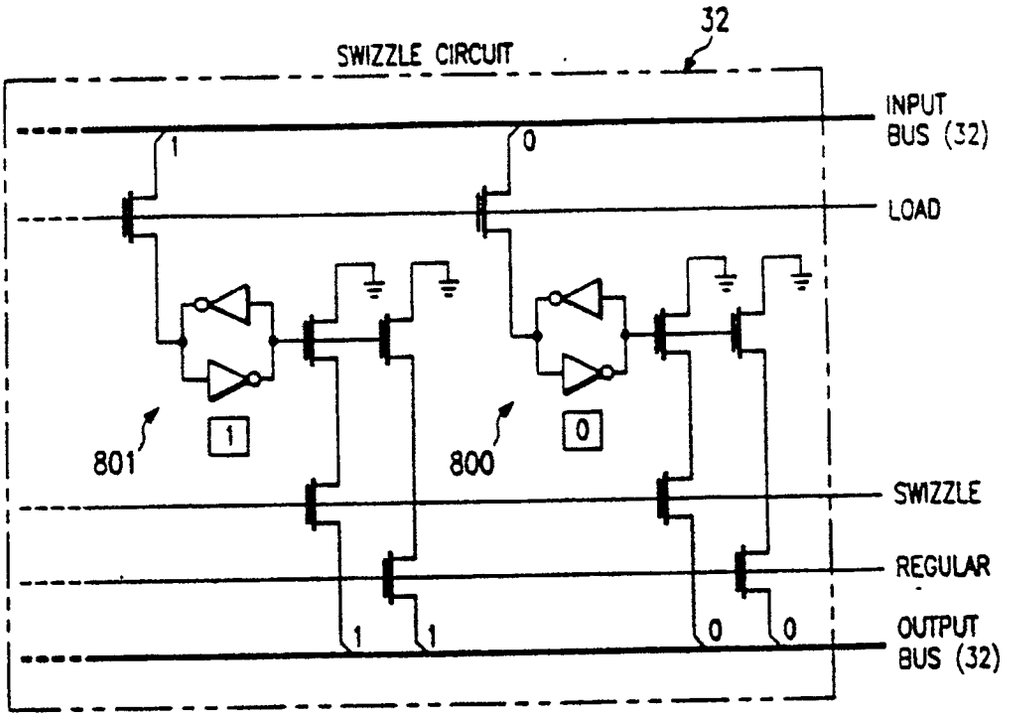

32
SWIZZLE CIRCUIT
INPUT BUS (32)
LOAD
1
0
801
800
SWIZZLE
REGULAR
OUTPUT BUS (32)

FIG. 8

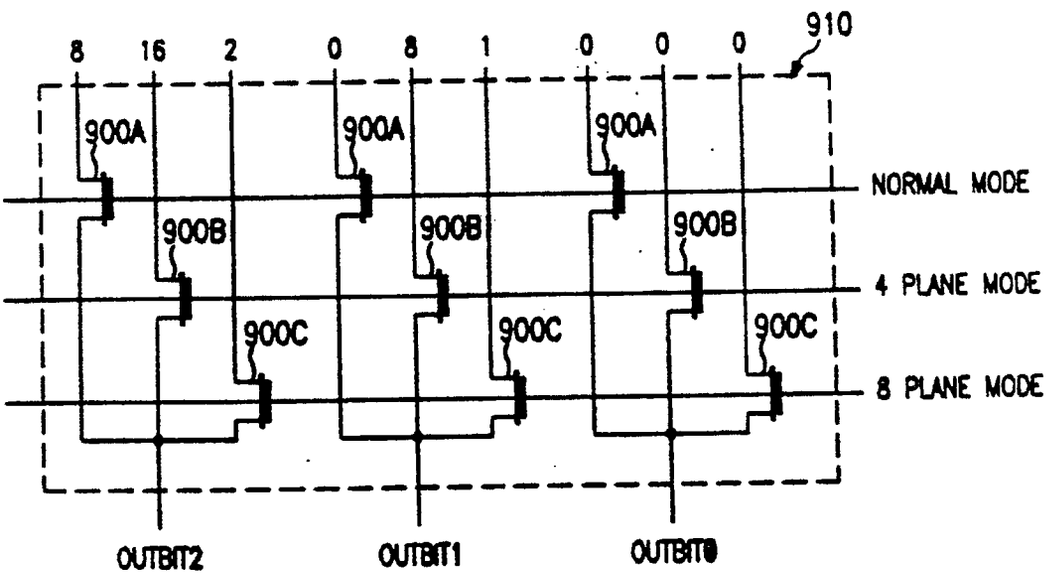

910
8 16 2 0 8 1 0 0 0
900A
900B
900C
NORMAL MODE
4 PLANE MODE
8 PLANE MODE
OUTBIT2
OUTBIT1
OUTBIT0

FIG. 9