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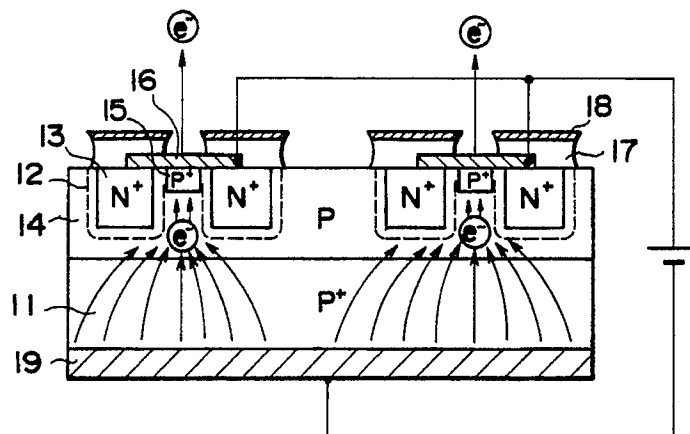
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⑤4 Electron emitting semiconductor device.

57) An electron emitting semiconductor device comprises a P-semiconductor layer formed on a semiconductive substrate; a Schottky barrier electrode formed on the P-semiconductor layer; plural P⁺-area

units positioned under and facing to the Schottky barrier electrode; and an N⁺-area in the vicinity of said P⁺-area units.

FIG. 1



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ELECTRON EMITTING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electron emitting semiconductor device.

Related Background Art

Among conventional electron emitting semiconductor devices, those utilizing avalanche amplification are disclosed for example in the U.S. Patents Nos. 4,259,678 and 4,303,930.

In such electron emitting semiconductor devices, an electron emitting part is constructed by forming a P-semiconductor layer and an N-semiconductor layer on a semiconductor substrate and reducing the work function of the surface of said N-semiconductor layer by depositing cesium or the like, and an inverse bias voltage is applied across the diode composed of said P- and N-semiconductor layers to induce avalanche amplification, whereby electrons are rendered "hot" and emitted from the electron emitting part in a direction perpendicular to the surface of the semiconductor substrate.

However, such conventional electron emitting semiconductor devices have been associated with following drawbacks, because cesium employed in the electron emitting part is chemically very active:

- (1) Extremely high vacuum (1×10^{-10} Torr or lower) is required for stable operation;
- (2) Service life and efficiency depend strongly on the level of vacuum; and
- (3) Device cannot be exposed to air.

Also in such conventional electron emitting semiconductor devices, since the electrons which have acquired strong energy by avalanche amplification reach the surface of the electron emitting part through the N-semiconductor layer, a considerable part of said energy is inevitably lost for example by lattice scattering in said N-semiconductor layer. In order to reduce such energy loss, the N-semiconductor layer has to be formed extremely thin (200 Å or less), but formation of such extremely thin N-semiconductor layer with sufficient uniformity and low defect rate is difficult, so that stable preparation of the device is therefore difficult.

SUMMARY OF THE INVENTION

The object of the present invention is to pro-

vide an electron emitting semiconductor device not associated with the drawbacks of the prior technology and capable of uniform electron emission over a wide area of arbitrary shape.

The foregoing object can be attained, according to the present invention, by an electron emitting semiconductor device comprising a P-semiconductive layer formed on a semiconductive substrate; a Schottky barrier electrode formed on said P-semiconductor layer; plurality P⁺-area units formed under said Schottky barrier electrode; and an N⁺-area formed in the vicinity of said P⁺-area units.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing the working principle of the electron emitting semiconductor device of the present invention;

Fig. 2 is a chart showing the energy bands in the vicinity of the surface of the electron emitting semiconductor device of the present invention;

Figs. 3A and 3B are schematic views of an electron emitting GaAs semiconductor device constituting a first embodiment of the present invention;

Figs. 4A and 4B are schematic views of an electron emitting GaAs semiconductor device constituting a second embodiment of the present invention;

Fig. 5 is a schematic plan view of an electron emitting semiconductor device constituting a third embodiment of the present invention;

Fig. 6 is a cross-sectional view along a line B - B in Fig. 5;

Fig. 7 is a schematic cross-sectional view of a part of an electron emitting semiconductor device constituting a fourth embodiment of the present invention; and

Fig. 8 is a schematic plan view thereof.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The electron emitting semiconductor device of the present invention, in which a Schottky electrode for a P-semiconductor layer is composed of an area doped with a material for reducing the work function of the surface of the electron emitting part (said material being hereinafter called work function reducing material), can form the electron emitting part in the direction of cross section of the substrate, and can also have plural electron emitting parts of arbitrary shapes in a single device.

Also since the work function reducing material employed in the present invention is an element extremely stable in the air, the device of the present invention does not require an ultra high vacuum for stable operation, does not show strong dependence of service life and efficiency on the level of vacuum, and can even be exposed to the air. Conventional electron emitting semiconductor devices show a large energy loss in the N-semiconductor layer because of the use of PN junction, so that the material of an extremely low work function has to be used. In practice, therefore, cesium alone has been used for this purpose. On the other hand, the device of the present invention shows a smaller energy loss than in the conventional devices because of the use of a Schottky junction, so that the usable work function reducing materials include metals of groups IA, IIA and IIIA of the periodic table and of lanthanoid, and silicides, borides and carbides of such metals. More specific examples of said material include TiC, ZrC, HfC, LaB₆, SmB₆, GdB₆, WSi₂, TiSi₂, ZrSi₂ and GdSi₂.

Besides, different from the conventional electron emitting semiconductor devices, the electrons which have acquired high energy by avalanche amplification need not go through the N-semiconductor layer for reaching the surface of the electron emitting part. Consequently the device of the present invention is not associated with the difficulty in manufacture such as the necessity of forming an extremely thin N-semiconductor layer, for example 200 Å or less, and can therefore be manufactured in stable manner.

In the following the present invention will be clarified in greater detail, with reference to Figs. 1 and 2.

Fig. 1 is a schematic view of an example of the electron emitting semiconductor device of the present invention, showing the working principle thereof. In Fig. 1, there are shown a semiconductive substrate 11; a depletion layer area 12; an n⁺ area 13; a p-semiconductor layer 14; a p⁺ area unit 15; a Schottky electrode 16; an n-ohmic electrode 18; and p-ohmic electrode.

The semiconductor material to be employed in the electron emitting device of the present invention can for example be Si, Ge, GaAs, GaP, AlAs, GaAsP, AlGaAs, SiC or BP, but any material that can form p-semiconductor can be used for this purpose, and particularly preferred is a material of indirect transition type with a large band gap.

Fig. 2 shows the energy bands in the vicinity of the surface of the electron emitting semiconductor device of the present invention.

In the following there will be explained the electron emitting process of the electron emitting semiconductor device of the present invention.

Under the application of an inverse bias voltage to a Schottky diode consisting of the p-semiconductor and the work function reducing material, the bottom Ec of the conduction band of the p-semiconductor assumes an energy level higher than the vacuum level E_{vac} of the Schottky electrode. Electrons generated by the avalanche amplification acquire an energy higher than the lattice temperature by an electric field in the depletion layer generated at the interface of the semiconductor and the metal electrode, and are injected into the Schottky electrode consisting of the work function reducing material. Thus said electrons, of which energy is not lost for example by lattice scattering and is therefore higher than the work function of the surface of the Schottky electrode, are emitted into the outer vacuum space from the surface of said Schottky electrode constituting the electron emitting part.

In the electron emitting semiconductor device of the present invention, because of the presence of an n⁺ area in the vicinity of the interface of the work function reducing material in the P-semiconductor substrate, there is generated a depletion layer at the P-N⁺ interface. Consequently the electrons injected from the P⁺-layer into the P-layer are restricted in their moving path by said depletion layer at the P-N⁺ interface and are concentrated in a p⁺-area unit provided in the electron emitting part, whereby the current density can be easily increased.

Also in the device of the present invention, since the P⁺-area unit and the N⁺-area constituting the electron emitting part can be formed for example by ion implantation from the surface of the semiconductor substrate in the device manufacturing process, there can be formed plural electron emitting parts of arbitrary shapes, at arbitrary positions on a same plane of a substrate.

Also as desired semiconductive layers can be deposited in succession for example by MBE (molecular beam epitaxy) on a semiconductive substrate, the electron emitting part can be constructed with such successively deposited layer. It is therefore possible to form plural electron emitting parts in a direction perpendicular to the surface of the substrate.

Furthermore, according to the present invention, the plural P⁺-area units may be arbitrarily positioned in the P-semiconductor layer, so that an electron beam of an arbitrary shape can be obtained.

[1st embodiment]

Fig. 3A is a plan view and Fig. 3B is a cross-sectional view along a line A - A in Fig. 3A, both schematically showing an electron emitting GaAs

semiconductor device constituting an embodiment of the present invention, wherein shown are a P⁺-Si substrate 101; a P⁻-layer 102; an annular N⁺-area 103; a point-shaped P⁺-area unit 104; an insulating film 105; ohmic electrodes 106, 107; and a Shottky electrode 108.

In the following there will be explained the method of producing the electron emitting semiconductor device shown in Figs. 3A and 3B.

- (1) On a P⁺-Si substrate 101 doped with As with an impurity concentration of $1 \times 10^{19} \text{ cm}^{-3}$, a P⁻-layer 102 with an As concentration of 3×10^{18} was formed by CVD (chemical vapor deposition) or LPE (liquid phase epitaxy).
- (2) Then apertures for the areas 103, 104 were formed by an ordinary photolithographic process, and ion implantations were conducted with B⁺ ions for the annular N⁺-area 103 to obtain an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$, and with As⁺ ions for the point-shaped P⁺-area units 104 to obtain an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$, and activation was conducted by annealing.
- (3) Then a SiO₂ insulating film 105 was formed by vacuum evaporation, and an aperture was formed therein by a photolithographic process.
- (4) Aluminum was vacuum evaporated on the annular N⁺-area 103 and on the rear surface of the substrate to form ohmic electrodes 106, 107.
- (5) Then, as the material constituting the Shottky electrode 108, a work function reducing material Ga ($\phi_{wk} = 3.1 \text{ eV}$) was deposited by vacuum evaporation in a thickness of 100 Å. Then, a heat treatment for 10 minutes at 350 °C was conducted to form GaSi₂, forming a satisfactory Shottky junctions with the point-shaped P⁺-area units 104.

In the electron emitting semiconductor device prepared as explained above, the application of an inverse bias voltage to the Shottky barrier diode 108 induced avalanche amplification at the interface between the Shottky electrode 108 and the point-shaped P⁺-area 104, whereby electrons of high energy were emitted from the GaSi surface.

As explained in the foregoing, in the present embodiment, the presence of the P⁺-area unit for concentrating the electric field and limiting the electron emitting part limits the point of electron emission, so that the distribution of electron emission in a device can be arbitrarily designed by the arrangement of said point-shaped P-area and the size of the P⁺-area unit.

Besides the electron emitting device of the present invention easily allows minituarization or integration of multiple devices because the conventional semiconductor process can be utilized for the preparation.

[2nd embodiment]

Fig. 4A is a plan view, and Fig. 4B is a cross-sectional view along a line A - A in Fig. 4A, both showing an electron emitting GaAs semiconductor device constituting a second embodiment of the present invention, wherein shown are a P⁺-Si substrate 401; a P⁻-layer 402; an annular N⁺-area 403; a point-shaped P⁺-area unit 404; an insulating film 405; ohmic electrodes 406, 407; and a Shottky electrode 408.

In the following there will be explained the method for producing the electron-emitting semiconductor device shown in Fig. 4.

- (1) On a P⁺-GaAs substrate 401 with an impurity concentration of $5 \times 10^{18} \text{ cm}^{-3}$, there was epitaxially grown a P⁻-GaAs layer 402 with an impurity concentration of $1 \times 10^{18} \text{ cm}^{-3}$ by MEB (molecular beam epitaxy) or MO-CVD (metalorganic chemical vapor deposition), employing Be as the P-impurity.
- (2) Maskless ion implantation was conducted with FIB (focused ion beam), employing Si²⁺ for the annular N⁺-area 403 with an accelerating voltage of 160 keV and Be⁺ for the point-shaped P⁺-area unit 404 with an accelerating voltage of 40 keV.
- (3) Subsequently SiO₂ was deposited by vacuum evaporation on both faces of the substrate 401, and the implanted impurities were activated by annealing for 3 minutes at 850 °C.
- (4) Then SiO₂ was entirely removed from the rear face of the substrate, and the interior alone of the annular N⁺-area on the top face was etched to obtain the insulating film 405.
- (5) Then Au-Zn alloy and Au-Ge alloy were deposited by vacuum evaporation respectively on the rear face of the P⁺-substrate 401 and on the n⁺-area of P⁻-GaAs layer 402. After the Au-Ge alloy film on the top face was patterned, heat treatment was applied for 3 minutes at 400 °C to obtain the ohmic electrodes 406, 407.
- (6) Finally LaB₆, which is a work function reducing material ($\phi_{WT} = 2.6 \text{ eV}$) capable of forming satisfactory Shottky junction to the positive holes of GaAs, was deposited by electron beam evaporation, thereby forming the shottky electrode.

The electron emitting semiconductor device prepared in this manner was placed in a vacuum chamber maintained at 2×10^{-7} Torr, and was given an inverse bias voltage of 7 V, whereupon electron emission of about 1 nA was observed.

[3rd embodiment]

Fig. 5 is a plan view, and Fig. 6 is a cross-

sectional view along a line B - B in Fig. 5, both showing an electron emitting semiconductor device constituting a third embodiment of the present invention.

In the following there will be explained the method for producing the device shown in Figs. 5 and 6.

(1) On an insulating Si substrate 511, there were grown a P⁺-layer 513 of an impurity concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and a P-semiconductor layer 504 of an impurity concentration of $3 \times 10^{16} \text{ cm}^{-3}$ by CVD (chemical vapor deposition) or LPD (liquid phase epitaxy).

(2) Then apertures for the areas 503, 505, 512 were formed by an ordinary photolithographic process, and As⁺ ions were implanted with an impurity concentration of $1 \times 10^{20} \text{ cm}^{-3}$ in the P⁺-area units 505, 512 and were activated by annealing.

(3) Subsequently a work function reducing material constituting the Schottky electrode 506, for example Gd ($\phi_{\text{WK}} = 3.1 \text{ eV}$), was deposited in a thickness of 100 Å by vacuum evaporation, and a satisfactory Schottky junction was formed by heat treatment for 10 minutes at 350 °C.

(4) Then, the electrode 508 and ohmic electrode 509 were formed by aluminum evaporation on an insulating layer on said Schottky electrode 506.

In the electron emitting semiconductor device prepared as explained above, the application of an inverse bias voltage to the Schottky diode induced avalanche amplification at the interface between the Schottky electrode 506 and the P⁺-area unit 505, whereby electrons of high energy were emitted from the GdSi₂ surface.

As explained in the foregoing, the present embodiment has a line-shaped P⁺-area unit 505 for concentrating the electric field and limiting the electron emitting part as shown in Fig. 5, so that the electron emission can be obtained continuously over a wide area. Consequently it can be utilized as the electron source for flat panel displays or other display devices in which a linear cathode has been employed.

Also the electron emitting semiconductor device of the present embodiment can be made as a large device or in a large area, because it is a silicon device utilizing the conventional semiconductor process.

[4th embodiment]

In the following there will be explained a fourth embodiment of the present invention, in which the electron emitting semiconductor device of the present invention is applied in a 7-segment image

display device, with reference to Figs. 7 and 8.

Fig. 7 is a schematic cross-sectional view of a part of the electron emitting semiconductor device of the present embodiment, and Fig. 8 is a schematic plan view thereof.

In the following there will be explained the method for producing said device shown in Figs. 7 and 8.

(1) On a P⁺-GaAs substrate 701 of an impurity concentration of $5 \times 10^{18} \text{ cm}^{-3}$, there was epitaxially grown a P-GaAs layer 704 of an impurity concentration of $1 \times 10^{16} \text{ cm}^{-3}$ by MBE (molecular beam epitaxy) utilizing Be as the P-impurity.

(2) Then an N⁺-layer 703 was formed by maskless ion implantation with an FIB (focused ion beam) of Si⁺ into the P-GaAs layer 704 with an accelerating voltage of 80 keV and a dose of about $5 \times 10^{13} \text{ cm}^{-2}$.

(3) Then P⁺-area units 705 constituting electron emitting areas were formed by ion implantation with an FIB of an accelerating voltage of 50 kV and a dose of about $1 \times 10^{13} \text{ cm}^{-3}$.

Said P⁺-area units 705 constitute seven electron emitting areas for displaying the 7-segment image.

(4) Then a SiO₂ layer was formed by sputter evaporation on the substrate 701 having the N⁺-area 703 and the P⁺-area units 705 thereon, and heat treatment for 3 minutes at 800 °C was applied in mixed gas of arsine, N₂ and H₂ to activate the implanted impurities.

(5) Then SiO₂ on the P⁺-area units 705 was removed to expose said area units, and LaB₆ ($\phi_{\text{WT}} = 2.6 \text{ eV}$) which is a work function reducing material capable of forming a satisfactory Schottky junction to the positive holes of GaAs was deposited in a thickness of about 200 Å by electron beam evaporation, thereby forming a Schottky electrode independently for each segment.

(6) Finally an ohmic electrode was formed on the rear face of the P⁺-substrate with Au-Zn alloy whereby the electron emitting device was completed.

The electron emitting semiconductor device thus completed was placed in a vacuum container maintained at 1×10^{-6} Torr, and a fluorescent plate was placed at a distance of 2 mm. By the electron emission from the device, there were observed luminous points corresponding to seven segments of said device. The electron emission was obtained only from segments in which the Schottky electrode was given a positive voltage, so that the display of numerals was possible by the combinations of seven segments.

As explained in the foregoing, the electron emitting device of the present invention is capable

of arbitrarily limiting the electron emitting part, and simultaneously forming plural electron emitting parts on a same substrate.

Furthermore, the electron emitting device of the present invention is capable of electron emission in a direction perpendicular to the cross section of the substrate, and is also capable of electron emissions in plural independent directions by forming the electron emitting cross sections in plural directions.

Also said device can be easily applied for example to a display, since the shape of the electron emitting part can be controlled by the P^+ -layer embedded in the P-layer.

An electron emitting semiconductor device comprises a P-semiconductor layer formed on a semiconductive substrate; a Schottky barrier electrode formed on the P-semiconductor layer; plural P^+ -area units positioned under and facing to the Schottky barrier electrode; and an N^+ -area in the vicinity of said P^+ -area units.

Claims

1. An electron emitting semiconductor device comprising a P-semiconductor layer formed on a semiconductive substrate; a Schottky barrier electrode formed on said P-semiconductor layer; plural P^+ -area units positioned under and facing to said Schottky barrier electrode; and an N^+ -area in the vicinity of said P^+ -area units.
2. An electron emitting semiconductor device according to claim 1, wherein said Schottky barrier electrode is composed of at least a material selected from Gd, LaB_6 , TiC, ZrC, HfC, SmB_6 , Gd_2B_6 , WSi_2 , $TiSi_2$, $ZrSi_2$ and $GdSi_2$.
3. An electron emitting semiconductor device according to claim 1, wherein said P-semiconductor is composed of at least a material selected from Si, Ge, GaAs, GaP, AlAs, GaAsP, AlGaAs, SiC and BP.
4. An electron emitting semiconductor device according to claim 1, wherein said Schottky barrier electrode has a thickness not exceeding 20 nm.
5. An electron emitting semiconductor device according to claim 4, wherein said Schottky barrier electrode has a thickness in a range from 5 nm to 15 nm.
6. An electron emitting semiconductor device according to claim 1, wherein said P^+ -area unit has an area not exceeding $8000 \mu m^2$.
7. An electron emitting semiconductor device according to claim 6, wherein said P^+ -area unit has an area in a range from 1000 to $6000 \mu m^2$.
8. An electron emitting semiconductor device according to claim 1, wherein said N^+ -area is formed in an annular form surrounding said P^+ -area unit.
9. An electron emitting semiconductor device hav-

ing a P-semiconductor layer formed on a semiconductor substrate, a Schottky barrier electrode on said P-semiconductor, and a P^+ -area unit under said Schottky barrier electrode, wherein said P^+ -area unit is stripe shaped.

10. An electron emitting semiconductor device according to claim 9, comprising plural N^+ -areas formed across said P^+ -area unit so as not to be in contact with said P^+ -area unit.

11. An electron emitting semiconductor device according to claim 9, wherein said Schottky barrier electrode is composed of at least a material selected from Gd, LaB_6 , TiC, ZrC, HfC, SmB_6 , Gd_2B_6 , WSi_2 , $TiSi_2$, $ZrSi_2$ and $GdSi_2$.

12. An electron emitting semiconductor device according to claim 9, wherein said P-semiconductor is composed of at least a material selected from Si, Ge, GaAs, GaP, AlAs, GaAsP, AlGaAs, SiC and BP.

13. An electron emitting semiconductor device according to claim 9, wherein said Schottky barrier electrode has a thickness not exceeding 20 nm.

14. An electron emitting semiconductor device according to claim 13, wherein said Schottky barrier electrode has a thickness within a range from 5 nm to 15 nm.

15. An electron emitting semiconductor device according to claim 9, wherein said P^+ -area unit has an area not exceeding $8000 \mu m^2$.

16. An electron emitting semiconductor device according to claim 15, wherein said P^+ -area unit has an area within a range from 1000 to $6000 \mu m^2$.

FIG.1

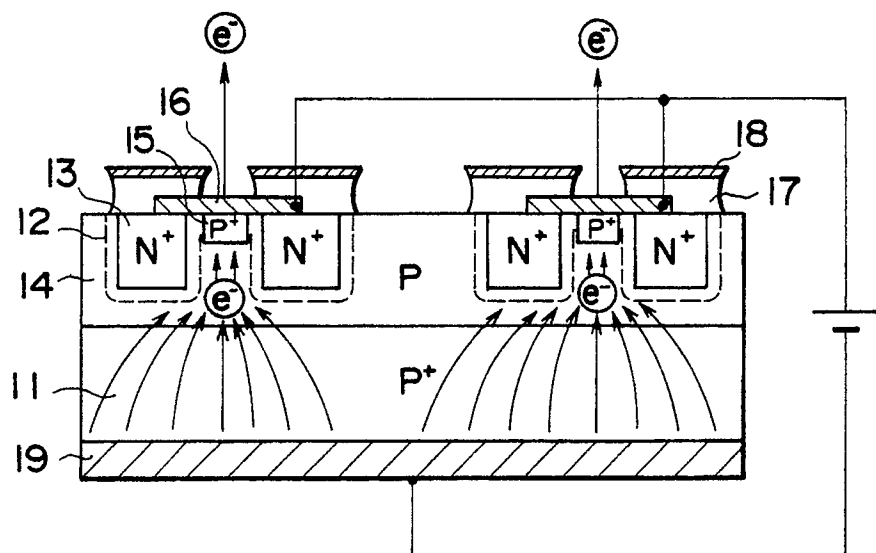


FIG.2

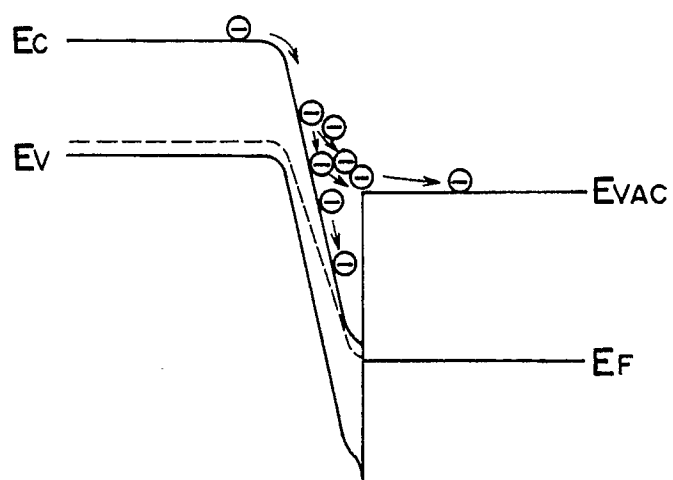


FIG. 3A

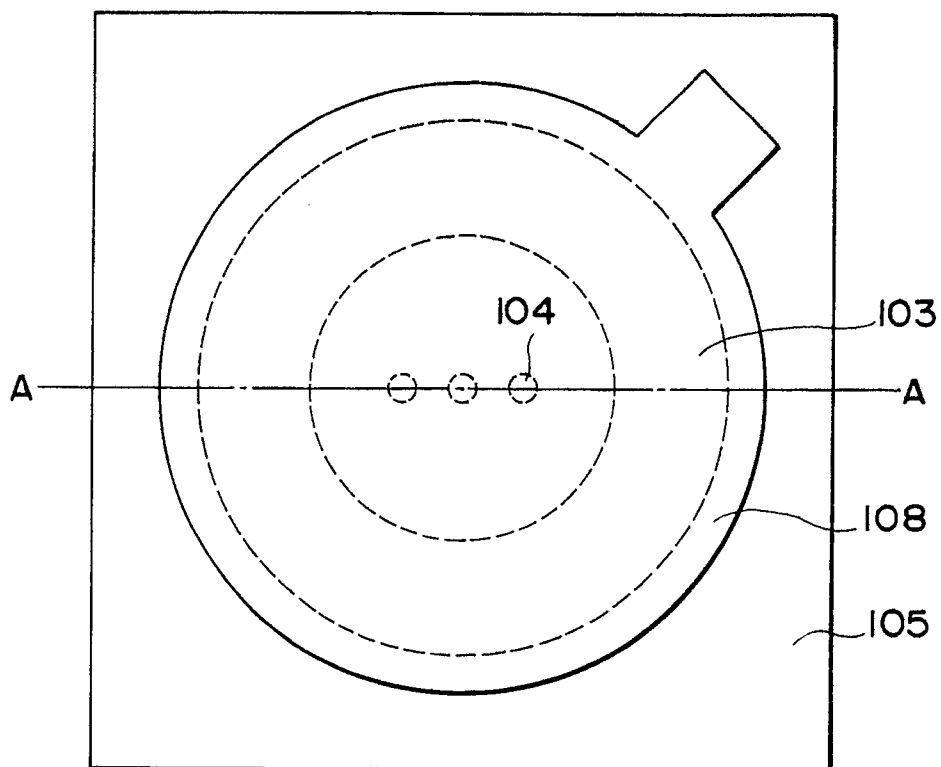


FIG. 3B

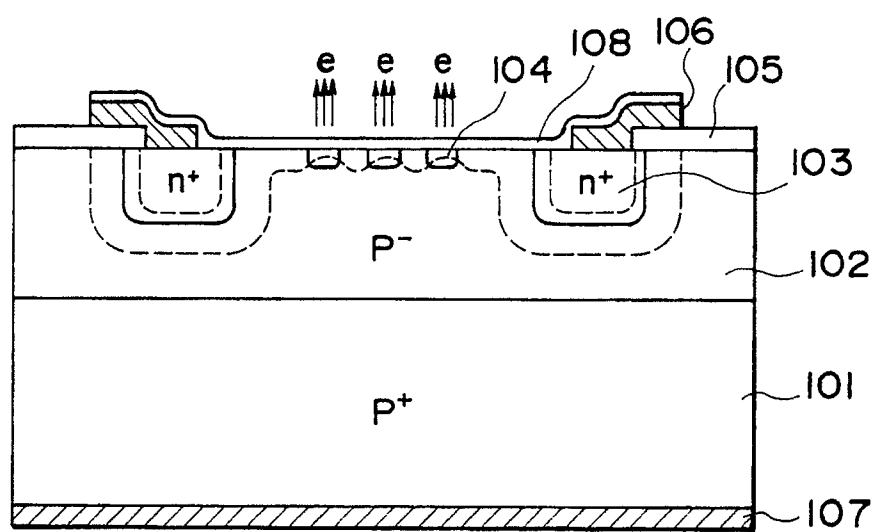


FIG. 4 A

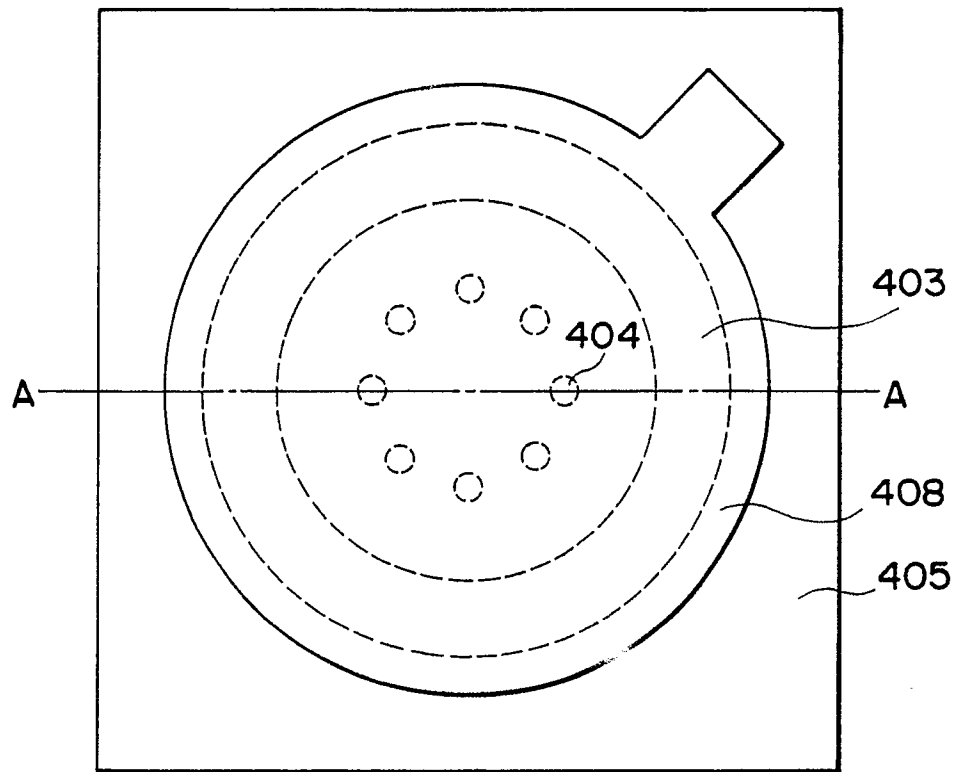


FIG. 4 B

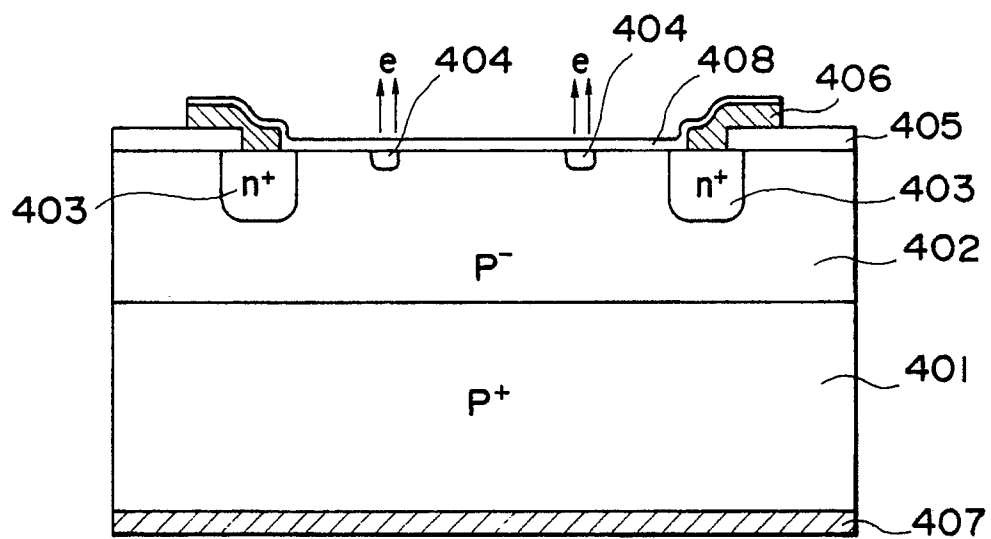


FIG.5

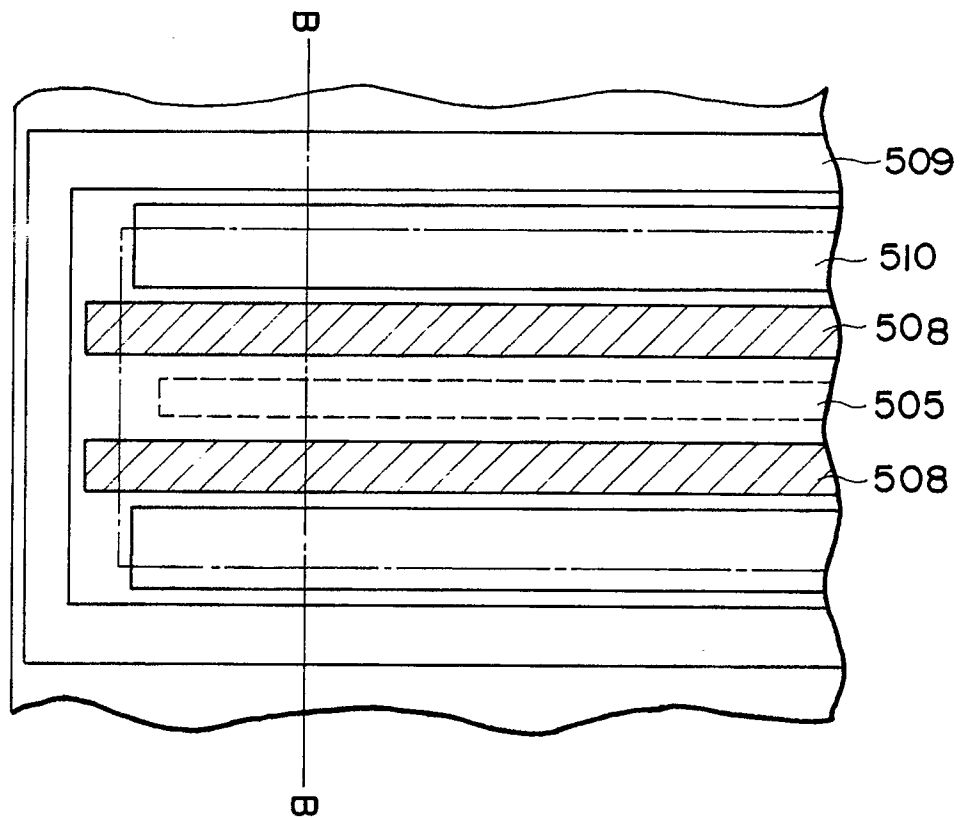


FIG. 6

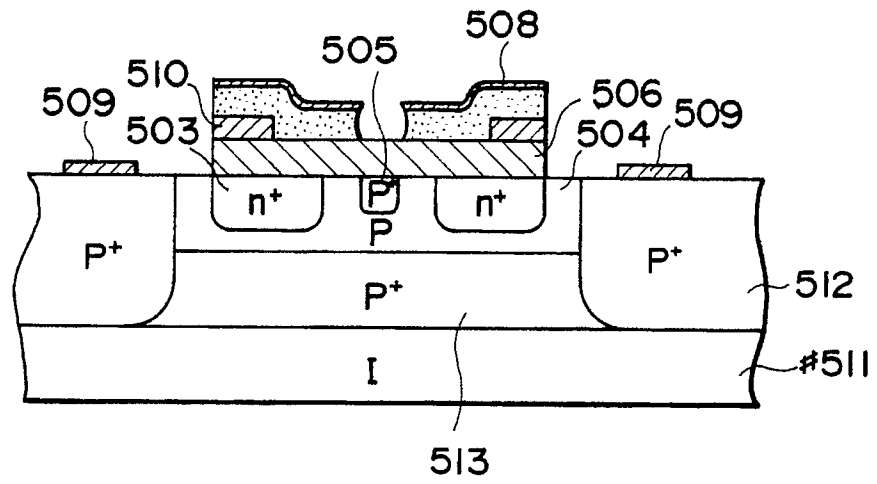


FIG. 7

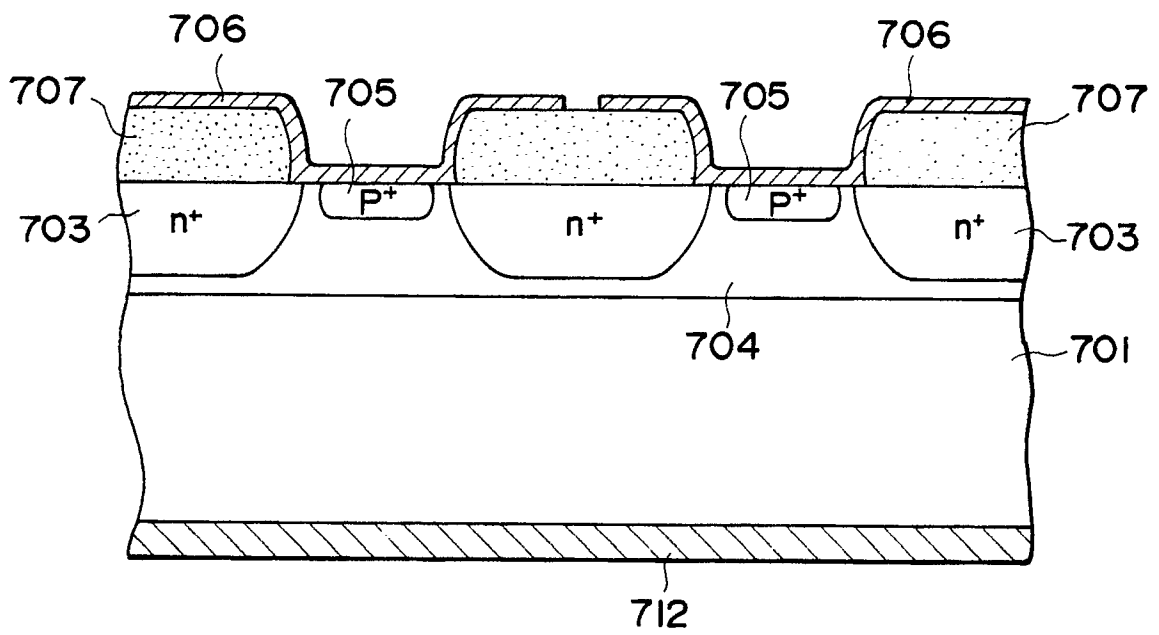


FIG. 8

