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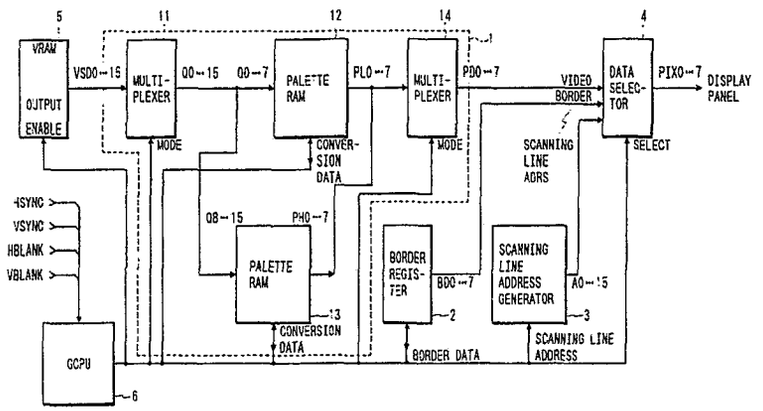
(54) Display apparatus.

(57) There is provided a display apparatus which uses a display panel using a liquid crystal having a bistability or a memory performance such as a ferroelectric liquid crystal and can display image data in various display modes in which the number of pixels (resolution), display color, minimum pixel unit, and the like respectively differ. The display apparatus comprises: a memory to store the image data; a pixel data output circuit to output the image data stored in the memory every pixel data; a converter to convert the pixel data which was output from the pixel data output circuit into binary data which is displayed on the display panel; a display data output circuit for converting the binary data converted by the converter into the display data corresponding to the display modc and outputting; and a display controller for allowing the image data which was output by the display data output circuit to be displayed on the display panel. A multiplexer is used as a pixel data output circuit. An RAM in which binary data has been stored is used as a converter.

FIG. 1



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DISPLAY APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a display apparatus and, more particularly, to an output circuit of image information which is suitable for application to a display apparatus using a binary display element such as a ferroelectric liquid crystal display element or the like having a bistability (memory performance) for an electric field.

Related Background Art

Recently, in displays of personal computers, work stations, and the like, realization of a large display screen and a high resolution is rapidly being progressed. Many display modes including the conventional display modes exist. When explaining an example of a graphics environment of a personal computer made of IBM (trade name: International Business Machines Corporation) which is generally frequently used, there are ten and a few kinds of display modes such as CGA (Color Graphic Adapter), EGA (Enhanced Graphic Adapter), VGA (Video Graphic Adapter), and the like. The resolutions and the numbers of colors which can be displayed in those display modes are different, respectively.

Fig. 10 shows a list of the above modes.

(1) With respect to the display color:

As will be understood from Fig. 10, the number of constructing bits per pixel (bits/pixel) differs every display mode and a storage format in an image memory (VRAM) also differs. Apparently, in the mode in which the number of constructing bits per pixel is large, the multi-color display can be executed.

Explanation will now be made as an example with respect to the display mode 13(h) (VGA) which can perform the highest multi-color display in the graphics environment of the personal computer made by IBM Corporation. An output flow of color information is as follows. First, when a certain address in a VRAM is accessed, the image data (bits/pixel: mode 13(h)) in a VRAM functions as an address to select a color register in a color palette in which color information has previously been stored. In the case of the VGA, the color palette has 256 color registers of 18 bits (6 bits for each of R, G, and B). The color information has been stored in the color registers. When one of the 256 color registers is selected by image data from the VRAM, the color data of R, G, and B each comprising six bits are read out and are led to D/A converters in the same color palette. One D/A converter is provided for each of R, G, and B and converts the 6-bit color data into the analog signal and sends to a display (CRT).

The output method of the color information (color palette + analog output) as mentioned above has advantages such that: the multi-color display can be realized although a data amount of the VRAM is not so large; the color on the display screen can be changed by rewriting the data of the color registers without needing to rewrite the data in the VRAM; the number of lines connected to the display can be reduced; and the like. Therefore, the above method is mainly a standard method in the present personal computers.

(2) With respect to the resolution:

In Fig. 10, the resolution also differs every display mode. For instance, the resolution is set to 320 x 200 pixels (picture elements) in the case of the mode D(h) and is set to 640 x 480 pixels in the case of the mode 12(h). Such a method whereby all of a number of kinds of display modes are supported by one display (CRT) is hitherto considered to be relatively difficult. In general, the display modes which can display are restricted (limited). On the other hand, in partial CRTs of the automatic tracking type or the like called "multiscan" and "multisync", a method whereby the scanning frequency of an electron beam is switched in accordance with each display mode is used to support the display modes in a relatively wide range. Therefore, if the display is executed in a display mode of small amount of display information (low resolution), the number of characters or numerals which are displayed as rough images is large.

Different from the case of displaying by the CRT or the like, the following points must be considered in the case where various kinds of display modes of different display colors and resolutions are applied to a display apparatus using a liquid crystal such as a ferroelectric liquid crystal or the like having the memory performance and color information is displayed.

(1) With respect to the display color:

In the case of a display apparatus using a binary display element represented by a ferroelectric liquid crystal display apparatus or the like, it is difficult to express gradations (in the depth direction) in an analogwise manner in one pixel (picture element) like a CRT or the like, that is, to three-dimensionally execute a gradation display. In the case of executing the gradation display by the binary display element, in general, a process such that the gradation (color) data in the depth direction is developed in the lateral direction (extending direction) is executed and the color information is two-dimensionally displayed (area gradation). Therefore, in the case where color information is displayed by the ferroelectric liquid crystal display apparatus or the like in various display modes of different display colors, the gradation (color) data in the depth direction which is inherently used for the CRT must be converted into the gradation data in the lateral direction (extending direction) in accordance with the arrangement of the pixels of the actual display apparatus in accordance with the display mode.

(2) With respect to the resolution:

In the case where the display is executed in various display modes which have conventionally been used in the CRT or the like by using a display apparatus such as a ferroelectric liquid crystal display apparatus or the like of a high resolution (1000 x 1000 pixels or more), the redundant pixels (the pixels remain) occur on the side of the liquid crystal display apparatus because the resolution in the CRT display mode is lower (an amount of display information is smaller) than the effective number of pixels (resolution) of the liquid crystal display apparatus. In such a case, the enlarged display can be also executed by simultaneously driving a plurality of electrodes in the vertical and lateral directions in a lump on the side of the liquid crystal display apparatus. For instance, in the case of displaying the screen in the mode D-(h) (320 x 200 pixels) by the ferroelectric liquid crystal display apparatus of 1280 x 1024 pixels or the like, the enlarged display from one time to four times can be realized. Even if such an enlarged display is used, redundant pixels also occur in the portion out of the effective display area depending on the relation between the number of effective pixels (resolution) of the liquid crystal display apparatus and the resolution in the display mode.

Therefore, it is necessary to execute a proper process to the portion (border portion) of the redundant pixels out of the effective display area.

In the case of displaying in the display mode of a low resolution by the CRT, the portion to which an electron beam is not irradiated is held black (dark) by thinning out and scanning the fluorescent display surface by reducing the scanning frequency of the electron beam. However, in the case of the ferroelectric liquid crystal display apparatus, if no image data is input, a state of the pixel is not assured (bright or dark; on or off). Therefore, it is necessary to also input data into the portion of the redundant pixels and to drive and control.

SUMMARY OF THE INVENTION

The present invention is made to eliminate the foregoing problems which cannot be realized by an image information output circuit which is used in a conventional CRT or the like. It is an object of the invention to realize an image information output circuit for displaying the screens in various display modes which have been used in a conventional CRT or the like onto a display apparatus using a binary display element such as a ferroelectric liquid crystal display apparatus or the like without losing image data.

Another object of the invention is to realize an image information output circuit of a display apparatus using a ferroelectric liquid crystal or the like having a bistability (memory performance), comprising: a first multiplexer for leading image data which is read out of an image memory to the next stage every pixel data; palette RAMs each for outputting pixel data on the basis of the data which is output from the first multiplexer; and a second multiplexer for converting the pixel data from the palette RAM into an output format to transfer to the display apparatus, wherein a converting process of the image data and a process for an area (frame portion) out of the effective display area are executed in accordance with a display mode request from the main body CPU, thereby making it possible to cope with a number of various display modes.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a constructional diagram of an image information output circuit according to the invention;

Fig. 2 is a whole constructional diagram of a graphics controller including the image information output circuit according to the invention and of a ferroelectric liquid crystal display panel unit;

Fig. 3 is a diagram showing a data conversion format of a pixel multiplexer 11;

Figs. 4A to 4C are diagrams each showing the relation between the gradation data of a palette register in a palette RAM and the arrangement

of the pixels of an actual display panel;

Figs. 5A to 5C are diagrams each showing the relation between the image data from a VRAM and the addresses of a palette register;

Fig. 6 is a diagram showing a data conversion format of a pixel selector 14;

Fig. 7 is a diagram showing a construction of a border register and examples of border data and a display pattern;

Fig. 8 is a diagram showing the relation between the position of a border portion on a display screen and the horizontal and vertical blanking signals;

Fig. 9 is a diagram showing an example of a transfer format from an image information output circuit according to the invention; and

Fig. 10A and 10B is a diagram showing display modes in a personal computer made by IBM Corporation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 2 is a whole constructional diagram of a graphics controller provided on the side of a main body apparatus such as a personal computer or the like as a supply source of image information and a ferroelectric liquid crystal display apparatus. The image information output circuit according to the invention is provided in the graphics controller in Fig. 2.

The display panel is constructed by arranging 1024 scanning electrodes and 2560 information electrodes like a matrix and sealing a ferroelectric liquid crystal into a space between two glass plates which were subjected to an orientation process. Scanning lines are connected to a scanning electrode driving circuit. Information lines are connected to an information electrode driving circuit. One pixel has a construction of two bits/pixel in which one pixel is divided into portions having an area ratio of 3:2 as shown in O in the display panel in Fig. 2. The gradation display of four levels per pixel can be performed.

A display controller receives the display information from the image information output circuit according to the invention and controls the scanning electrode driving circuit and the information electrode driving circuit.

The graphics controller comprises: a CPU (central processing unit: hereinafter, referred to as a GCPU) to control the whole display functions; a VRAM (image information storing memory); and a display interface serving as an image information output circuit according to the invention. The graphics controller controls the management of the display information and the whole communication between a host CPU and the display apparatus.

Fig. 1 is a constructional diagram of the display interface according to the invention. The display interface comprises: a gradation conversion section 1 to convert image data from the VRAM into area gradation data; a border register 2 to determine data in the portion out of an effective display area; a scanning line address generator 3; and a data selector 4 for converting the image data into an output format to transfer the image data to the liquid crystal display apparatus. The operation will now be described hereinbelow with reference to the drawings.

(1) Gradation conversion section

When explaining the display modes under the graphics environment of the personal computer made by IBM Corporation as an example, the number of constructing bits per pixel of the image data stored in a VRAM 5 differs every display mode in a manner such that it is set to 4 bits/pixel in the mode 3(h) and is set to 8 bits/pixel in the mode 13-(h). In the embodiment, data of two bytes (16 bits) in the image data stored in the VRAM 5 is always output by a single reading operation (access) for the VRAM 5. Therefore, the number of pixels which are output by a single access to the VRAM 5 differs depending on the display mode. For instance, the image data of four pixels is output in the case of the mode 3(h) by the single access. The image data of two pixels is output in the case of the mode 13(h) by the single access. Since a palette RAM 12, which will be explained hereinlater, executes a gradation conversion on a pixel unit basis, the image data which was read out of the VRAM 5 must be led to the palette RAM 12 on a pixel unit basis.

A pixel multiplexer 11 is provided for this purpose. Fig. 3 shows an image data conversion format of the pixel multiplexer 11. The conversion modes are switched by a command from a GCPU 6 (Fig. 2). For instance, in the display mode 3(h), the image data of four pixels is output from the VRAM 5 by the single access. Therefore, the pixel multiplexer 11 is operated in a conversion mode B. In the conversion mode B, the pixel multiplexer 11 extracts the data of two pixels of VSD_0 to VSD_3 and VSD_4 to VSD_7 at the first phase from VSD_0 to VSD_{15} including data of four pixels which are output from the VRAM 5 and leads as Q_0 to Q_3 and Q_8 to Q_{11} to the palette RAM 12 and a palette RAM 13, respectively. Then, at the second phase, the data of two pixels of VSD_8 to VSD_{11} and VSD_{12} to VSD_{15} are led to the palette RAMs 12 and 13 as Q_0 to Q_3 and Q_8 to Q_{11}, respectively. As mentioned above, the pixel multiplexer 11 separately leads the image data to the palette RAMs 12

and 13 at two phases. On the other hand, in Fig. 3, conversion modes A and C correspond to the cases where the image data format in the VRAM is set to 8 bits/pixel and 2 bits/pixel, respectively. In a manner similar to the case of the above 4 bits/pixel, the image data is led to the palette RAM 12 on a pixel unit basis.

The palette RAMs 12 and 13 correspond to a portion for converting the pixel data (color information) from the VRAM 5 into the ON/OFF data of the pixels of the actual display panel on a unit pixel basis, respectively. The conversion from <color information in the depth direction> into <gradation information in the lateral direction> (area gradation) according to the invention is realized in the above portion. In the embodiment of Fig. 1, two palette RAMs have been arranged in parallel as a countermeasure for a point that the image data conversion rate in the palette RAM is slower than a required transfer rate to the display apparatus. If a processing speed of the palette RAM is sufficiently high, no problem occurs even when only one palette RAM is used. On the contrary, in the case where a reading speed from the VRAM 5 or operating speeds of the multiplexers 11 and 14 are enough high, by increasing the number of palette RAMs, the processing speed of the conversion system can be raised in correspondence to it.

Each of the palette RAMs 12 and 13 is constructed by 256 registers having a length of eight bits which are called palette registers. The gradation information (ON/OFF data of the pixels) corresponding to the color information of the pixels is previously written by the GCPU 6. In the embodiment, the same gradation information is written into the palette RAMs 12 and 13. Although the writing and reading operations for each palette RAM can be executed at arbitrary timings, they are ordinarily performed as necessary every horizontal or vertical scanning period.

Figs. 4A to 4C are diagrams each showing the relation between the gradation data (ON/OFF data of pixels) of the palette register in the palette RAM and the arrangement of the pixels of the actual display panel. Fig. 4C shows the minimum pixel unit of the display panel used in the embodiment. As mentioned above, one pixel is divided into portions at an area ratio of 3:2 and the gradation display of four levels is realized by respectively independently driving the two portions. Each of Figs. 4B and 4A shows a handling of one pixel in the enlarged display mode. By handling four pixels and sixteen pixels as one pixel in a lump, respectively, the enlarged display of two times and four times can be realized. The number of gradations which can be displayed also increases to 8 levels and 16 levels. As shown in Figs. 4A to 4C, the gradation data of the palette register corresponds to the ON/OFF data of each pixel on the display panel at a ratio of 1:1.

As shown in Figs. 5A to 5C, the pixel data (color information) from the VRAM 5 functions as an address to select the palette register in the palette RAM. For instance, in the case where the pixel data (color information) from the VRAM 5 relates to 4 bits/pixel, one of the 16 palette registers is selected. On the other hand, in the case where the pixel data relates to 8 bits/pixel and 2 bits/pixel, one of the 256 palette registers and one of the 4 palette registers are selected. When a certain palette register is selected, the gradation data PL_0 to PL_7 and PH_0 to PH_7 stored therein are output and are led to the pixel multiplexer 14 at the next stage.

The pixel multiplexer 14 executes a process to convert the ON/OFF data (data of at most eight bits) of the pixel which is output from the palette RAM into the number of bits which can be displayed in accordance with the enlarged display mode (e.g., 1x, 2x, 4x) of the display panel.

Fig. 6 shows conversion modes of the pixel multiplexer 14. For instance, a conversion mode B is selected in the case of executing the enlarged display of two times (2x) by the display panel. At this time, since the number of gradation data which can be obtained per pixel is equal to four bits, only four lower bits (PL_0 to PL_3; PH_0 to PH_3) are extracted from the 8-bit data PL_0 to PL_7 and PH_0 to PH_7 which are output from the palette RAMs 12 and 13, respectively. The extracted eight bits are output as PIX_0 to PIX_7. On the other hand, conversion modes A and C show conversion formats in the enlarged display mode of four times (4x) and in the equal magnification mode (1x), respectively.

As described above, the pixel data (color information) in the VRAM 5 is converted into the gradation data on the display panel by the two multiplexers 11 and 14 and the palette RAMs.

(2) Border register section

As mentioned above, in the case where the number of effective pixels of the liquid crystal display apparatus is larger than the resolution of the display mode, some pattern must be displayed in the redundant pixels (border portion) out of the effective display area. The border register 2 has been provided to store data which is output to the border portion. Fig. 7 shows a construction of a border register. In the embodiment, the border register fundamentally comprises one register of a length of eight bits and the eight bits correspond to border data BD_0 to BD_7 (Fig. 7), respectively. On the other hand, the border register 2 has a construction of what is called a double buffer. Data in

the border register 2 can be rewritten at an arbitrary timing from the GCPU 6. The actual border data is set into a border register output stage at a timing of a horizontal or vertical sync signal. A timing to transmit the data set in the border register 2 is controlled by horizontal and vertical blanking signals (HBlank and vBlank). Fundamentally, as shown in Fig. 8, border data is output when either one of the horizontal and vertical blanking signals is set to the Lo (low) level (in the blanking period). Image data in the effective display area is output in a period of time other than the blanking period. Explanation will be made in detail in conjunction with the operation of a data selector, which will be explained hereinlater.

(3) Scanning line address data generator

The scanning line address generator 3 has been provided to generate scanning line address data A_0 to A_{15} of the display panel. The generator 3 comprises a 12-bit binary counter (up to 4096 scanning lines can be selected) which uses as clocks a horizontal sync signal Hsync which is input from the display controller on the liquid crystal display apparatus side. The counter can preset a count value (scanning line address data) from the GCPU 6 at an arbitrary timing. Further, a count-up width (how many scanning lines should be jumped and scanned) can be also set.

(4) Output section to the liquid crystal display apparatus

The image data transfer formats to the ferroelectric liquid crystal display apparatus have already been proposed by the same applicant as the present invention in Japanese Patent Application Nos. 61-212184, 63-285141, and the like with respect to a communicating method to realize a high resolution display in a display element having a memory performance. According to the above propositions, with respect to the transfer of image data, there is used a method whereby the scanning line address information and the image information are serially time-sharingly transferred on the same transmission line for the scanning lines which need to be rewritten.

The data selector 4 has been provided to realize those transfer formats. The data selector 4 time-sharingly switches three kinds of data such as image data PD_0 to PD_7 which were subjected to the gradation conversion, border data BD_0 to BD_7, and scanning line address data A_0 to A_{15} on the basis of timing control signals from the GCPU 6 and sends the switched data to the display apparatus.

Fig. 9 shows an example of a transfer format from the display interface serving as an image information output circuit according to the invention which conforms with the methods of the above propositions. In Fig. 9, when the horizontal sync signal Hsync is input for a period of time when the horizontal blanking signal HBlank is set to the Lo level (in the blanking period), the data selector 4 first outputs the scanning line address data A_0 to A_{15} by two cycles (four clocks (CLK)) by the timing control from the GCPU 6. Then, the border data BD_0 to BD_7 from the border register 2 are continuously transmitted onto communication lines PIX_0 to PIX_7 for a period of time until the HBlank is set to the Hi (high) level. When the HBland is set to the Hi level (after completion of the blanking period), the image data PD_0 to PD_7 in the effective display area which were subjected to the gradation conversion are transmitted onto the communication lines PIX_0 to PIX_7. In Fig. 9, when the information of 640 pixels (1280 dots/640 pixels) has been transferred as image data in the effective display area, the GCPU 6 again sets the HBlank to the Lo level. When the HBlank is set to the Lo level, the data selector 14 again allows the border data BD_0 to BD_7 to be transmitted onto the communication lines PIX_0 to PIX_7 and finishes the transfer of the data (640 pixels) of all of the pixels.

Fig. 9 shows transfer timings in the horizontal scanning direction. The data selector 4 also similarly distinguishes the border area and the effective display area by using the vertical blanking signal with respect to the vertical scanning direction and switches the output data.

Further, by controlling the timings of the HBlank and VBlank, the effective display area can be also displayed at an arbitrary position on the display screen.

As described above, in the display apparatus using the ferroelectric liquid crystal or the like having the bistability (memory performance), there is provided an image information output circuit having: a first multiplexer to lead image data which is read out of an image memory to the next stage every pixel; palette RAMs for outputting ON/OFF data of predetermined pixels on the basis of data which is output from the first multiplexer; and a second multiplexer to convert the data from the palette RAMs into an output format to transfer it to a display apparatus. The converting process of the image data and the process of an area (frame portion) out of the effective display area are executed in accordance with a display mode request from a main body CPU. Thus, display screens in various display modes which have conventionally been used in a CRT or the like can be displayed on the display apparatus using a binary display

element such as a ferroelectric liquid crystal display apparatus or the like without losing the image.

Claims

1. A display apparatus which uses a display panel using a liquid crystal having a memory performance and can display image data in a plurality of display modes in which the number of pixels, display color, minimum pixel unit, and the like respectively differ, comprising: memory means for storing the image data;
pixel data output means for outputting the image data stored in the memory means pixel data by pixel data;
converting means for converting the pixel data which was output by the pixel data output means into binary data which is displayed on the display panel;
display data output means for converting the binary data which was converted by the converting means into display data corresponding to the display mode and outputting; and
display control means for allowing the image data which was output by the display data output means to be displayed on the display panel.

2. A display apparatus according to claim 1, wherein the pixel data output means is a multiplexer.

3. A display apparatus according to claim 1, wherein the converting means is an RAM (random access memory) in which binary data has been stored.

4. A display apparatus according to claim 1, wherein the converting means is constructed by a plurality of RAMs (random access memories) in each of which binary data has been stored.

5. A display apparatus according to claim 1, further having frame display means for displaying desired frame image data to an area out of an effective display area of the image data which was displayed on the display panel.

6. A display apparatus according to claim 5, wherein the frame display means outputs and displays the frame image data of the area out of the effective display area within horizontal and vertical blanking periods of time of the image data which is displayed in the effective display area.

7. A display apparatus according to claim 1, wherein the display data output means is a multiplexer.

8. A display apparatus according to claim 1, wherein the liquid crystal having the memory performance is a ferroelectric liquid crystal.

9. A display apparatus using a display panel using a liquid crystal having a memory performance, comprising:
frame display means for displaying frame image data to an area out of an effective display area to display image data of the display panel,
wherein the frame display means outputs and displays the frame image data within horizontal and vertical blanking periods of time of the image data.

10. A display apparatus according to claim 9, wherein the liquid crystal having the memory performance is a ferroelectric liquid crystal.

11. A display apparatus according to claim 9, wherein the frame display means sets the frame image data of the area out of the effective display area within one horizontal scanning period or one vertical display period of time of the image data.

12. A display apparatus according to claim 9, wherein the frame display means further has memory means for storing the frame image data which is displayed to the area out of the effective display area.

13. A display controller for controlling a display having discrete display states, the display controller being operable in a plurality of display modes, including conversion means for converting stored image data into displayable image data responsive to the selected mode.

14. An image output control circuit for displaying images in a selected one of a plurality of display modes on a discrete level display device, in which there are provided gradation conversion means for displaying a depthwise colour gradation appearance on the display, in dependence upon the selected format.

FIG. 1

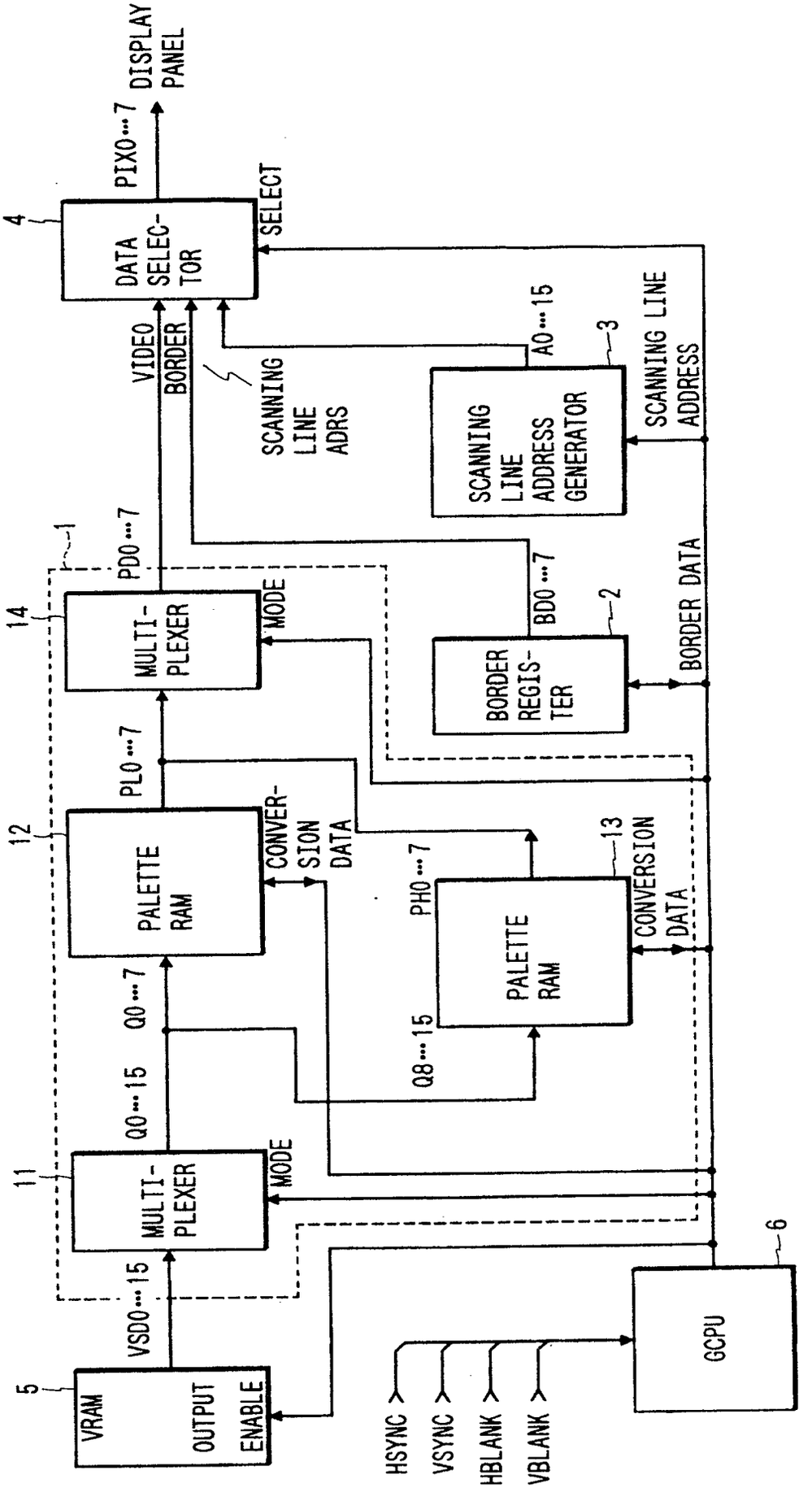
DISPLAY PANEL
PIX0...7
4
DATA SELEC-TOR
SELECT
VIDEO BORDER
SCANNING LINE ADRS
A0...15
3
SCANNING LINE ADDRESS GENERATOR
SCANNING LINE ADDRESS
1
PD0...7
14
MULTI-PLEXER
MODE
BD0...7
2
BORDER REGIS-TER
BORDER DATA
PL0...7
12
PALETTE RAM
CONVER-SION DATA
PH0...7
13
PALETTE RAM
CONVERSION DATA
Q0...7
Q8...15
Q0...15
11
MULTI-PLEXER
MODE
VSD0...15
5
VRAM
OUTPUT ENABLE
HSYNC
VSYNC
HBLANK
VBLANK
6
GCPU

FIG. 2

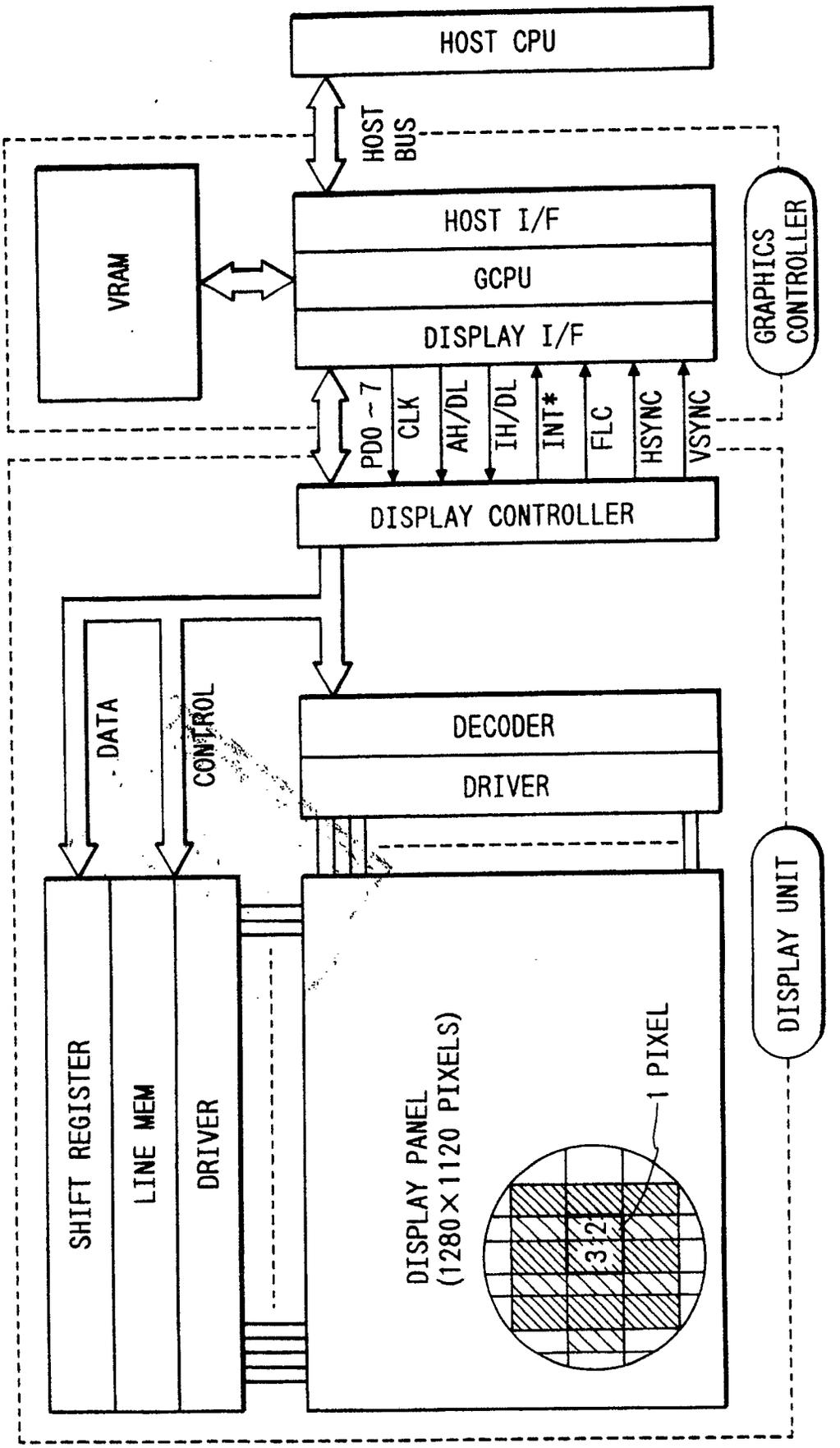
HOST CPU
HOST BUS
VRAM
HOST I/F
GCPU
DISPLAY I/F
GRAPHICS CONTROLLER
PD0 ~ 7
CLK
AH/DL
IH/DL
INT*
FLC
HSYNC
VSYNC
DISPLAY CONTROLLER
DATA
CONTROL
DECODER
DRIVER
SHIFT REGISTER
LINE MEM
DRIVER
DISPLAY PANEL
(1280×1120 PIXELS)
1 PIXEL
312
DISPLAY UNIT

FIG. 3

PIXEL MULTIPLEXER 11 CONVERSION MODE

MODE	PHASE	INPUT (VRAM DATA)	OUTPUT (PALETTE ADRS)
A	1	VSD 0～7	Q 0～7 [8BITS/PIXEL]
		VSD 8～15	Q 8～15
B	1	VSD 0～3	Q 0～3 [4BITS/PIXEL]
		VSD 4～7	Q 8～11
	2	VSD 8～11	Q 0～3
		VSD 12～15	Q 8～11
C	1	VSD 0～1	Q 0～1 [2BITS/PIXEL]
		VSD 2～3	Q 8～9
	2	VSD 4～5	Q 0～1
		VSD 6～7	Q 8～9
	3	VSD 8～9	Q 0～1
		VSD 10～11	Q 8～9
	4	VSD 12～13	Q 0～1
		VSD 14～15	Q 8～9

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FIG. 4A

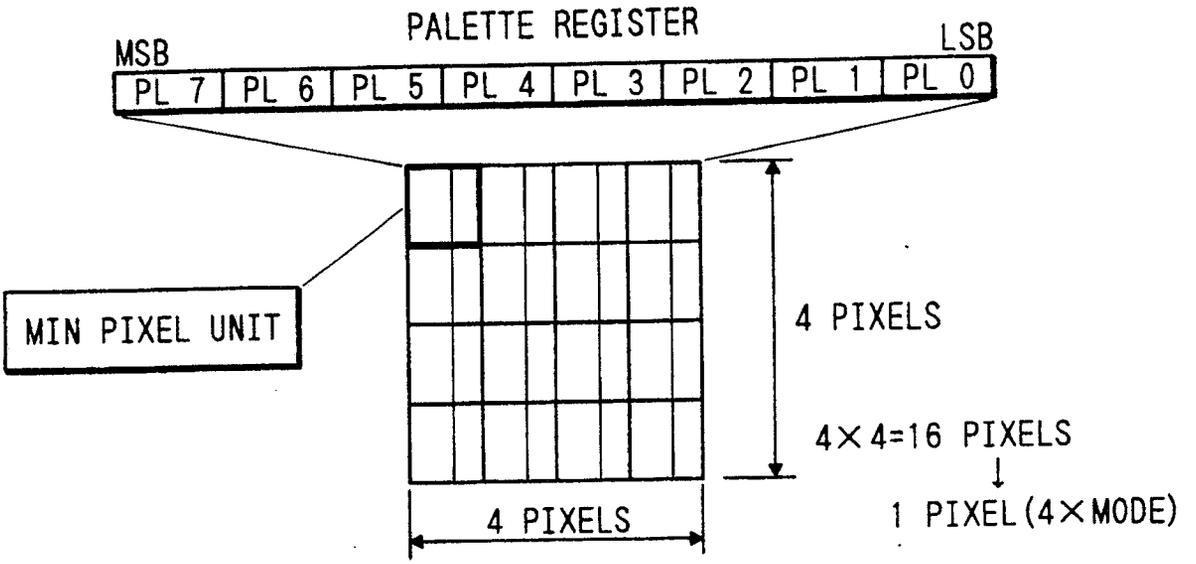


FIG. 4B

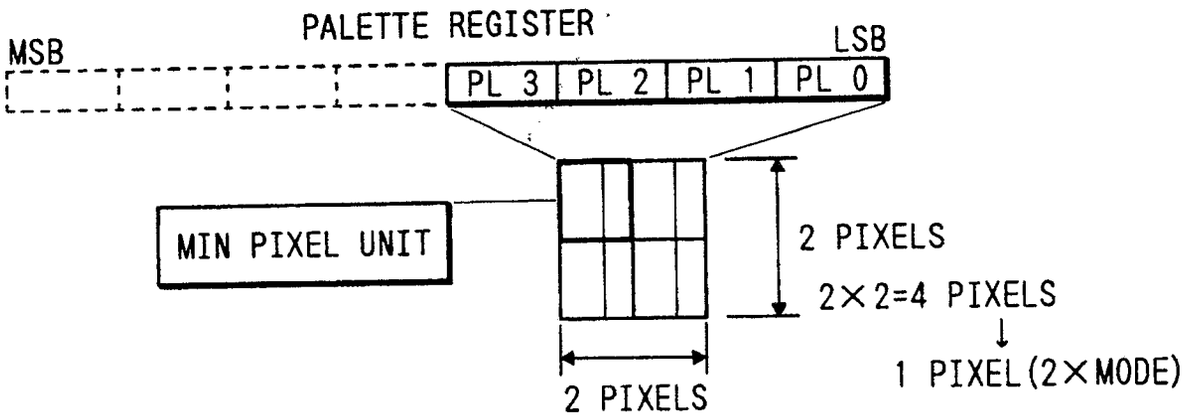


FIG. 4C

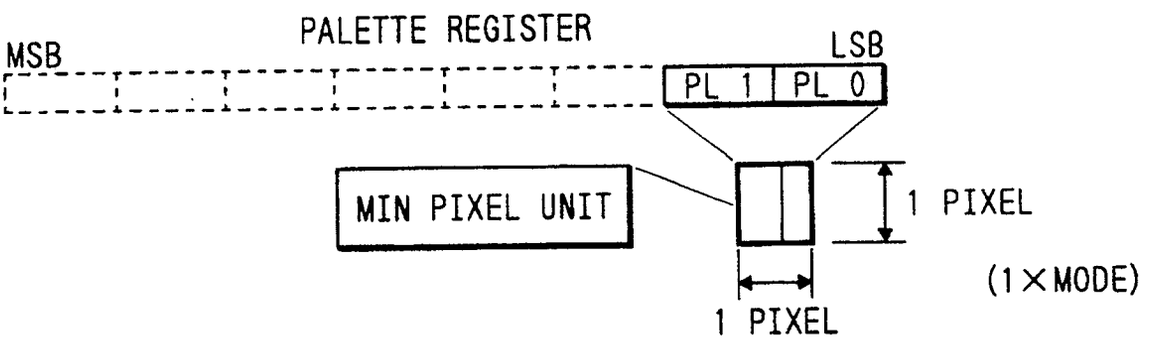


FIG. 5A

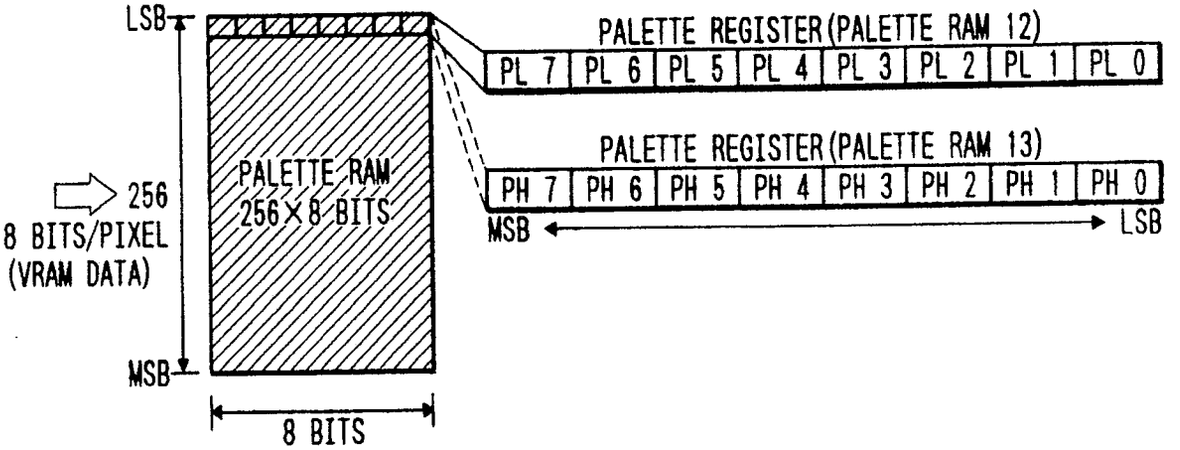


FIG. 5B

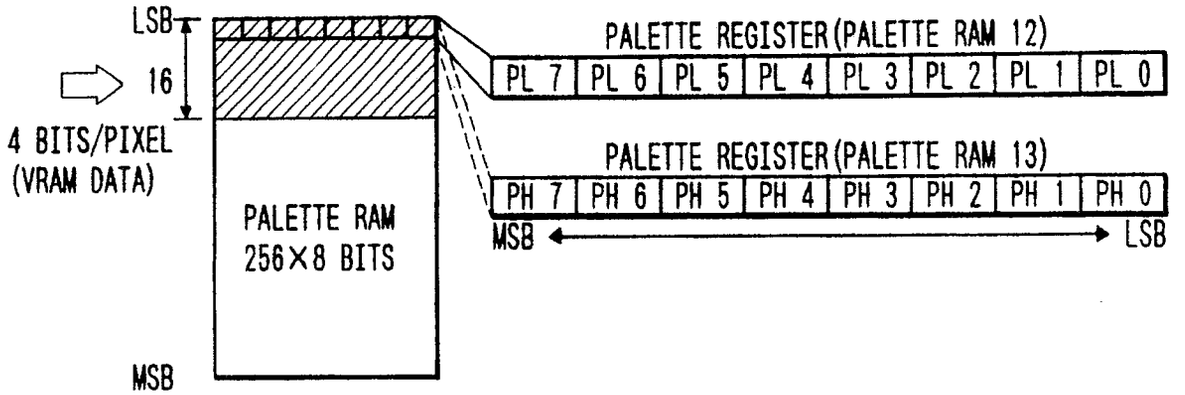


FIG. 5C

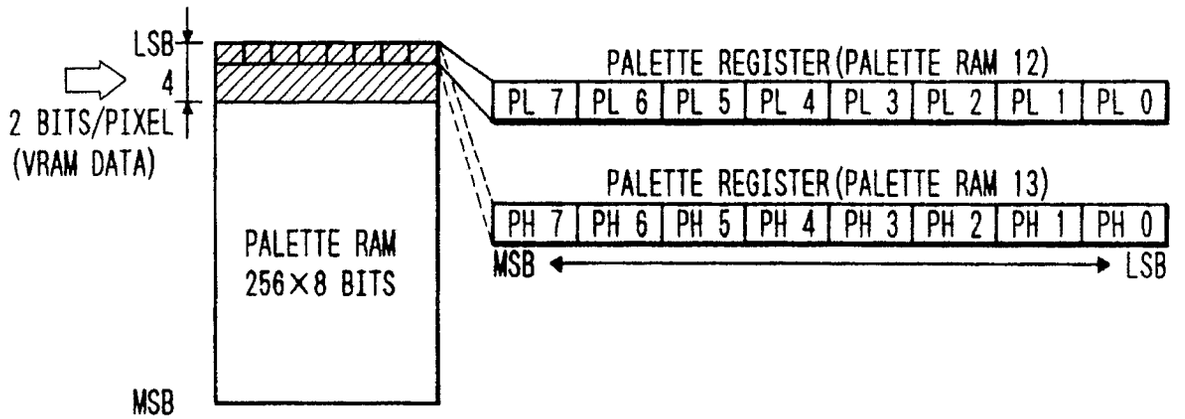


FIG. 6

PIXEL MULTIPLEXER 14 CONVERSION MODE

MODE	PHASE	INPUT (PALETTE DATA)		OUTPUT (PIXEL ON/OFF)	
A	1	PL 0~7	→	PD 0~7	[4X MODE]
	2	PH 0~7		PD 0~7	
B	1	PL 0~3		PD 0~3	[2X MODE]
		PH 0~3		PD 4~7	
C	1	PL 0~1		PD 0~1	[1X MODE]
		PH 0~1		PD 2~3	
	2	PL 0~1		PD 4~5	
		PH 0~1		PD 6~7	

EP 0 421 772 A2

FIG. 7

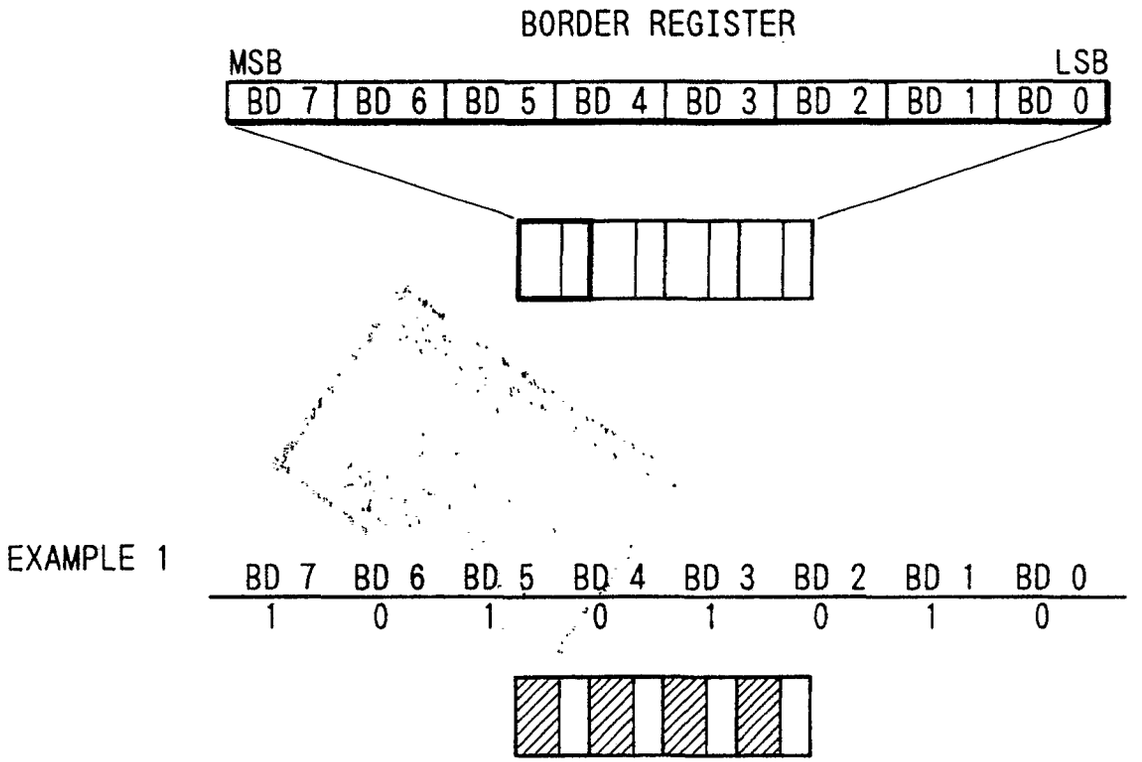
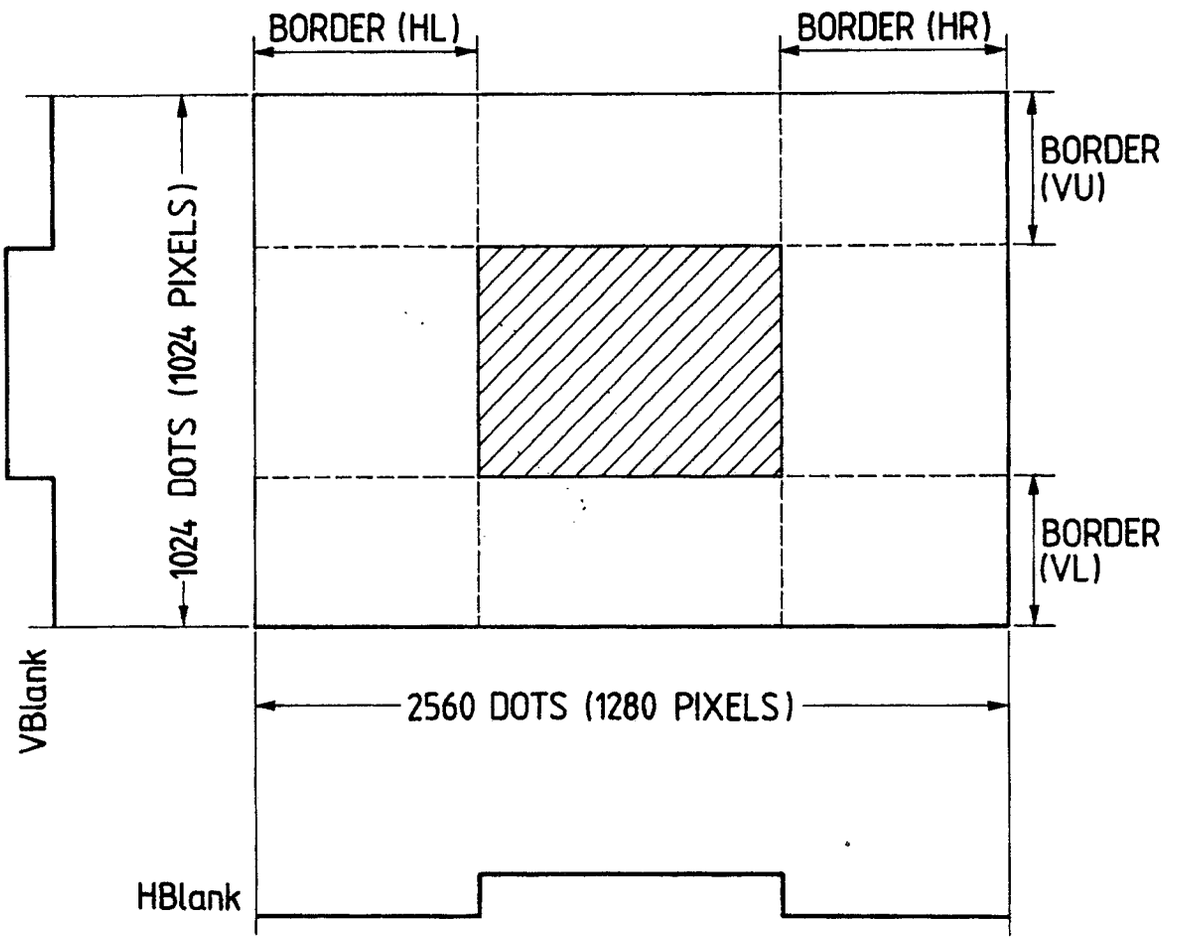

BORDER REGISTER
MSB
LSB
BD 7
BD 6
BD 5
BD 4
BD 3
BD 2
BD 1
BD 0
EXAMPLE 1
BD 7 BD 6 BD 5 BD 4 BD 3 BD 2 BD 1 BD 0
1 0 1 0 1 0 1 0
EXAMPLE 2
BD 7 BD 6 BD 5 BD 4 BD 3 BD 2 BD 1 BD 0
0 0 1 1 0 0 1 1

FIG. 8



(HL) : HORIZONTAL LEFT
(HR) : HORIZONTAL RIGHT
(VU) : VERTICAL UPPER
(VL) : VERTICAL LOWER

FIG. 9

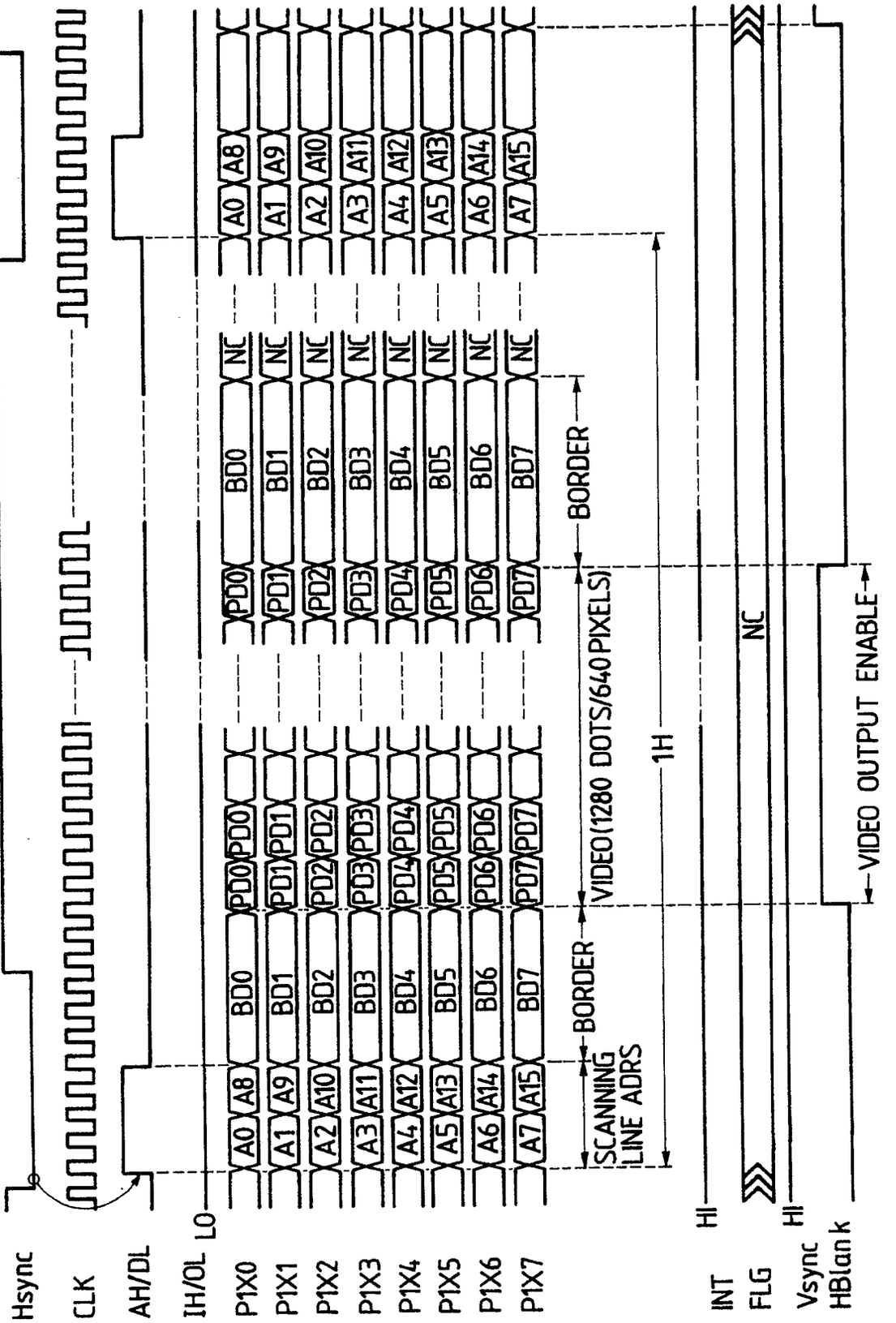

Hsync
CLK
AH/DL
IH/OL
P1X0
P1X1
P1X2
P1X3
P1X4
P1X5
P1X6
P1X7
INT
FLG
Vsync
HBlank
LO
HI
A0 A8 BD0 PD0
A1 A9 BD1 PD1
A2 A10 BD2 PD2
A3 A11 BD3 PD3
A4 A12 BD4 PD4
A5 A13 BD5 PD5
A6 A14 BD6 PD6
A7 A15 BD7 PD7
NC
BORDER
VIDEO(1280 DOTS/640 PIXELS)
1H
SCANNING LINE ADRS
VIDEO OUTPUT ENABLE

FIG. 10A

ALPHANUMERIC MODE

MODE	NO OF PIXELS	COLOR	BITS/PIXEL
0, 1	320×200	16	4
0*, 1*	320×350	16	4
0+, 1+	320×400	16	4
2, 3	640×200	16	4
2*, 3*	640×350	16	4
2+, 3+	720×400	16	4
7*	720×350	mono	1
7+	720×400	mono	1

FIG. 10B

GRAPHICS MODE

MODE	NO OF PIXELS	COLOR	BITS/PIXEL
4.5	320×200	4	2
6	640×200	2	1
D	320×200	16	4
E	640×200	16	4
F	640×350	4	2
10	640×350	16	4
11	640×480	2	1
12	640×480	16	4
13	320×200	256	8