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(54) **A logic circuit.**

(57) Output driving circuitry (31) can be connected to, or included in, an emitter-coupled logic circuit (2) of the kind providing mutually-complementary first and second logic signals. The circuitry (22) comprises a first transistor (Q_4), having a base terminal for connection to receive the said first logic signal, a collector terminal connected to a first power supply line (2ND POWER SOURCE) of the circuitry, and an emitter terminal connected to an output node (13) of the circuitry, the transistor being connected in an emitter-follower circuit configuration so as to provide at the said output node (13) an output signal (OR OUTPUT) derived from the said first logic signal.

The circuitry further includes pull-down means (Q_5, R_{11}) including a second transistor (Q_5), having a base terminal connected to a control node (15) of the pull-down means and having an emitter terminal connected to a second power supply line (3RD POWER SOURCE) of the circuitry that is lower in potential than the said first power supply line, when the circuitry is in use, and having a collector terminal connected to the said output node (13) of the circuitry. The pull-down means also include a resistor (R_{11}) connected between the said output node (13) and a third power supply line (4TH POWER SOURCE) of the circuitry that is higher in potential than the said second power supply line (3RD POWER SOURCE) when the circuitry is in use.

Control means (not shown) connected to the said control node (15) operate in dependence upon

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the emitter-coupled logic circuit to facilitate fall in the potential of the said output node (13), when the said output signal (OR OUTPUT) is subjected to a transition from a high to a low logic level, but to maintain the said second transistor (Q_5) in a non-conductive operating condition when the said output signal (OR OUTPUT) is not being subjected to such a transition.

Such circuitry can enable the high-to-low transition to occur desirably quickly without increasing the power consumption unacceptably.

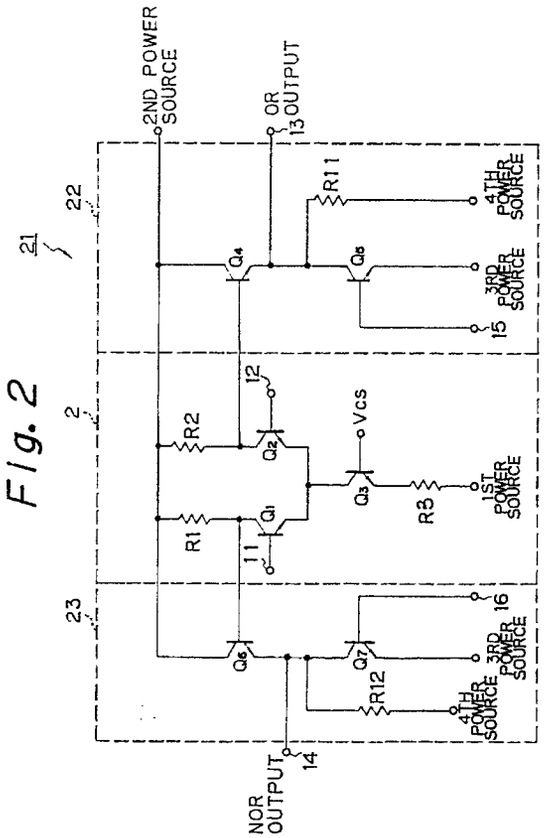

Fig. 2

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EUROPEAN SEARCH REPORT

Application Number

EP 90 31 0171

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X Y	US-A-3 978 347 (HOLLSTEIN et al.) * Figures 1,2; column 1, line 63 - column 3, line 64 *	1-4, 11-13,19, 21,32 5,6,14,20, 33	H 03 K 19/086 H 03 K 19/013
Y	PATENT ABSTRACTS OF JAPAN, vol. 11, no. 271 (E-536)[2718], 3rd September 1987; & JP-A-62 72 221 (NEC CORP.) 02-04-1987 * Fig.; p. (E-536)[2718] *	5,6,14,20, 33	
A	EP-A-0 317 271 (APPLIED MICRO CIRCUITS CORP.) * Figures 1-4; column 5, line 29 - column 12, line 1 *	1-6,8	
A	WO-A-8 601 055 (TANDEM COMPUTERS INC.) * Figure 4; page 10, lines 17-26 *	16-18	
A	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 343 (E-796)[3691], 2nd August 1989; & JP-A-1 101 022 (HITACHI LTD) 19-04-1989 * Fig.; p. (E-796)[3691] *	22	
A	EP-A-0 176 799 (FUJITSU LTD) * Figure 1; page 10, lines 11-14 *	25	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 03 K
A	RCA TECHNICAL NOTES, no. 771, 25th September 1968, Princeton, NJ, US; D.C. BUSSARD: "Saturating transistor emitter follower"	16,22	

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	21 August 91	FEUER F.S.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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A: technological background
O: non-written disclosure
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E: earlier patent document, but published on, or after the filing date
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&: member of the same patent family, corresponding document