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Circuit for driving a liquid crystal panel.

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Description

The present invention relates to a semiconductor integrated circuit and, more particularly, to a semiconductor integrated circuit used in an LSI for driving a liquid crystal panel with a MOS structure and displaying data on the liquid crystal panel.

An ordinary LCD-driver/controller IC is disclosed in "EDN Electrical Design News", vol. 30, no. 18, August 1985, Newton, Massachusetts, US, pages 83-88, Ed Teja: "LCD-driver/controller ICs offer versatility in configuration and function". A semiconductor integrated circuit for driving a liquid crystal panel generally comprises a group of shift registers for transferring data, a wire for fetching the data transferred from each of the shift registers, and a circuit for receiving the data and outputting a signal corresponding to the data. Fig. 1 illustrates a circuit which is formed as an LSI. The LSI includes shift registers 151a to 151n, signal fetch wires 151b to 151n, circuit blocks 151c to 151n, and signal fetch pads 151d to 151n.

When a semiconductor integrated circuit is formed on a chip as an LSI, in order to reduce the size of the chip, the circuit is divided into A and B arrays to fetch output signals from four sides of the chip, as illustrated in Fig. 2. Since the order of arrangement of output pads 151Ad to 151Bd is the same as that of data transfer, data is transferred from left to right in the A array and from right to left in the B array in shift registers 151Aa to 151Ba, as shown in Fig. 2. The circuit blocks supplied with signals from the shift registers have the same block pattern to easily lay out a mask pattern. Circuit blocks 151Ac to 151Bc in the A array and circuit blocks 151Bc to 151Bc in the B array are, therefore, arranged opposite to each other. In Fig. 2, the direction of character "P" of each circuit block corresponds to that of a mask pattern of the circuit block.

Fig. 3 is a detail view of a right-side part of the circuit shown in Fig. 2. Referring to Fig. 3, shift register 151Ab comprises clocked inverters 17A1 and 17A2 which are connected in cascade, and circuit block 151Ac includes MOS transistor 17A3. Furthermore, shift register 151Ba comprises clocked inverters 17B1 and 17B2 which are connected in cascade, and circuit block 151Bc includes transistor 17B3. The direction of current 17AI of transistor 17A3 of the circuit block in the A array is opposite to that of current 17BI of transistor 17B3 of the circuit block in the B array. Even though transistors 17A3 and 17B3 whose current directions are opposite to each other are formed on the same chip, the dispersions of output characteristics of these transistors, due to misalignment of the mask caused in the manufacture process, are different as shown in Fig. 4. In Fig. 4, L denotes output characteristics of transistor 17A3, and M indicates those of transistor 17B3.

An explanation of misalignment of the patterns of, for example, a diffusion mask and a polysilicon mask will be given as follows. Fig. 5 shows glass mask misalignment of source diffusion layer S_1 , drain diffusion layer D_1 , and gate electrode G_1 of transistor 17A3 and that of source diffusion layer S_2 , drain diffusion layer D_2 , and gate electrode G_2 of transistor 17B3. The misalignment of gate electrode G_1 increases the resistance of source diffusion layer S_1 and decreases that of drain diffusion layer D_1 , and the misalignment of gate electrode G_2 decreases the resistance of source diffusion layer S_2 and increases that of drain diffusion layer D_2 . The increase of resistance of the source diffusion layer is more influential than that of resistance of the drain diffusion layer since a voltage between the gate electrode and source diffusion layer is lowered by not only a variation in value of the resistance but also a drop of voltage of a resistor of the source diffusion layer and a threshold voltage of the transistor is heightened by increase in a voltage between the substrate and source diffusion layer. As the drain voltage and drain current characteristics of the transistors, as shown in Fig. 6, the current of transistor 17A3 whose source resistance increases is smaller than that of transistor 17B3 whose source resistance decreases.

Fig. 7 illustrates circuit blocks 151Ac and 151Bc including differential amplifiers 15A and 15B, respectively. Differential amplifiers 15A and 15B greatly influence the output characteristics of the circuit blocks. Since, however, the differential amplifiers are asymmetric and the currents thereof flow in the directions opposite to each other, they exhibit different output characteristics as shown in Fig. 8.

It is accordingly an object of the present invention to provide a semiconductor integrated circuit for driving a liquid crystal panel in which the output characteristics between elements or circuits are uniformed to obtain uniform outputs.

According to an aspect of the present invention, there is provided a semiconductor integrated circuit for driving a liquid crystal panel, comprising: a semiconductor chip; a first group of m data transfer means formed on said semiconductor chip, for transferring data in one direction; a second group of m data transfer means formed on said semiconductor chip, for transferring data from said first group of m data transfer means in a direction opposite to said one direction; and first and second groups of m data output means for temporarily storing data from said first and second groups of m data transfer means and outputting the data outside said semiconductor chip, wherein circuit elements of a first one of said first group of data output means and an m-th one of said second group of data output means, those of a second one of said first group thereof and a (m-1)th one of said second group thereof, ..., and those of an m-th one of said first group thereof and a first one of said second group

thereof have output stages for supplying data outside said semiconductor chip, the circuit elements constituting the output stages have the same function and are symmetrically arranged, and currents flow through the symmetrically-arranged circuit elements in the same direction.

In the present invention, the transistors of both circuit blocks, which greatly influence the circuit characteristics between the blocks, are symmetrical and the currents thereof flow in the same direction. Even though the dispersion of the characteristics due to mask misalignment occurs in the manufacturing process, the uniform characteristics can be obtained between both the circuit blocks.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1 and 2 are block diagrams illustrating a conventional semiconductor integrated circuit for driving a liquid crystal panel;

Fig. 3 is a circuit diagram illustrating the conventional semiconductor integrated circuit;

Fig. 4 is a graph of the electrical characteristics of MOS transistors of the conventional semiconductor integrated circuit;

Fig. 5 is a plan pattern view of the MOS transistors of the conventional semiconductor integrated circuit;

Fig. 6 is a graph of the electrical characteristics of the MOS transistors of the conventional semiconductor integrated circuit;

Fig. 7 is a circuit diagram of the conventional semiconductor integrated circuit using differential amplifiers;

Fig. 8 is a graph of the output characteristics of the differential amplifiers;

Figs. 9 and 10 are block diagrams showing a semiconductor integrated circuit for driving a liquid crystal panel according to the present invention;

Fig. 11 is a circuit diagram specifically showing shift registers and circuit blocks of the circuit shown in Figs. 9 and 10;

Fig. 12 is a graph of the output characteristics of a MOS transistor at the output stage of the circuit blocks shown in Fig. 11;

Fig. 13 is a circuit diagram specifically showing shift registers and circuit blocks shown in Figs. 9 and 10;

Fig. 14 is a graph of the output characteristics of a differential amplifier at the output stage of the circuit blocks shown in Fig. 13;

Fig. 15 is a pattern plan view of the MOS transistor shown in Fig. 12; and

Fig. 16 is a graph of electrical characteristics of the MOS transistor shown in Fig. 12.

An embodiment of the present invention will be described with reference to the accompanying drawings.

Fig. 9 is a block diagram showing a basic arrangement of a semiconductor integrated circuit for driving a liquid crystal panel according to the embodiment of the present invention. In Fig. 9, shift registers 11Aa to 1mAa connected in cascade, for transferring data from an LSI for driving a liquid crystal panel to the right and shift registers 11Ba to 1mBa connected in cascade, for transferring the data to the left are arranged so as to turn around a data transfer path. Signal lines 11Ab to 1mAb are arranged between shift registers 11Aa to 1mAa and circuit blocks 11Ac to 1mAc, respectively, to supply data from the shift registers to the circuit blocks. Signal lines 11Bb to 1mBb are formed between shift registers 11Ba to 1mBa and circuit blocks 11Bc to 1mBc, respectively, to supply data from the shift registers to the circuit blocks. Circuit blocks 11Ac to 1mAc and 11Bc to 1mBc include transistors to the gates of which data is input through signal lines 11Ab to 1mAb and 11Bb to 1mBb. In the upper and lower corresponding circuit blocks in Fig. 9, portions of the circuit blocks directly connected to pads, mentioned later, have a symmetrical structure and the same function, and the current flows through the circuit portions in the same direction. Circuit blocks 11Ac to 1mAc and 11Bc to 1mBc temporarily store data from shift registers 11Aa to 1mAa and 11Ba to 1mBa, respectively.

Fig. 10 is a block diagram of the semiconductor integrated circuit shown in Fig. 9, which is formed on chip CH. The circuit is divided into two stages of A and B arrays, and pads 21Ad to 2mAd and 21Bd to 2mBd are pulled out of four sides of chip CH. In Fig. 10, symbol IP indicates an input pad.

Fig. 11 is a circuit diagram specifically showing part 2c of the circuit shown in Fig. 10. The A Array comprises shift register 1mAa including clocked inverters 3A1 and 3A2, circuit block 1mAc including MOS transistor 3A3 for receiving transfer data, as a gate signal, from shift register 1mAa through signal line 1mAb, and pad 1mAd serving as a terminal for supplying data from circuit block 1mAc outside the chip. The B array comprises shift register 1mBa including clocked inverter 3B1 and 3B2, circuit block 11Bc including MOS transistor 3B3 for receiving transfer data, as a gate signal, from shift register 11Ba through signal line 11Bb, and pad 11Bd serving as a terminal for supplying data from the circuit block outside the chip.

Since MOS transistors 3A3 and 3B3 are directly connected to other circuits, each of which constitutes an LSI for driving a liquid crystal panel which is arranged outside the chip, through pads 1mAd and 11Bd, respectively, the MOS transistors greatly influence the characteristics of circuit blocks 1mAc and 11Bc. The plan patterns of MOS transistors 3A3 and 3B3 are symmetrical, and currents 3AI and 3BI flow in the same direction. Therefore, as shown in Fig. 12, the output characteristics of MOS transistors 3A3 and

3B3 are the same.

Fig. 13 is a circuit diagram specifically showing another example of part 2c of the circuit shown in Fig. 10. In Fig. 13, reference numerals 15A and 15B denote differential amplifiers, TR1 and TR2 indicate constant current source transistors, C1 and C2 show dynamic storing capacitors, AS1 and AS2 indicate analog switches, and IN1 and IN2 denote inverters. Since differential amplifiers 15A and 15B are directly connected to other circuits, each of which constitutes an LSI for driving a liquid crystal panel which is arranged outside the chip, through pads 1mA_d and 11B_d, respectively, the differential amplifiers greatly influence the characteristics of circuit blocks 1mA_c and 11B_c. The plan patterns of differential amplifiers 15A and 15B are symmetrical, and currents 3A_I and 3B_I flow in the same direction. Even though mask misalignment occurs in manufacturing an LSI for driving a liquid crystal panel, the output characteristics of differential amplifiers 15A and 15B are the same, as shown in Fig. 14.

Fig. 15 is a plan pattern view of transistors 3A3 and 3B3 shown in Fig. 11 for explaining the effects obtained by symmetrically arranging the MOS transistors. In conventional transistors which are asymmetrically arranged and into which currents flow in different directions, even though they are formed in the same chip, the characteristics of the transistors vary with the misalignment of masks and the angle of ion-implantation for diffusion of an impurity into source and drain regions. If, however, the transistors are symmetrically arranged and the directions of the currents flowing through the transistors are the same, the characteristics of the transistors are uniformed. Even when misalignment occurs between a diffusion mask pattern and a mask pattern of polysilicon gates G₁₁ and G₁₂, source regions S₁₁ and S₁₂ have the same increase in resistance and drains D₁₁ and D₁₂ have the same decrease in resistance, and the currents of transistors 3A3 and 3B3 flow in the same direction. As shown in Fig. 16, therefore, the drain voltage - drain current characteristics of the transistors are the same.

In MOS transistors 17A3 and 17B3 of the conventional semiconductor integrated circuit for driving a liquid crystal panel shown in Fig. 5, their plan patterns are asymmetrical, and the area of source region S₁ of MOS transistor 17A3 is in inverse proportion to that of source region S₂ of MOS transistor 17B3. Further, the area of drain regions D₁ of MOS transistor 17A3 is in inverse proportion to that of drain region D₂ of MOS transistor 17B3. The source resistances of MOS transistors 17A3 and 17B3 are in inverse proportion to each other, and the drain resistances the MOS transistors are also in inverse proportion to each other. Hence, the electrical characteristics of the transistors are different.

The differences in area between source regions

S₁ and S₂ and between drain regions D₁ and D₂ of MOS transistors 17A3 and 17B3 are caused by the mask misalignment in the manufacturing process. The differences are also caused for the following reason. To form the source and drain regions, an impurity diffuse from the surface of a semiconductor substrate at a predetermined implantation angle which is shifted from the right angle with the surface of the semiconductor substrate and therefore, a portion where the implantation is intercepted by the gate region is narrow and the other portion is large. The difference in area causes the electrical characteristics of the transistors to differ from each other.

As is apparent from Fig. 15, however, the plan patterns of MOS transistors 3A3 and 3B3 are symmetrical with respect to line L. The areas of source regions S₁₁ and S₁₂ of both the transistors are proportionate to each other and the areas of drain regions D₁₁ and D₁₂ thereof are proportionate to each other. Accordingly, the source resistances of transistors 3A3 and 3B3 are proportionate to each other and the drain resistances thereof are proportionate to each other.

Since the plan patterns of MOS transistors 3A3 and 3B3 are symmetrical with respect to line L, even if source regions S₁₁ and S₁₂ and drain regions D₁₁ and D₁₂ are shifted from polysilicon gates G₁₁ and G₁₂, the electrical characteristics of both the transistors are always the same. The drain voltage - drain current characteristics of the transistors are therefore the same, as shown in Fig. 16.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A circuit for driving a liquid crystal panel, comprising:

a semiconductor chip (CH);

a first group of m data transfer means (11Aa, 12Aa, ..., 1mAa) formed on said semiconductor chip (CH), for transferring data in one direction;

a second group of m data transfer means (11Ba, 12Ba, ..., 1mBa) formed on said semiconductor chip (CH), for transferring data from said first group of m data transfer means (11Aa, 12Aa, ..., 1mAa) in a direction opposite to said one direction; and

first and second groups of m data output means (11Ac, 12Ac, ..., 1mA_c; 11Bc, 12Bc, ..., 1mBc) for temporarily storing data from said first and second groups of m data transfer means (11Aa, 12Aa, ..., 1mAa; 11Ba, 12Ba, ..., 1mBa) and outputting the data outside said semiconductor chip (CH),

characterized in that circuit elements of a

first one (11Ac) of said first group of data output means (11Ac, 12Ac, ..., 1mAc) and an m-th one (1mBc) of said second group of data output means (11Bc, 12Bc, ..., 1mBc), those of a second one (12Ac) of said first group thereof and a (m-1)th one (1m-1Bc) of said second group thereof, ..., and those of an m-th one (1mAc) of said first group thereof and a first one (11Bc) of said second group thereof have output stages for supplying data outside said semiconductor chip (CH), the circuit elements constituting the two groups of output stages have the same function and are symmetrically arranged so that, in use, currents flow through the symmetrically-arranged circuit elements in the same direction.

2. A circuit according to claim 1, characterized in that said first and second groups of data transfer means (11Aa, 12Aa, ..., 1mAa; 11Ba, 12Ba, ..., 1mBa) comprise m shift registers serving as data transfer means which are connected in cascade, and said data output means (11Ac, 12Ac, ..., 1mAc; 11Bc, 12Bc, ..., 1mBc) constituting said first and second groups of data output means include MOS transistors (3A3, 3B3) to gates of which data is input from said data transfer means.
3. A circuit according to claim 1, characterized in that said circuit elements constituting said first and second groups of data output means (11Ac, 12Ac, ..., 1mAc; 11Bc, 12Bc, ..., 1mBc) and serving as output stages for supplying data outside said semiconductor chip (CH) are differential amplifiers (15A, 15B).

Patentansprüche

1. Schaltung zum Antreiben eines Flüssigkristallfeldes, umfassend:
einen Halbleiterchip (CH);
eine erste Gruppe von m Datentransfereinrichtungen (11Aa, 12Aa, ..., 1mAa), die auf dem Halbleiterchip (CH) gebildet sind, zum Transferieren von Daten in einer Richtung;
eine zweite Gruppe von m Datentransfereinrichtungen (11Ba, 12Ba, ..., 1mBa), die auf dem Halbleiterchip (CH) gebildet sind, zum Transferieren von Daten von der ersten Gruppe von m Datentransfereinrichtungen (11Aa, 12Aa, ..., 1mAa) in einer Richtung entgegengesetzt zur ersten Richtung; und
erste und zweite Gruppen von m Datenausgabeeinrichtungen (11Ac, 12Ac, ..., 1mAc; 11Bc, 12Bc, ..., 1mBc) zum zeitweiligen Speichern von Daten von den ersten und zweiten Gruppen von m Datentransfereinrichtungen (11Aa, 12Aa, ...,

1mAa; 11Ba, 12Ba, ..., 1mBa) und Ausgeben der Daten nach außerhalb des Halbleiterchips (CH);
dadurch **gekennzeichnet**, daß

Schaltungselemente einer ersten (11Ac) der ersten Gruppe von Datenausgabeeinrichtungen (11Ac, 12Ac, ..., 1mAc) und einer m-ten (1mBc) der zweiten Gruppe von Datenausgabeeinrichtungen (11Bc, 12Bc, ..., 1mBc), die einer zweiten (12Ac) der ersten Gruppe davon und einer (m-1)ten (1m-1Bc) der zweiten Gruppe davon, ... und die einer m-ten (1mAc) der ersten Gruppe davon und einer ersten (11Bc) der zweiten Gruppe davon Ausgabestufen haben zum Zuführen von Daten nach außerhalb des Halbleiterchips (CH), wobei die Schaltungselemente, die die zwei Gruppen von Ausgabestufen bilden, die gleiche Funktion haben und symmetrisch angeordnet sind, so daß bei Benutzung Ströme durch die symmetrisch angeordneten Schaltungselemente in der gleichen Richtung fließen.

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet daß die ersten und zweiten Gruppen von Datentransfereinrichtungen (11Aa, 12Aa, ..., 1mAa; 11Ba, 12Ba, ..., 1mBa) m Schieberegister umfassen, die dienen als Datentransfereinrichtungen, welche in Kaskadenform verbunden sind, und die Datenausgabeeinrichtungen (11Ac, 12Ac, ..., 1mAc; 11Bc, 12Bc, ..., 1mBc), welche die ersten und zweiten Gruppen von Datenausgabeeinrichtungen bilden, MOS-Transistoren (3A3, 3B3) beinhalten, an deren Gates Daten eingegeben werden von den Datentransfereinrichtungen.
3. Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Schaltungselemente, welche die ersten und zweiten Gruppen von Datenausgabeeinrichtungen (11Ac, 12Ac, ..., 1mAc; 11Bc, 12Bc, ..., 1mBc) bilden und dienen als Ausgabestufen zum Zuführen von Daten nach außerhalb des Halbleiterchips (CH), Differentialverstärker (15A, 15B), sind.

Revendications

1. Circuit pour commander un panneau à cristaux liquides comprenant :
une puce de semi-conducteur (CH) ;
un premier groupe de m dispositifs de transfert de données (11Aa, 12Aa, ..., 1mAa) formé sur ladite puce de semi-conducteur (CH), pour transférer des données dans une direction ;
un second groupe de m dispositifs de transfert de données (11Ba, 12Ba, ..., 1mBa) formé sur ladite puce de semi-conducteur (CH), pour transférer des données à partir dudit pre-

mier groupe de m dispositifs de transfert de données (11Aa, 12Aa, ..., 1mAa) dans une direction opposée à ladite direction ; et

des premier et second groupes de m dispositifs de sortie de données (11Ac, 12Ac, ..., 1mAc ; 11Bc, 12Bc, ..., 1mBc) pour stocker temporairement des données à partir desdits premier et second groupes de m dispositifs de transfert de données (11Aa, 12Aa, ..., 1mAa ; 11Ba, 12Ba, ..., 1mBa) et pour fournir les données à l'extérieur de ladite puce de semi-conducteur (CH),

caractérisé en ce que des éléments de circuit d'un premier dispositif (11Ac) dudit premier groupe de dispositifs de sortie de données (11Ac, 12Ac, ..., 1mAc) et un m-ième dispositif (1mBc) dudit second groupe de dispositifs de sortie de données (11Bc, 12Bc, ..., 1mBc), ceux d'un second dispositif (12Ac) dudit premier groupe de ceux-ci et un (m-1)ième dispositif (1m-1Bc) dudit second groupe de ceux-ci, ..., et ceux d'un m-ième dispositif (1mAc) dudit premier groupe de ceux-ci et un premier dispositif (11Bc) dudit second groupe de ceux-ci, ont des étages de sortie pour fournir des données à l'extérieur de ladite puce de semi-conducteur (CH), les éléments de circuit constituant les deux groupes d'étages de sortie ont la même fonction et sont disposés symétriquement de sorte que lors de leur utilisation, des courants passent à travers les éléments de circuit disposés symétriquement dans la même direction.

2. Circuit selon la revendication 1, caractérisé en ce que lesdits premier et second groupes de dispositifs de transfert de données (11Aa, 12Aa, ..., 1mAa ; 11Ba, 12Ba, ..., 1mBa) comprend m registres à décalage servant comme dispositifs de transfert de données qui sont reliés en cascade, et ledit dispositif de sortie de données (11Ac, 12Ac, ..., 1mAc ; 11Bc, 12Bc, ..., 1mBc) constituant lesdits premier et second groupes de dispositifs de sortie de données comprend des transistors MOS (3A3, 3B3) aux grilles desquels des données sont introduites à partir desdits dispositifs de transfert de données.

3. Circuit selon la revendication 1, caractérisé en ce que lesdits éléments de circuit constituant lesdits premier et second groupes de dispositifs de sortie de données (11Ac, 12Ac, ..., 1mAc ; 11Bc, 12Bc, ..., 1mBc) et servant comme étages de sortie pour fournir des données à l'extérieur de ladite puce de semi-conducteur (CH) sont des amplificateurs différentiels (15A, 15B).

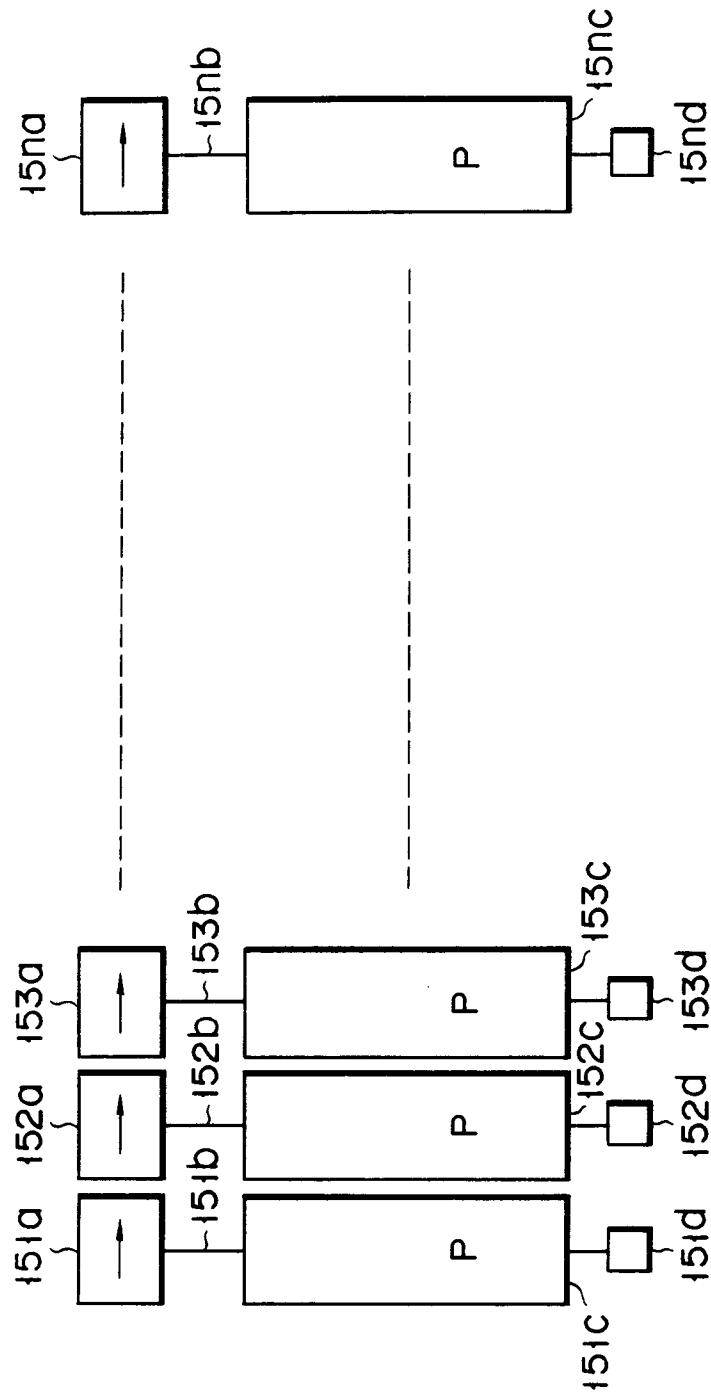


FIG. 1

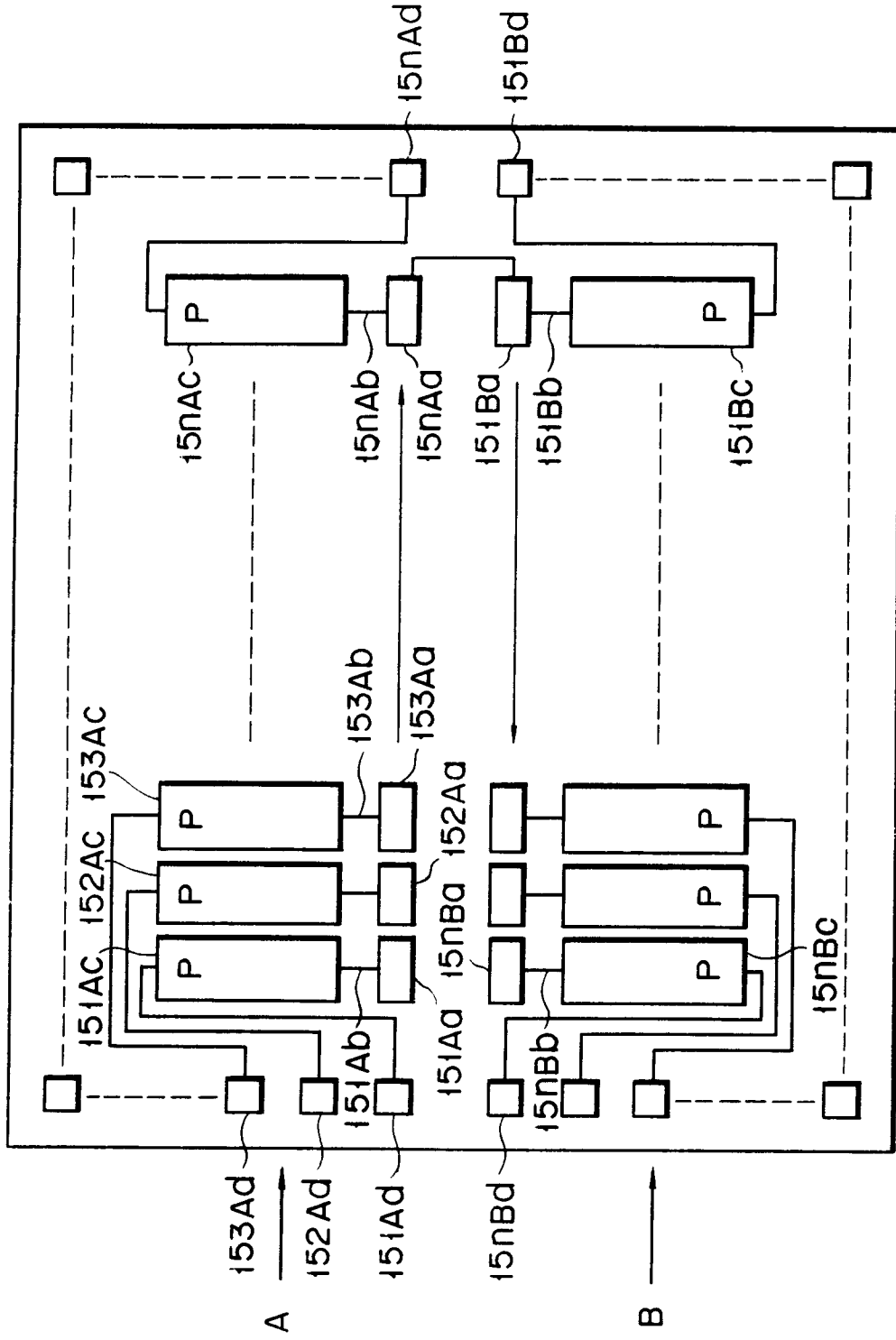


FIG. 2

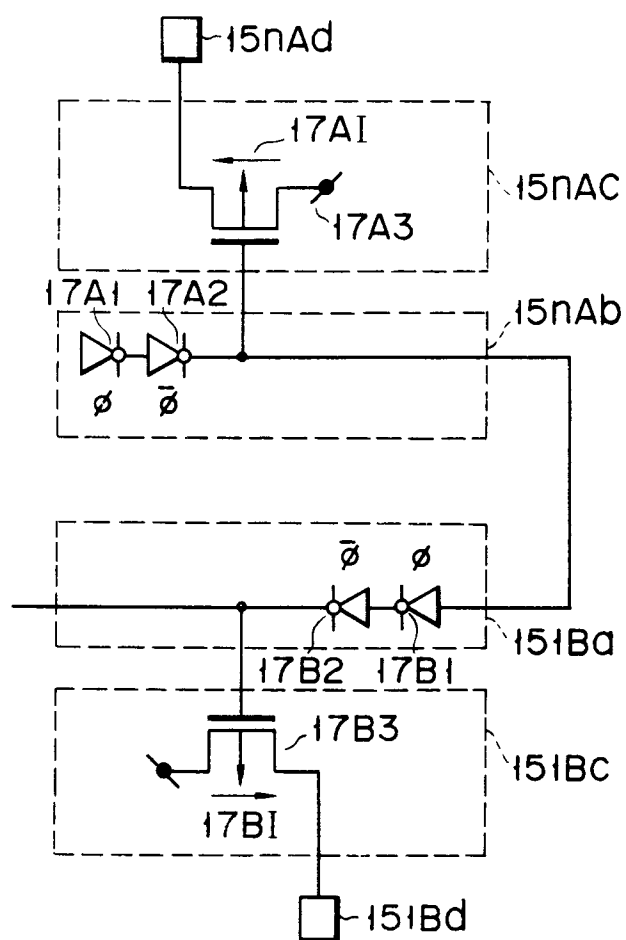


FIG. 3

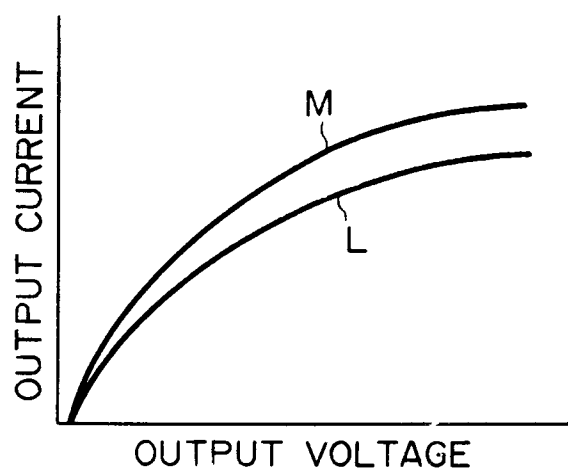


FIG. 4

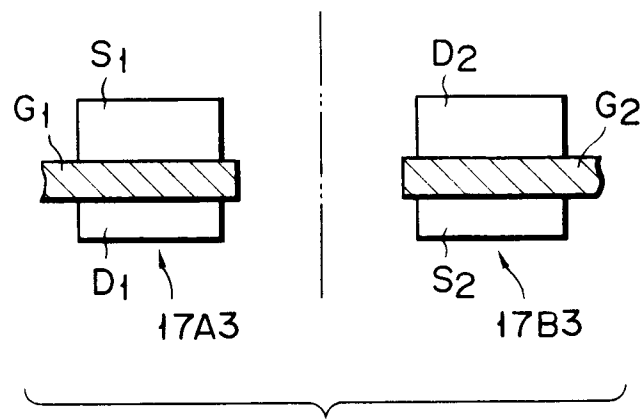


FIG. 5

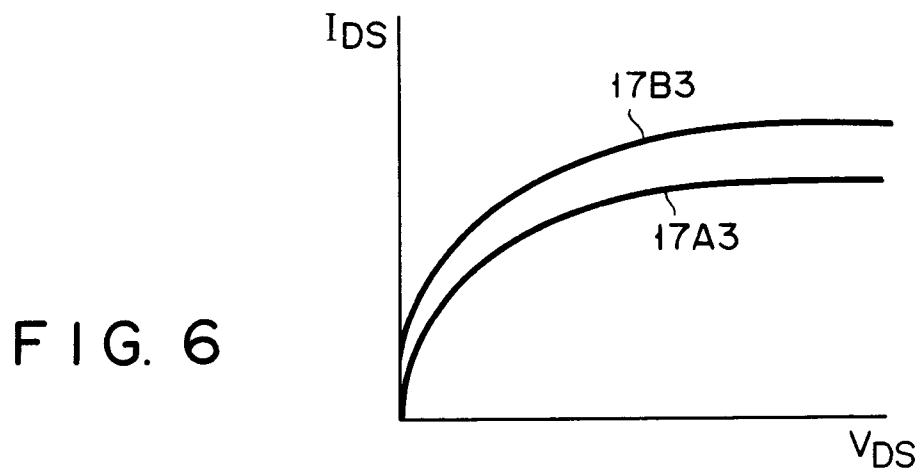


FIG. 6

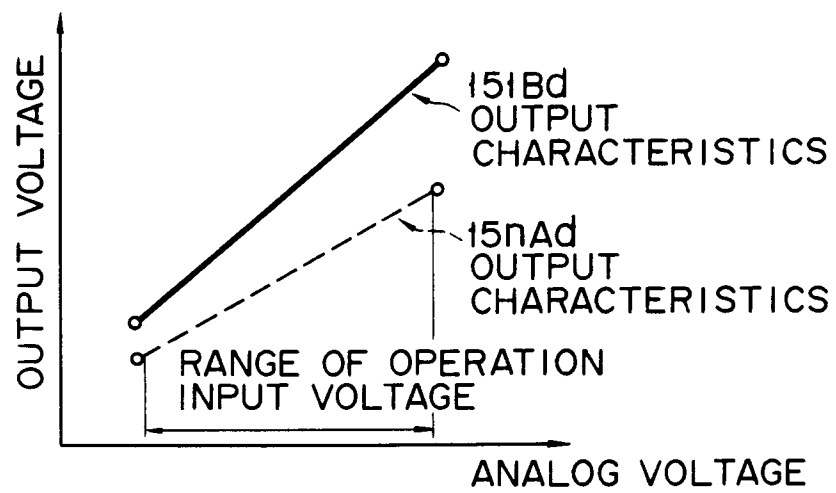


FIG. 8

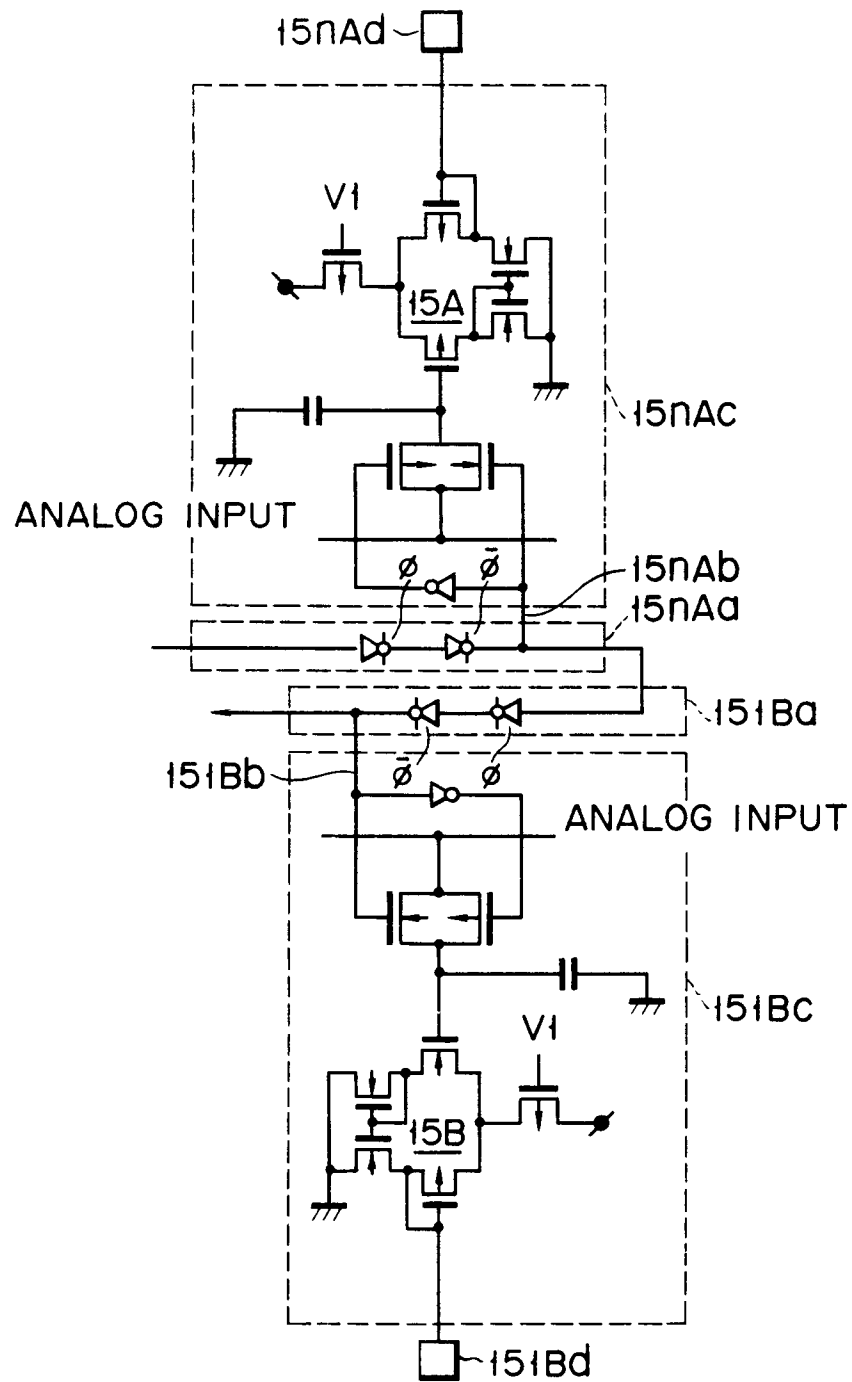


FIG. 7

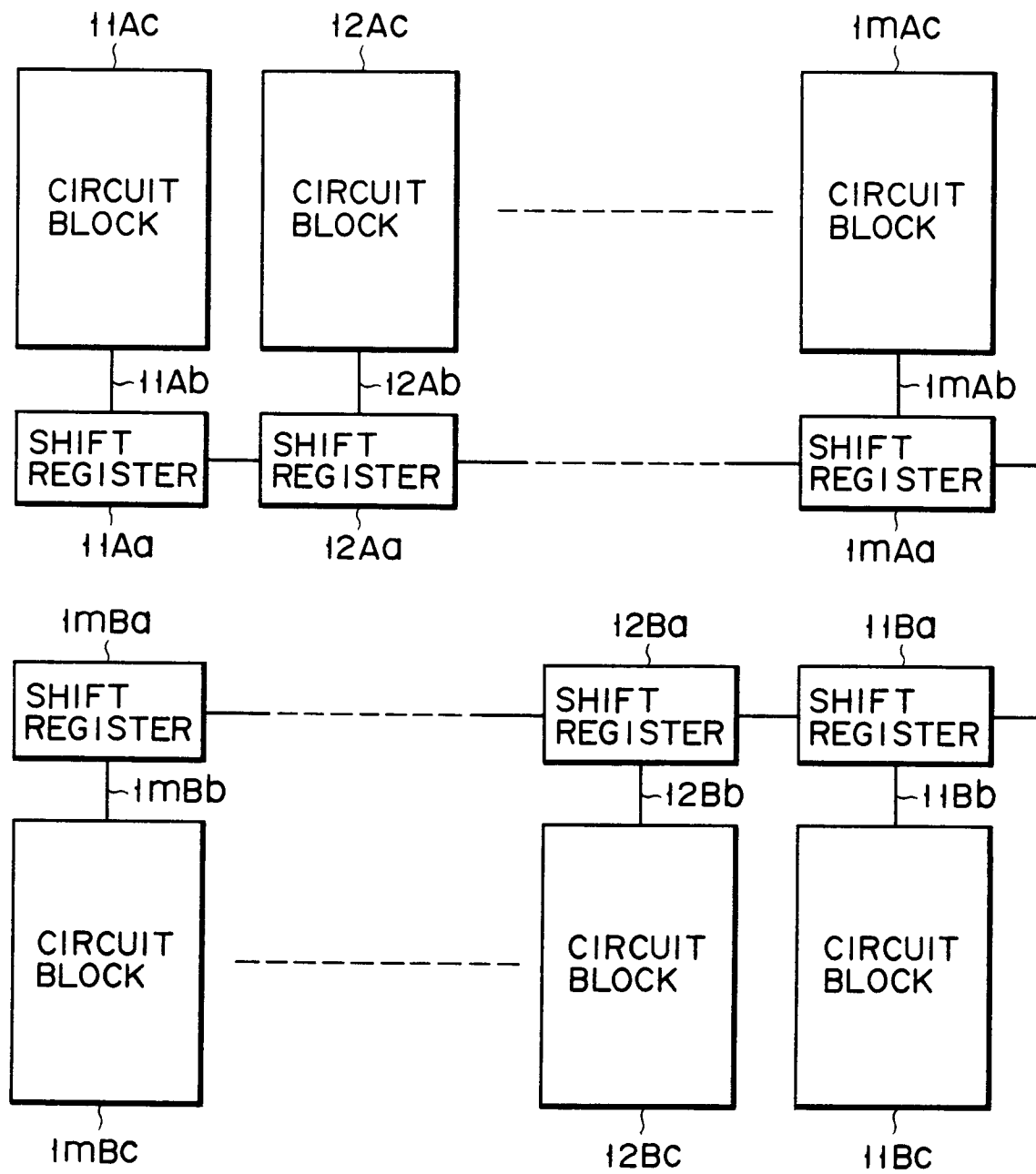


FIG. 9

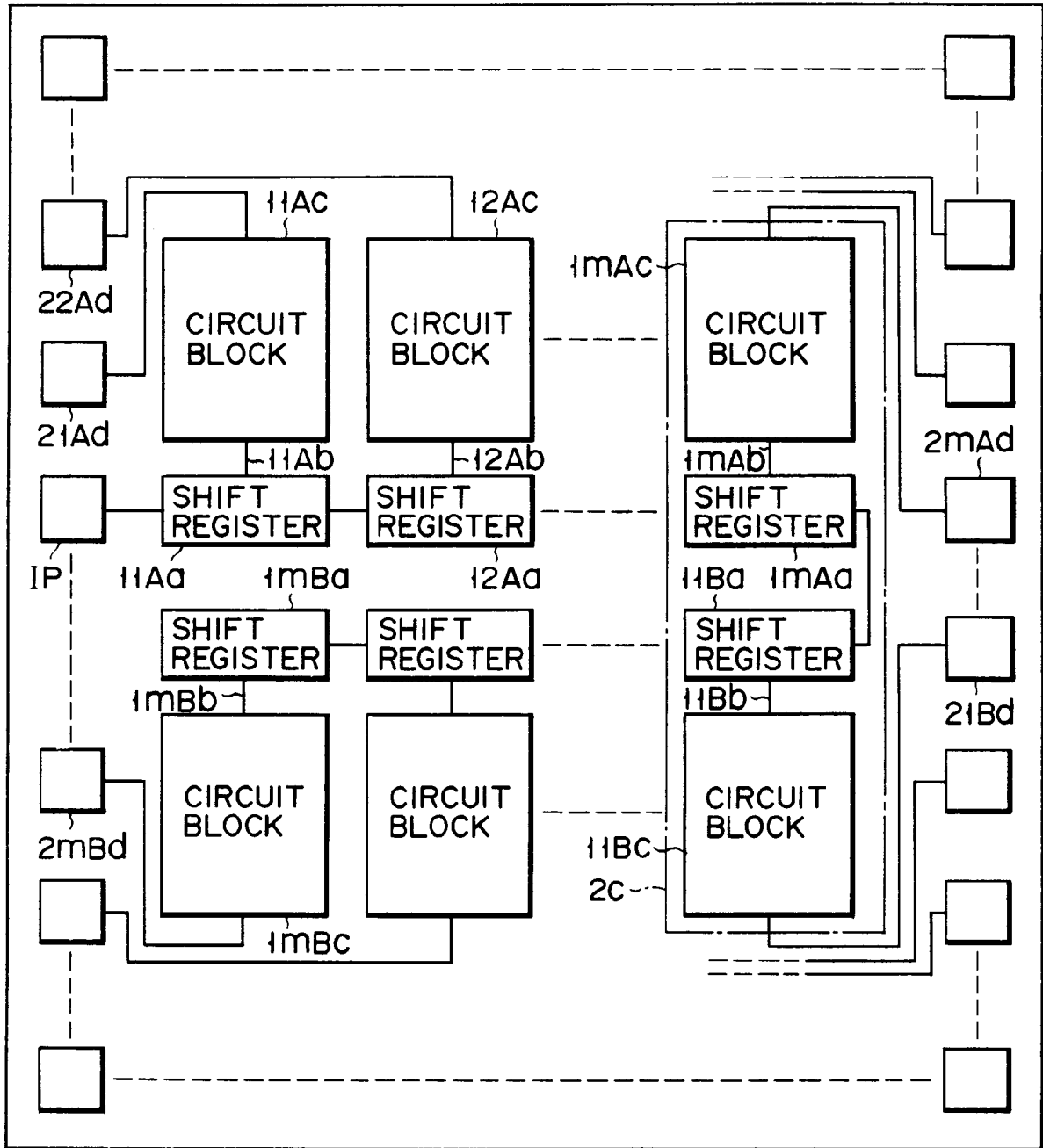
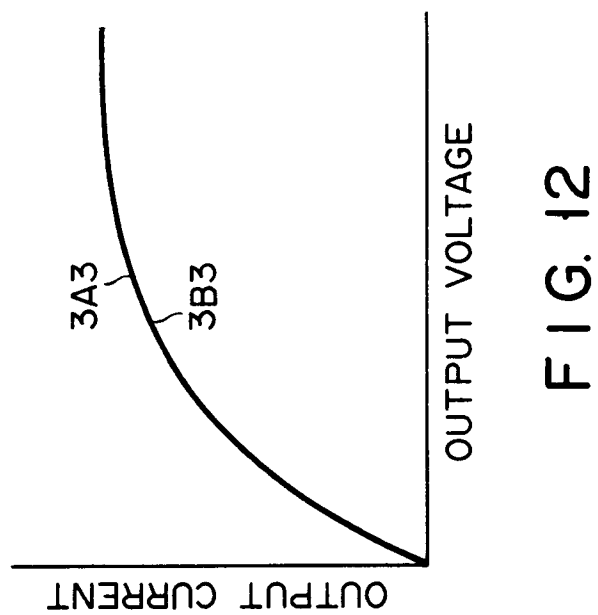
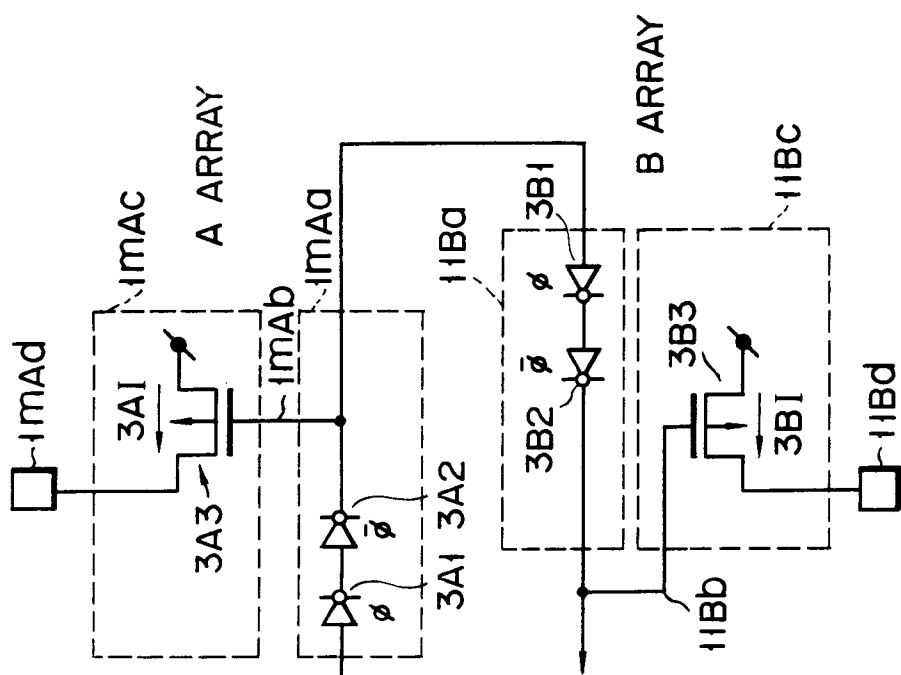


FIG. 10



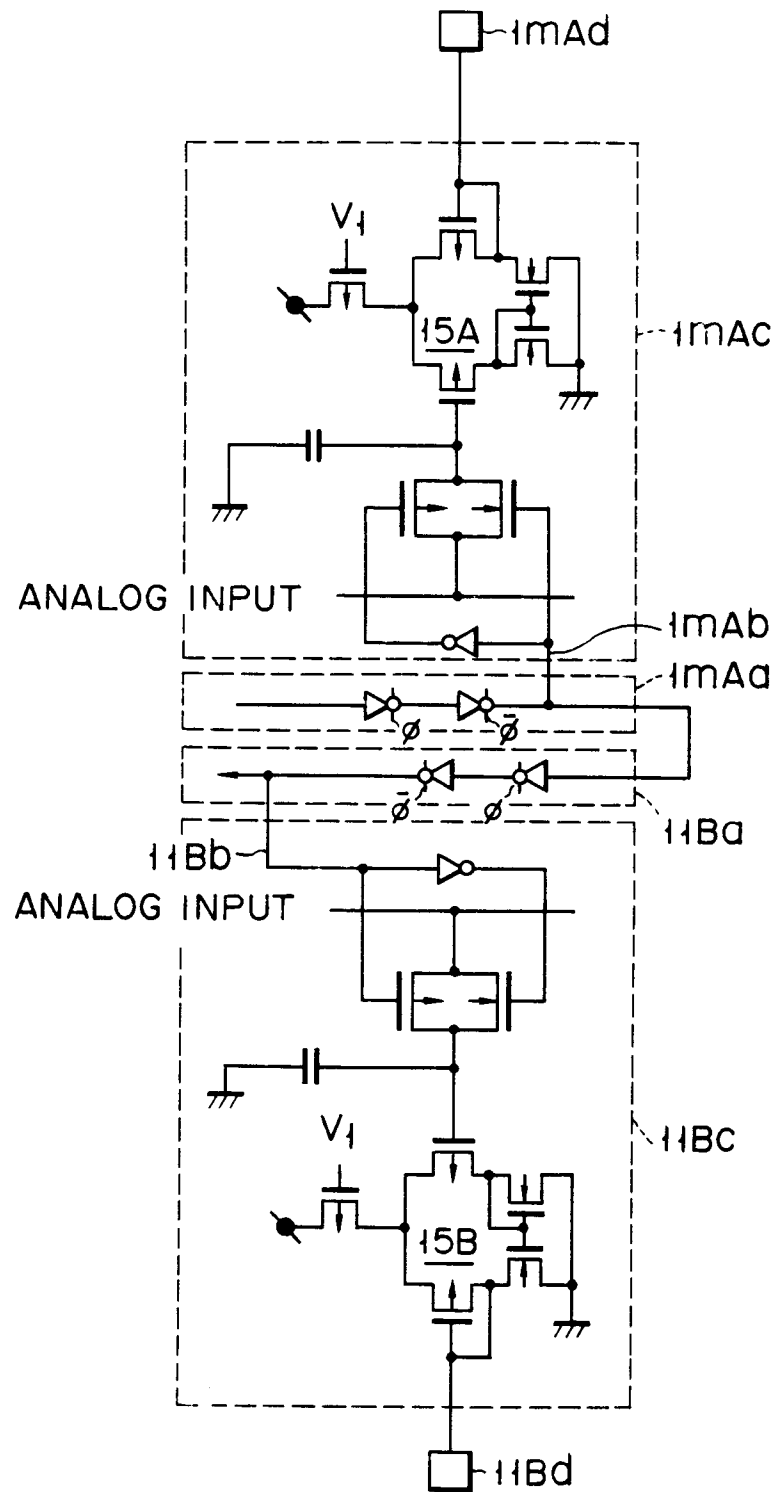


FIG. 13

FIG. 14

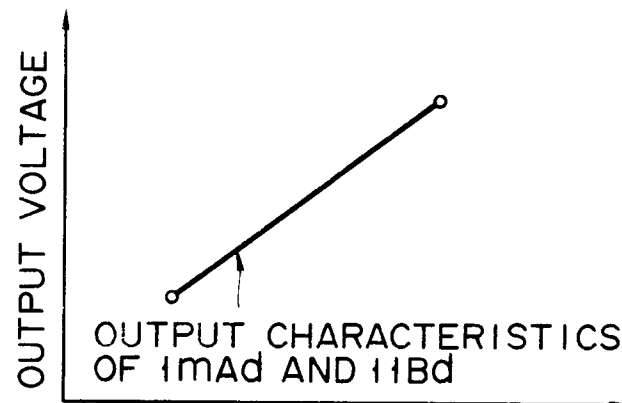


FIG. 15

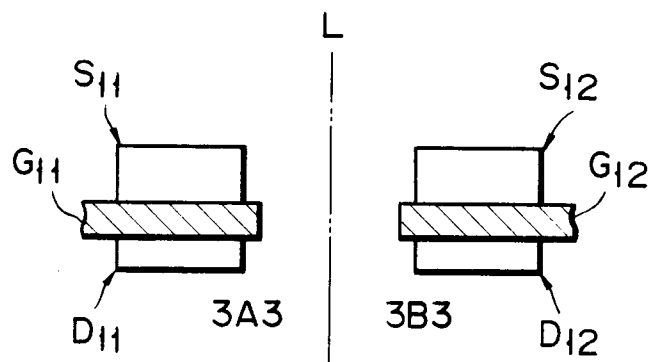


FIG. 16

