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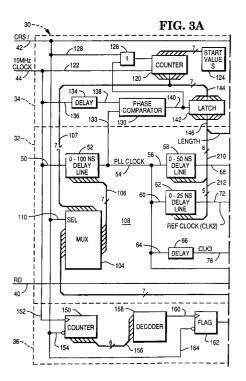
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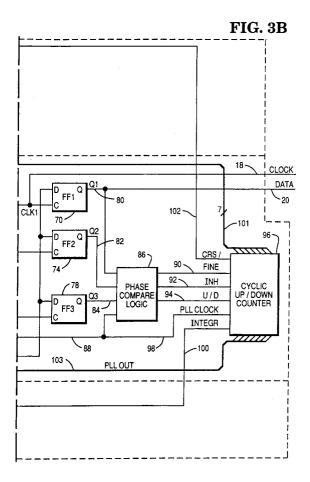
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54) Digital phase lock loop decoder.

(57) A digital phase lock loop decoder for decoding Manchester encoded data includes a controllable delay line (52) which provides a PLL CLOCK signal, which is delayed in respective further delay lines (58,62) and a compensating delay (66), to provide three phased clock signals (CLK1,CLK2,CLK3) defining a window for sampling the incoming data signal (RD). The sampled signals are applied to phase compare logic (86) which provides control signals for a counter (96), in dependence on the samples in the current and previous windows. The 7-bit counter output is fed back to control the phase of the controllable delay line (52) such that the central phased clock signal (CLK2) coincides with the mid-bit data transition. When data is not being received a delay correction section (34) continuously updates a compensating value which compensates for delay variations and is stored in a latch (142) for use during data reception.







EUROPEAN SEARCH REPORT

Application Number EP 90 31 1758

	Citation of document with indication	. where appropriate.	Relevant	CLASSIFICATION OF THE	
Category	of relevant passages	,or o appropriates	to claim	APPLICATION (Int.Cl.5)	
D,A	US-A-4 584 695 (WONG ET * column 3, line 40 - co figure 5 *		1-12	H03M5/12 H03L7/08 H04L7/033	
A	EP-A-O 317 159 (AMERICAN TELEGRAPH COMPANY) * page 3, line 4 - line * page 5, line 58 *		1,6,12		
A	US-A-4 789 996 (BUTCHER) * claim 1; figure 3 *		1,2		
A	US-A-4 788 605 (SPIESMAN * claim 1 *	ET AL.)	1		
A	EP-A-0 240 232 (HEWLETT- * column 4, line 40 - co		1		
				TECHNICAL FIELDS SEARCHED (Int.Cl.5)	
				HO3M	
				H04L H03L	
	The present search report has been draw	n up for all claims			
	Place of search	Date of completion of the search		Examiner	
	THE HAGUE	30 December 1993	Bru	inet, L	
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