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(54) **Determination of the error rate of data storage devices.**

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(56) References cited :
GB-A- 2 205 679
US-A- 4 574 234
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 1, June 1989, pages 420-421, New York, US; "Measurement scheme for detecting the reliability degradation of rotating memories which utilize an amplitude sampling data detection channel"

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Description

Technical Field of the Invention

The invention relates to the field of data storage devices, and more particularly to a method of determining the error rate of such a device.

Background of the Invention

Practitioners in the art of rotating magnetic memory devices, also known as disk drives, direct access storage devices, and DASD devices, have recognized for some time that one measure of the accuracy with which such a device has been manufactured is the bit error rate of the device.

One means of testing such a device is to record a known data pattern on the disks, and then read back the data pattern, in order to detect read errors. This procedure usually is very time consuming in that a read error usually does not occur until after a very large number of data patterns have been written to the disk(s) and then read back. For example, this classical testing technique requires that the quantity of data read back from the disk(s) be greater than the reciprocal of the error rate of the disk drive being tested.

As a result, others have attempted to shorten the time that is required to obtain a measure of a disk drive's error rate.

United States Patent 4,394,695 is an example. This patent relates to the evaluation of the bit error rate of magnetic recording systems by providing a window generating means that is responsive to the raw data that is read back from the magnetic recording media. This window generating means operates to provide a plurality of data windows, each of a different width (the different data windows in the patent being simulated by providing a plurality of raw data delays). The position of the data is compared to the edges of this plurality of windows. Data that falls outside of a window is counted as an error, and is accumulated in a counter for that particular window.

A well known technique for evaluating a magnetic recording system is the window margin test. In this test, data is read, and the overall bit distribution within a clock defined data window is measured. United States Patent 4,578,721 describes this type of a test, and also describes the injection of noise into the drive, for the purpose of monitoring the bits that then fall outside the window, or in the alternative, the narrowing of the window size to insure that errors are not later encountered in the drive's operating environment, when a full length window is used. The patent offers an improvement for noise and media defect detection, wherein data is first delayed toward one edge of the window until errors are detected. The data is then advanced 5% toward the centre of the window from its failure point. Noise or media defects will thereafter cause an error.

The above mentioned prior means of determining signal detection parameter margins in storage devices all deal with signal channels employing peak detection. In peak detection signal channels, a read signal pulse is compared to a pair of adjacent read clock pulses, also referred to as a data detection window. Generally in all of these techniques, a measured distance between the data pulses and an edge of the data window is noted, and, based upon this measured distance, some form of an algorithmic means is used to predict at what data rate read data errors will occur. These prior techniques have been used as manufacturing qualifying tools, for example.

IBM Technical Disclosure bulletin, vol.32 No 1, June 1989 further describes a prior art technique for determining the error rate of rotating memory devices having amplitude sampling detection signal channels, i.e. channels wherein the amplitude of an analog read signal is sampled at reoccurring clock intervals, in order to detect the binary data that was read back from a disk for each clock interval.

Disclosure of the Invention

The present invention seeks to provide an improved method whereby the data error rate of data storage devices, employing amplitude detection, may be predicted.

Accordingly there is provided a method for determining the data error rate of a data storage device of the kind having a record medium on which data has been written, and amplitude detection circuit means for detecting said data upon reading the same back from said medium, said detection circuit means including data clock means, wherein the method comprises the steps of,

A - reading said data back from said medium, to thereby generate an analog signal that is representative of said data,

B - sampling the amplitude of said analog signal at a plurality of intervals of said data clock, to thereby produce a plurality of individual amplitude samples,

C - comparing each of said plurality of individual amplitude samples to at least one reference amplitude, and generating a plurality of difference values as a result thereof, the method being characterised by the steps of:

D - value segregating said plurality of difference values, and storing a count of the number of each of said difference values, and

E - translating said stored count of difference values into a measure of the data error rate of said data storage device.

In another aspect of the invention, there is provided a data storage device having a record medium comprising;

write channel means for writing amplitude encoded data onto said medium,

read channel means for reading said written data back from said medium, and for generating an analog read signal as a result thereof,

analog to digital convertor means having an output, and having an input connected to receive said analog read signal,

clock means connected in controlling relation to said analog to digital convertor means, and operable to cause said analog to digital convertor means to provide at said output a sample digital amplitude at predetermined intervals of said clock means,

amplitude sensitive data decoding means connected to the output of said analog to digital convertor means,

read error function means connected to the output of said analog to digital convertor, and operable to compare said sample digital amplitudes at said predetermined intervals of said clock means to expected digital amplitudes for said samples, to thereby generate a digital difference amplitude for each of said sample digital amplitudes, characterised in that:

memory means for segregating said digital difference amplitudes in accordance with the different magnitudes thereof, and

means for addressing said memory means and for providing output display means depicting a frequency histogram of said segregated digital difference magnitudes.

In a preferred embodiment, the data storage device is a rotating data storage device and preferably a magnetic disk drive wherein the record medium is a magnetic disk.

Without limitation thereto, embodiments of the invention will be described with reference to partial response (PR) signalling techniques that utilizes amplitude detection of the analog read back data signal. More specifically, a read signal channel operating in the mode class IV partial response (PRIV) coding technique will be described. The specific form of PRIV to be described is of the partial response maximum likelihood (PRML) type.

Amplitude detection techniques, of which PR is an example, do not allow the use of the above described prior testing techniques, for example window margin testing, because the position of an analog read signal peak, in relation to the edges of a data window, is of no significance in amplitude detection devices, which devices depend upon the amplitude of the analog signal at a clock interval as a means of detecting the binary data that was previously written at that clock interval.

While the above forms of partial response data encoding/decoding are well known in the art, copending and commonly assigned United States patent application Serial Number 07/258,937 by E. A. Cunningham et al, and entitled Clocking Method and Apparatus for use With Partial Response Coded Binary Data, is incorporated herein by reference, both for its background teaching and for its teaching of one way in which a data clock may be generated from the analog read signal that is provided by reading PRIV encoded data back from a disk.

In accordance with the invention, a pattern of data, preferably a plurality of binary bits, is first written on the disk of the drive being tested. This data is then read back from the disk. The amplitude of the incoming analog read signal is then sampled at reoccurring clock intervals. In a preferred embodiment, the analog amplitude of each sample is digitized. This sample amplitude is then compared to reference amplitude values that are expected to be received for each binary bit that was recorded on the disk. For example, the digitized read signal is then compared to digital values that are expected to be received for each binary bit that was recorded on the disk.

This comparison provides a difference value for each binary bit that was stored on the disk. Like magnitude difference values are stored in one of a plurality of buffers or registers. The count content of this plurality of buffers provides a histogram depicting the distribution of the like magnitude difference values. This relative amplitude histogram provides a output means for determining the bit error rate of the disk drive being tested, i.e. the shape of the histogram provides a measure of the error rate pass/fail status of the disk drive being tested.

In one preferred arrangement, the circuit means for accomplishing the above defined testing of a disk drive may be placed within each disk drive, to form an integral part thereof. In this way, the circuit means may be periodically enabled to self test the error rate of the disk drive. These periodic self test results can then be logged in a memory means, thus enabling the user to monitor disk drive performance with use, ageing, and the like.

As a further preferred feature, the construction and arrangement of the invention can be used to evaluate anticipated circuit changes and the like to a disk drive. By comparing the measured data error rate both before and after incorporation of the circuit changes into the disk drive, it can be quickly determined if an anticipated change will improve or degrade the performance of the disk drive's data channel.

Brief Description of the Drawings

FIG. 1 shows a schematic of the write/read channel circuit means of an exemplary disk drive having an amplitude signal detection means in the read channel, wherein the read channel's analog read signal is digitized, and then connected to an error rate detection circuit means in accordance with the invention,

FIG. 2 shows an exemplary analog read signal that is generated by the read channel circuit means of FIG. 1, showing the digitized samples that are generated therefrom by the analog to digital convertor of FIG. 1 at a number of clock pulse intervals or times, and showing a comparison of the digitized samples to expected digital values of the same, to thereby generate difference values corresponding to each clock pulse,

FIG. 3 shows an embodiment of the 16x16 bit RAM shown in FIG. 1, and shows how the difference values of FIG. 2 operate to address storage locations of the RAM, thereby causing a RAM storage location (i.e. a register of FIG. 3) to increment by one count upon the occasion of each individual addressing event, and

FIG. 4 shows a representative histogram of the type that is provided by the counts that are stored in the registers of FIG. 3 as a result of the testing of a disk drive having amplitude signal detection means in the read channel thereof.

Detailed Description of the Invention

The present invention finds utility when used with any type of a data storage device that provides amplitude sampling data detection. In accordance with the invention, the amplitude of a read back signal is sampled at data clock intervals. These sample signals are then compared to expected signals that are representative of the data that was originally recorded on the disk (for example), to thereby provide difference signals. The resulting difference signals are then magnitude segregated and stored for use in providing a histogram that is a measure of the disk drive's read error rate.

The invention will be described with reference to a disk drive that contains a write/read channel means having partial response maximum likelihood (PRML) detection. However, the invention as claimed is not limited thereto.

Reference may be made to US application SN. 07/258,937, above mentioned, for a general description of partial response coding techniques. In summary, this coding technique is a form of pulse amplitude modulation that is used to convey digital information, wherein the effect of a known amount of intersymbol magnetic recording interference can be eliminated, because the interference is of a known quantity.

FIG. 1 is a schematic showing of the write/read channel means of an exemplary disk drive having an partial response IV (PRIV) maximum likelihood coding. This figure also shows an error rate measuring/detection circuit means in accordance with the invention.

Class IV partial response coding (PRIV) is a three signal level form of partial response coding. Advance amplitude sampling coding and detection techniques, of which PRIV is an example, intentionally provide intersymbol interference. As a result, peak amplitude signal detection cannot be used to detect the binary content of the analog read back signal that is generated when such coded data is read back from the disk.

FIG. 2 shows an exemplary analog read back signal 20, as it is generated by the disk drive read channel means of FIG. 1.

The analog read signal that is derived from reading a magnetic track that has been recorded (i.e. written) by the use of the PRIV technique provides three critical signal amplitudes, labeled "Zero", "+A" and "-A" in FIG. 2. As is well known to those skilled in the art, the values "+A" and "-A" comprises detection thresholds that enable the PRIV circuit means to detect the reading of binary 1's.

Note that FIG. 2 also contains the offset decimal values "32", "48" and "16", wherein the value "32" is associated with the above mentioned value "Zero". The decimal values "32", "48" and "16" represent the values of an offset binary numbering system whose values are provided by the output of analog to digital convertor (A/D) 19 shown in FIG. 1, as will be explained.

Note also that PRIV analog read signal 20 of FIG. 2 contains positive and negative peak signal amplitudes

that are caused by reading recorded magnetic transitions from the disk. However, in partial response coding, the binary content of the recorded data is not contained in the time position of these peaks, as it is in the peak detection recording technology discussed above. For example, in PRIV coding, the presence of a "Zero" signal amplitude at a clock interval represents (i.e. is decoded as) a binary "0", and the presence of either a "+A" of a "-A" threshold amplitude at a clock interval represents a binary "1".

By way of a summary description of the invention, the top row of FIG. 2 contains a sequence of clock pulse times, labeled clock pulses 1 through 15. At clock pulse 2, the amplitude of analog read signal 20 is decimal 50, see the row labeled "A/D output". Since the amplitude of signal 20 is above "+A" at clock time 2, the read signal sample amplitude of 50 is decoded as a binary "1" data bit by the disk drive's read channel. In accordance with operation of the invention, the expected value of decimal 48, see the row labeled "Expected Output", is compared to the actual value of signal 20, i.e. to the value 50, to thereby derive a difference value of +2 (i.e. the signal value was two units higher than was expected at clock pulse 2 for the reading of a binary "1").

In like manner, a difference value is provided for each clock pulse during the reading of the recorded data from the disk(s) of the disk drive being tested, see the row labeled "Difference". The magnitude segregated collection of these difference values then form a testing means, such the histogram of FIG. 4, enabling the failure rate of the disk drive to be determined. Note that this test can be performed without a failure to properly read binary recorded data actually occurring. That is, the expected A/D output values may all fall within values allowing proper decoding of binary "1" and "0", and yet in accordance with the invention, the history represented by the difference row of FIG. 2, and the histogram of FIG. 4, enables a failure rate of the disk drive to be determined with great accuracy.

The output data of the present invention may, for example, comprise go/no-go test wherein rejected disk drives from a manufacturing process may be quickly determined.

FIG. 1 is a schematic showing of the write channel and the read channel of an exemplary disk drive having a signal amplitude coding means in the write channel, and having a signal amplitude decoding means in the read channel, wherein the read channel's analog read signal is digitized, and the digitized values are connected to an error rate detection circuit means in accordance with the invention.

With reference to FIG. 1, the write portion 10 of a magnetic transducer 13 is first used to write a number of disk tracks with random input binary data, as is provided to the write channel by way of input conductor 11. The form that data 11 takes is not critical to the invention. However, in an embodiment of the invention it has been found advantageous to write random binary data. Data 11 is encoded to provide for amplitude sampling data detection during the subsequent reading back of the disk tracks. For example, partial response maximum likelihood encoding network 12 is used to encode binary data 11 before the data is written to the disk tracks.

While the construction and arrangement of the write and read channels of FIG. 1 are not to be taken as a limitation on the invention, these two channels both include an arm electronics network (RE) network 15. As is well known by those skilled in the art, network 15 provides a variety of electronic functions, including for example amplification of the write/read signal.

Once the disk is written, the read channel, and read portion 14 of head 13, is used to read back the written encoded data. The read channel of FIG. 1 includes AE network 15, an automatic gain control network 16 and an equalization network 17. As a result of the operation of network means 15-17, an analog read signal is present on conductor 18. This analog signal is connected to the input of A/D convertor 19. By way of example, analog signal 20 of FIG. 2 is present on conductor 18.

In the decoding of analog read signal 20, the analog values or amplitudes of signal 20 are sampled at clock times or intervals of a clock that is provided to A/D convertor 19 by way of conductor 21′ shown in FIG. 1. The frequency of this clock may be synchronized to read back signal 20 as is described in above mentioned application SN. 07/258,937, if desired.

Again without limitation thereto, the disk drive read channel shown in FIG. 1 includes a maximum likelihood detector network 21 (also known in the art as an ML detector or a Verterbi detector). The basic function of detector 21 is to decode the three significant A/D output values "Zero", "+A" and "-A" of FIG. 2 into binary "1" and "0" at each pulse of clock 21.

In the exemplary disk drive of FIG. 1, a decode network 22 is also provided. The binary output 23 of network 22 comprises the original binary input 11 that was presented to the write channel during the writing of data to the disk drive.

Dotted line conductor 30 connects the digitized sample signal output 24 of A/D convertor 19 (i.e. the row labeled "A/D output" in FIG. 2) to an error rate detection circuit means in accordance with the invention. Conductor 30 is dotted to indicate that the circuit means of the invention may be connected to conductor 24 only during the testing of the disk drive, or, alternatively, the circuit means of the invention may be formed as an integral portion of each disk drive, as the disk drive is manufactured.

In this explanation, but without limitation thereto, the output of A/D convertor 19 comprises a 6-bit binary

word whose minimum value is "000000" (i.e. decimal 0) and whose maximum value is "111111" (i.e. decimal 63), as is shown in the following TABLES A-D. These decimal values, and more specifically the decimal values of 0, 16, 32, 48 and 64, comprise the vertical axis of FIG. 2. The pulses of clock 21 comprises the horizontal axis of FIG. 2.

Note that the decimal values 16, 32 and 48 are significant values in that these values are the three expected values against which the digitized sample magnitudes of signal 20 are compared at the time of each clock pulse.

In FIG. 2, analog read signal 20 is shown with the mid range A/D convertor output value of 32 as a base line for signal 20, i.e. the zero value of signal 20 is located on the horizontal value line 32 of FIG. 2. As a result, the various digitized signal values that comprise the output of A/D convertor 19 provide an offset binary numbering system by which the amplitude of analog read back signal 20 is determined.

As will be appreciated by those skilled in the art, many different means may be provided for determining a difference value for each sample of analog read back signal 20 within the spirit and scope of the invention.

In a preferred embodiment of the invention, the 6-bit output of A/D convertor 19 is applied to the input of error function network 31. Network 31 operates to determine the difference between (1) the expected baseline value of 32 for analog signal 20, (2) the expected negative value of 16 for signal 20, or (3) the expected positive value of 32 for signal 20, at each of the respective pulses of clock 21.

An example of the first above mentioned difference occurs at clock pulse 1. At this clock pulse, the 6-bit A/D output value of 011110 (decimal 30) is correctly decoded as a binary "0". The expected value is, however, 100000 (decimal 32). As a result, error function network 31 generates a difference value of 1010 (corresponding to decimal +2) on its output conductor 32.

An example of the second above mentioned difference occurs at clock pulse 6. At this clock pulse, the 6-bit A/D output value of 001101 (decimal 13) is correctly decoded as a binary "1". The expected value is, however, 010000 (decimal 16). As a result, error function network 31 generates a difference value of 0101 (corresponding to decimal -3) on its output conductor 32.

The function of error function network 31 is shown in the following TABLES A-D, as will be explained in detail. In summary, error function network 31 operates to map from the 64 different 6-bit input values that can be provided by output 24 of A/D convertor 19, to 16 different addressable storage locations within the 16x16 bit RAM shown in FIG. 1. Stated differently, error function network 31 operates to convert a 6-bit input on conductor 30 to a 4-bit output on conductor 32.

In this manner, error magnitudes are segregated, and counts of each individual error magnitude are accumulated in individual storage locations of RAM 33, in accordance with the frequency with which each addressable location has been addressed during the testing of a disk drive. RAM 33 is constructed and arranged so that the count stored in an addressable location of the RAM is incremented by one count for each addressing event of that storage location. FIG. 3 shows an embodiment of RAM 33 which includes 16 registers or counters, as will be described.

In the FIG. 1 embodiment of the invention, but without limitation thereto, error function network 31 has the effect of bracketing 16 sample error slots about each of the expected sample values of decimal 48, 32 and 16, which values are shown on the vertical axis of FIG. 2. Each of these slots corresponding to one of the sixteen different storage locations of RAM 33. This effectively puts error zones, represented by the storage locations, on each side of these expected values, with the addressing of storage location "0" representing a no error condition in a sample's magnitude. Thus the above mentioned mapping function measures the difference between magnitude of a received sample value and the expected magnitude value for the sample, and causes the measured difference magnitude to be logged as one event into the corresponding storage location, i.e. a measured difference value of +3 is logged into the +3 storage location, as will be described.

FIG. 4 is a representative histogram of the type that is provided by the various count magnitudes that are stored in the 16 addressable locations of RAM 33 after a disk drive has been tested in accordance with the invention. The horizontal axis of this figure presents the sixteen storage locations, starting with a storage location "-8" on at the left end of the horizontal axis, and progressing through storage location "0", to storage location "+7" at the right end of the horizontal axis. The vertical axis presents the relative count magnitudes that are stored in each storage location at the end of a test.

As will be apparent from a later consideration of TABLES A-D, storage location "-8" is addressed whenever the 4-bit output of error function network 31 comprises "0000", storage location "0" is addressed whenever the 4-bit output of error function network 31 comprises "1000", and storage location "+7" is addressed whenever the 4-bit output of error function network 31 comprises "1111".

By way of example, the histogram of FIG. 4 may be generated by reading out the contents of the sixteen storage locations of RAM 33 after the testing of the disk drive. Controller 36, error address register 34 and error data register 35 are provided for this purpose. Controller 36 can then be used to drive display such as a

cathode ray tube or a printer 37. In addition, controller 36 may provide a go/no-go output by way of pass/fail indicator or output means 38.

FIG. 3 shows an embodiment of the 16x16 bit PAM 33 of FIG. 1 wherein the sixteen addressable storage locations of RAM 33 are formed by an address latch 49, a 16x1 multiplexer 50, and a bank 51 of sixteen individual registers, each register being N bit positions in length (in FIG. 1, N = 16).

The input to latch 49 comprises the 4-bit binary output word 32 from error function network 31, shown in FIG. 1. This input 32 includes the "difference" value row shown in FIG. 2. The 4-bit word values that are possible at input 32 cover the range of the sixteen binary values from "1111" to "0000", and also covers a correspondingly defined 16-slot decimal range that extends from a decimal value of "+7" to a decimal value of "-8", as is defined by, and as will be described relative to, TABLES A-D.

The defined relationship between this binary word range and this decimal slot range is shown in FIG. 3 by way of a 4-bit address that is associated with each of the sixteen registers 51, wherein the sixteen individual registers are identified as "+7", "+6" ------ "-7" and "-8". This convention is also used in the following TABLES A-D.

As testing of the disk drive progresses, a 4-bit binary number within the above range of numbers is presented as an input TO latch 49 at the time of the occurrence of each pulse of clock 21. This number is retained in latch 49 until the time of occurrence of the next clock pulse.

Latch 49 presents this 4-bit number to multiplexer 50. Multiplexer 50 then operates to address one of the sixteen registers 51, and clock pulse 21 increments the content of that register by one count.

By way of further explanation, assume that register "+1" contains a count of "M", and that the next 4-bit difference word that is applied to the input of latch 49 is "1001" (for example, the difference row value of +1 that is measured at clock pulse 3 in FIG. 2). This event will cause the content of register "+1" to increment to the value "M+1". In this way, the measured difference values are magnitude segregated, and like magnitude difference values are counted.

After the disk drive has been tested, a microprocessor, such as controller 36 of FIG. 1, can be used to address the individual registers 51 in order to generate an output such as at 37 and/or 38 of FIG. 1.

The functioning of error function network 31 is shown in the following tables. In summary, error function network 31 maps from 64 different 6-bit input values, as is provided by the output of A/D convertor 19, to 16 different addressable locations within RAM 33 of FIG. 1, or to sixteen different addressable registers of FIG. 3. In this manner, counts are accumulated in each storage location or register, in accordance with the frequency with which each addressable location or register has been addressed during the testing of a disk drive.

Error function network 31 has the effect of bracketing a 16 sample count or slot region about each of the expected sample values of decimal 48, 32 and 16 shown on the vertical axis of FIG. 2, each of these slots corresponding to one of the sixteen different storage locations or registers. This effectively puts error bars or zones, represented by the storage locations or registers, on each side of these expected values, with the addressing of storage location or register "0" representing a no error condition in a sample's magnitude. Thus the above mentioned mapping function measures the difference between magnitude of a received sample value and the expected magnitude value for the sample, and causes the measured difference magnitude to be logged as one event into the corresponding storage location or register, i.e. a measured difference value of +3 is logged into the +3 register of FIG. 3.

With reference to the following tables,

(1) TABLE A shows the operation of error function network 31 for the 6-bit outputs of A/D convertor 19 in the range of binary values from 111111 to 110000, i.e. in the range of values of the FIG. 2 analog read signal that fall within the decimal values from 64 to 48, as shown on the vertical axis of FIG. 2,

(2) TABLE B shows the operation of error function network 31 for the 6-bit outputs of A/D convertor 19 in the range of binary values from 101111 to 100000, i.e. the range of values of the FIG. 2 analog read signal that fall within the decimal values from 47 to 32, as shown on the vertical axis of FIG. 2,

(3) TABLE C shows the operation of error network 31 for the 6-bit outputs of A/D convertor 19 in the range of binary values from 011111 to 010000, i.e. the range of values of the FIG. 2 analog read signal that fall within the decimal values from 31 to 16, as shown on the vertical axis of FIG. 2, and

(4) TABLE D shows the operation of error network 31 for the 6-bit outputs of A/D convertor 19 in the range of binary values from 001111 to 000000, i.e. the range of values of the FIG. 2 analog read signal that fall within the decimal values from 15 to 0, as shown on the vertical axis of FIG. 2.

In these four tables, the values that are within parentheses are the decimal equivalents of the binary numbers immediately adjacent thereto.

The column of the tables labeled "Register Incremented" refers to the register of FIG. 3 (sixteen registers, labeled "-8" through "+7" are provided in FIG. 3), whose number content is incremented by one count each time that error function network 31 generates the 4-bit address of the particular register. For example, each

time the output of A/D convertor 19 provides one of the three expected outputs upon the occurrence of a pulse of clock 21 (i.e. one of the decimal values 48, 32 or 16 of FIG. 2), error function network 31 generates the 4-bit address "1000", and register "0" is addressed and incremented by one count. After the disk drive has been tested, it is usual that the count contained in registers "0" and "-1" are the highest of all registers, and are approximately equal in value, as is shown in the example histogram of FIG. 4.

The column of the tables labeled "Register Incremented" also refers to the storage location of RAM 33 of FIG. 1 (sixteen storage locations are provided), whose number content is incremented by one count each time that error function network 31 generates the 4-bit address of the particular RAM storage location.

In these tables the exemplary A/D output values that are shown in FIG. 2 for clock pulses 1-15 are also shown in parentheses. This is done as an aid to understanding how these exemplary A/D output values cause specific storage locations or registers to increment by one count. For example, in TABLE C an A/D output of decimal 30 is shown, and as a result, the register "-2" of FIG. 3 is incremented by one count.

TABLE A

A/D Output	Error Function Output Address	Increment Register
111111 (63)	1111 (15)	+7
111110	.	.
111101	.	.
111100	.	.
111011	.	.
111010	.	.
111001	.	.
111000 (56)	1111 (15)	+7
110111 (55)	1111 (15)	+7
110110	1110	+6
110101	1101	+5
110100	1100	+4
110011	1011	+3
110010 (50)	1010	+2
110000 (49)	1010	+1
110000 (48)	1000	0

TABLE B

A/D Output	Error Function Output Address	Increment Register
101111 (47)	0111 (7)	-1
101110	0110	-2
101101	0101	-3
101100	0100	-4
101011	0011	-5
101010	0010	-6
101001	0001	-7
101000 (40)	0000 (0)	-8
100111 (39)	1111 (15)	+7
100110	1110	+6
100101	1101	+5
100100	1100	+4
100011	1011	+3
100010 (34)	1010	+2
100001	1010	+1
100000 (32)	1000	0

TABLE C

A/D Output	Error Function Output Address	Increment Register
011111 (31)	0111 (7)	-1
011110 (30)	0110	-2
011101	0101	-3
011100	0100	-4
011011	0011	-5
011010	0010	-6
011001	0001	-7
011000 (24)	0000 (0)	-8
010111 (23)	1111 (15)	+7
010110	1110	+6
010101	1101	+5
010100	1100	+4
010011	1011	+3
010010	1010	+2
010001	1010	+1
010000 (16)	1000	0

TABLE D

A/D Output	Error Function Output Address	Increment Register
001111 (15)	0111 (7)	-1
001110 (14)	0110	-2
001101 (13)	0101	-3
001100	0100	-4
001011	0011	-5
001010	0010	-6
001001	0001	-7
001000 (8)	0000 (0)	-8
000111 (7)	.	.
000110	.	.
000101	.	.
000100	.	.
000011	.	.
000010	.	.
000001	.	.
000000 (0)	0000	-8

FIG. 4 is a representative histogram of the type that is provided by the various count magnitudes that are stored in the sixteen storage locations of RAM 33 of FIG. 1, or in the sixteen registers of FIG. 3, after a disk drive has been tested in accordance with the invention. The horizontal axis of this figure presents the sixteen registers of FIG. 3, starting with register -8 on at the left end of the horizontal axis, and progressing through register 0, to register +7 at the right end of the horizontal axis. The vertical axis presents the relative count magnitudes that are stored in each register at the end of a test.

By way of example, the histogram of FIG. 4 may be generated by reading out the contents of the sixteen storage location of PAM 33, the sixteen registers shown in FIG. 3, after the testing of the disk drive, and then using this derived data to drive a display means such as a cathode ray tube or a printer 37 of FIG. 1.

In FIG. 4, the histogram is shown as being quite symmetrical about the count values that are stored in registers 0 and -1. While this is a typical case, it need not be so. Also note that in this exemplary case, no counts were stored in the four end registers -8, -7, +6 and +7. This situation is an indication that the tested disk drive will be able to sustain a fairly high data rate before read back errors begin to occur.

As an example of one use of the invention, a manufacturing specification for disk drives of a given type

may specify the minimum histogram dimension 90 and/or 91 that must exist in order for a disk drive to pass a manufacturing qualification test. Another approach to the use of a histogram in accordance with the invention is to extend the generally bell shaped curve, as at 92 and 93, in order to estimate at what data rate read errors will likely begin to occur. For example, a histogram such as is shown by dotted line 100 would likely indicate a failing disk drive, due to the flat slope exhibited by the two ends of the histogram curve.

Further utility for the invention is found when a testing means in accordance with the invention is incorporated within each disk drive that is manufactured. In this way, operation of the invention can be performed periodically during the life of the disk drive, perhaps as a portion of periodic maintenance procedures.

Claims

1. A method for determining the data error rate of a data storage device having a record medium on which data has been written, and having amplitude detection circuit means for detecting said data upon reading the same back from said medium, said detection circuit means including data clock means, the method comprising the steps of,

   A - reading said data back from said medium, to thereby generate an analog signal that is representative of said data,

   B - sampling the amplitude of said analog signal at a plurality of intervals of said data clock, to thereby produce a plurality of individual amplitude samples,

   C - comparing each of said plurality of individual amplitude samples to at least one reference amplitude, and generating a plurality of difference values as a result thereof, the method being characterised by the steps of:

   D - value segregating said plurality of difference values, and storing a count of the number of each of said difference values, and

   E - translating said stored count of difference values into a measure of the data error rate of said data storage device.

2. A method as claimed in claim 1 wherein step B includes the step of converting said plurality of individual analog amplitude samples into a plurality of individual digital amplitude samples, and

   wherein step C includes comparing each of said plurality of digital amplitude samples to an reference digital amplitude, and generating a plurality of digital difference values as a result thereof.

3. A method as claimed in claim 1 or claim 2 wherein said data storage device operates to write said data to said medium with said data encoded in accordance with a partial response coding technique, and wherein said amplitude detection circuit means operates to detect the data content of an analog partial response read back signal.

4. A method as claimed in any preceding claim including the steps of recording binary data on said record medium after said binary data has been encoded using a partial response coding technique, wherein step A comprises

   reading said coded binary data pattern back from said medium, to thereby generate a continuous analog signal that is representative of said coded binary data pattern, and wherein

   step C occurs prior to partial response decoding of the said coded binary data pattern that is generated in step A.

5. A method as claimed in any preceding claim wherein step D comprises the steps of

   providing a plurality of individually addressable storage locations, said storage locations being constructed and arranged to increment the stored count content thereof by one count for each address occurrence,

   generating the same storage address for all similar ones of said value segregated difference values, and

   utilizing said generated storage addresses to address said storage locations, to thereby store a count of the number of occurrences of said similar ones of said value segregated difference values.

6. A method as claimed in any preceding claim wherein step D includes the generation of a histogram of said stored count of value segregated difference values.

7. A Data Storage device comprising:

a record medium,

write channel means for writing amplitude encoded data onto said medium,

read channel means for reading said written data back from said medium, and for generating an analog read signal as a result thereof,

analog to digital convertor means (19) having an output, and having an input connected to receive said analog read signal,

clock means (21') connected in controlling relation to said analog to digital convertor means, and operable to cause said analog to digital convertor means to provide at said output a sample digital amplitude at predetermined intervals of said clock means,

amplitude sensitive data decoding means (21) connected to the output of said analog to digital convertor means,

read error function means (31) connected to the output of said analog to digital convertor, and operable to compare said sample digital amplitudes at said predetermined intervals of said clock means to expected digital amplitudes for said samples, to thereby generate a digital difference amplitude for each of said sample digital amplitudes, characterised in that it further includes:

memory means (33) for segregating said digital difference amplitudes in accordance with the different magnitudes thereof, and

means (36) for addressing said memory means and for providing output display means depicting a frequency histogram of said segregated digital difference magnitudes.

8. A data storage device as claimed in claim 7 wherein said memory means value segregates said digital difference magnitudes, and stores a count of the number of occurrences of each individual one of said digital difference magnitudes, and wherein said means for addressing said memory means translates said stored count of individual difference magnitudes into a measure of the read error rate of said data storage device.

9. A data storage device as claimed in claim 7 or claim 8 wherein said memory means comprises counter means (51) having a plurality of addressable locations, the address of each location of said counter means corresponding to a different individual digital difference magnitude, and wherein the content of each of said addressable locations increments one count for each addressing event.

10. A data storage device as claimed in any of claims 7 to 9, wherein said write channel means operates to write data to said medium with said data encoded in accordance with a partial response coding technique, and wherein said read channel means operates to amplitude sample detect the data content of an analog partial response read back signal.

Patentansprüche

1. Ein Verfahren zur Bestimmung der Datenfehlerrate einer Datenspeichervorrichtung mit einem Speichermedium, auf dem Daten geschrieben sind, und einem Amplitudenerkennungsschaltmittel zur Erkennung der genannten Daten beim Einlesen derselben vom genannten Medium, wobei das genannte Erkennungsschaltmittel ein Datentaktmittel umfaßt, bei dem das Verfahren die folgenden Schritte umfaßt:

A - Einlesen der genannten Daten vom genannten Medium, um dadurch ein analoges Signal zu erzeugen, das für die genannten Daten repräsentativ ist,

B - Abtasten der Amplitude des genannten analogen Signals mit einer Mehrzahl an Intervallen des genannten Datentakts, um so eine Mehrzahl an einzelnen Amplitudenproben zu erzeugen,

C - Vergleichen jeder der genannten Mehrzahl einzelner Amplitudenproben mit mindestens einer Referenzamplitude, und Erzeugen einer Mehrzahl von Differenzwerten als Ergebnis davon, wobei das Verfahren durch folgende Schritte charakterisiert ist:

D - Werttrennung der genannten Mehrzahl an Differenzwerten, und Speicherung einer Zählung der Anzahl jeder der genannten Differenzwerte, und

E - Umwandlung der genannten gespeicherten Zählung der Differenzwerte in ein Maß für die Datenfehlerrate der genannten Datenspeichervorrichtung.

2. Ein Verfahren gemäß Anspruch 1, bei dem der Schritt B den Schritt der Umwandlung der genannten Mehrzahl einzelner analoger Amplitudenproben in eine Mehrzahl einzelner digitaler Amplitudenproben umfaßt, und

wobei der Schritt C den Vergleich jeder der genannten Mehrzahl digitaler Amplitudenproben mit einer Referenzamplitude und die Erzeugung einer Mehrzahl digitaler Differenzwerte als Ergebnis davon umfaßt.

3. Ein Verfahren gemäß Anspruch 1 oder 2, bei dem die genannte Datenspeichervorrichtung die genannten Daten auf das genannte Medium schreibt, wobei die genannten Daten in Übereinstimmung mit einem Teilantwortkodierverfahren kodiert werden, un wobei das genannte Amplitudenerkennungsschaltmittel den Dateninhalt eines analogen Teilantworteinlesesignals erkennt.

4. Ein Verfahren gemäß allen vorherigen Ansprüchen, wobei die folgenden Schritte enthalten sind:
Aufzeichnung von Binärdaten auf dem genannten Speichermedium, nachdem die genannten Daten in Übereinstimmung mit einem Teilantwortkodierverfahren kodiert wurden, wobei der Schritt A folgendes umfaßt:
Einlesen des genannten kodierten Binärdatenmusters aus dem genannten Medium, um so ein kontinuierliches analoges Signal zu erzeugen, das für das genannte kodierte Binärdatenmuster repräsentativ ist, und wobei
Schritt C vor der Teilantwortdekodierung des genannten kodierten Binärdatenmusters, das in Schritt A erzeugt wird, erfolgt.

5. Ein Verfahren gemäß allen vorherigen Ansprüchen, wobei der Schritt D die folgenden Schritte umfaßt:
Bereitstellung einer Mehrzahl einzeln adressierbarer Speicherstellen, wobei die genannten Speicherstellen so konstruiert und angeordnet sind, daß der gespeicherte Zählinhalt darin bei jeder Adresse um eine Zählung inkrementiert wird,
Erzeugung derselben Speicheradresse für alle Werte, die den genannten wertgetrennten Differenzwerten ähnlich sind, und
Verwendung der genannten erzeugten Speicheradressen zur Adressierung der genannten Speicherstellen, um so eine Zählung der genannten Werte, die den genannten wertgetrennten Differenzwerten ähneln, zu speichern.

6. Ein Verfahren gemäß allen vorherigen Ansprüchen, wobei der Schritt D die Erzeugung eines Histogramms der genannten gespeicherten Zählung wertgetrennter Differenzwerte umfaßt.

7. Eine Datenspeichervorrichtung, die folgendes umfaßt:
ein Speichermedium,
ein Schreibkanalmittel, um die amplitudenkodierten Daten auf das genannte Medium zu schreiben,
ein Lesekanalmittel, um die genannten geschriebenen Daten vom genannten Medium einzulesen, und um ein analoges Lesesignal als Resultat davon zu erzeugen,
ein Analog/Digital-Konvertermittel (19) mit einem Ausgang und mit einem Eingang, der so angeschlossen ist, daß er das genannte analoge Lesesignal empfangen kann,
ein Taktmittel (21'), das in einem steuernden Verhältnis an das genannte Analog/Digital-Konvertermittel angeschlossen ist und bewirkt, daß das genannte Analog/Digital-Konvertermittel am genannten Ausgang in vorbestimmten Intervallen des genannten Taktmittels eine digitale Probeamplitude bereitstellt,
ein amplitudenempfindliches Datendekodiermittel (21), das an den Ausgang des genannten Analog/Digital-Konvertermittels angeschlossen ist,
ein Lesefehlerfunktionsmittel (31), das an den Ausgang des genannten Analog/Digital-Konvertermittels angeschlossen ist und die genannten digitalen Probeamplituden in den genannten vorbestimmten Intervallen des genannten Taktmittels mit erwarteten digitalen Amplituden für die genannten Proben vergleicht, um so für jede der genannten digitalen Probeamplituden eine digitale Differenzamplitude zu erzeugen, dadurch charakterisiert, daß sie weiterhin folgendes umfaßt:
ein Speichermittel (33) zur Trennung der genannten digitalen Differenzamplituden in Übereinstimmung mit den verschiedenen Größen davon, und
ein Mittel (36) zur Adressierung des genannten Speichermittels und zur Bereitstellung eines Ausgangsanzeigemittels, das ein Frequenzhistogramm der genannten getrennten digitalen Differenzgrößen abbildet.

8. Eine Datenspeichervorrichtung gemäß Anspruch 7, bei der der genannte Speichermittelwert die genannten digitalen Diferenzgrößen trennt und eine Zählung der Anzahl des Auftretens jeder einzelnen der genannten digitalen Differenzgrößen speichert, und wobei das genannte Mittel zur Adressierung des genannten Speichermittels die genannte gespeicherte Zählung einzelner Differenzgrößen in ein Maß für die Lesefehlerrate der genannten Datenspeichervorrichtung umwandelt.

9. Eine Datenspeichervorrichtung gemäß Anspruch 7 oder 8, bei der das genannte Speichermittel ein Zählmittel (51) mit einer Mehrzahl adressierbarer Speicherstellen umfaßt, wobei die Adresse jeder Speicherstelle des genannten Zählmittels einer anderen einzelnen digitalen Differenzgröße entspricht, und bei der der Inhalt jeder der genannten adressierbaren Speicherstellen bei jeder Adressierung um eine Zählung inkrementiert wird.

10. Eine Datenspeichervorrichtung gemäß den Ansprüchen 7 bi 9, bei der das genannte Schreibkanalmittel Daten in das genannte Medium schreibt, wobei die genannten Daten in Übereinstimmung mit einem Teilantwortkodierverfahren kodiert werden, und bei der das genannte Lesekanalmittel den Dateninhalt eines analogen Teilantworteinlesesignals in einer Amplitudenprobe einliest.

Revendications

1. Méthode pour déterminer le taux d'erreur de données d'un dispositif d'emmagasinage de données ayant un support d'enregistrement sur lequel des données ont été écrites, et ayant un circuit de détection d'amplitude pour détecter lesdites données après lecture à partir dudit support, ledit circuit de détection comprenant un moyen d'horloge de données, la méthode comprenant les étapes de :
   A - lire lesdites données à partir dudit support, de façon à générer ainsi un signal analogique qui est représentatif desdites données,
   B - échantillonner l'amplitude dudit signal analogique à une pluralité d'intervalles de ladite horloge de données, de façon à produire ainsi une pluralité d'échantillons d'amplitude indivuduels,
   C - comparer chacun de ladite pluralité d'échantillons d'amplitude indivuduels à au moins une amplitude de référence, et générer une pluralité de valeurs de différence résultantes ; la méthode étant caractérisée par les étapes de :
   D - séparer selon la valeur ladite pluralité de valeurs de différence, et emmagasiner un compte du nombre de chacune des valeurs de différence, et
   E - traduire ledit compte emmagasiné des valeurs de différence en une mesure du taux d'erreur de données dudit dispositif d'emmagasinage de données.

2. Méthode telle que revendiquée dans la revendication 1, dans laquelle l'étape B comprend l'étape de convertir ladite pluralité d'échantillons d'amplitude analogiques individuels en une pluralité d'échantillons d'amplitude numériques individuels, et
   dans laquelle l'étape C comprend la comparaison de chacun de ladite pluralité d'échantillons d'amplitude numériques à une amplitude numérique de référence, et la génération d'une pluralité de valeurs de différence numériques résultantes.

3. Méthode telle que revendiquée dans la revendication 1 ou 2, dans laquelle ledit dispositif d'emmagasinage de données est adapté pour écrire lesdites données sur ledit support avec lesdites données codées selon une technique de codage à réponse partielle, et dans laquelle ledit circuit de détection d'amplitude est adapté pour détecter les données contenues dans un signal analogique de lecture à réponse partielle.

4. Méthode telle que revendiquée dans l'une des revendications précédente comprenant les étapes de :
   enregistrer des données binaires sur ledit support d'enregistrement après que lesdites données binaires ont été codées en utilisant une technique de codage à réponse partielle, dans laquelle l'étape A comprend :
   la lecture de la configuration desdites données binaires codées à partir dudit support, de façon à générer un signal analogique continu qui est représentatif de ladite configuration des données binaires codées, et dans laquelle,
   l'étape C a lieu avant le décodage à réponse partielle de ladite configuration de données binaires qui est générée à l'étape A.

5. Méthode telle que revendiquée dans l'une des revendications précédentes dans laquelle l'étape D comprend les étapes de :
   fournir une pluralité d'emplacements de mémoire adressables individuellement, lesdits emplacements de mémoire étant déterminés et adaptés pour incrémenter le contenu du compte emmagasiné d'un compte pour chaque survenance d'adresse,
   générer la même adresse de mémoire pour toutes les valeurs similaires parmi lesdites valeurs de

différence séparées selon la valeur, et

utiliser lesdites adresses de mémoire générées pour adresser lesdits emplacements de mémoire, de façon à emmagasiner un compte du nombre de survenances desdites valeurs de différence séparées selon la valeur.

6. Méthode telle que revendiquée dans l'une des revendications précédentes dans laquelle l'étape D comprend la génération d'un histogramme dudit compte emmagasiné des valeurs de différences séparées selon la valeur.

7. Dispositif d'emmagasinage de données comprenant :

un support d'enregistrement,

un canal d'écriture pour écrire des données de codage d'amplitude sur ledit support,

un canal de lecture pour lire lesdites données écrites sur ledit support, et pour générer un signal de lecture analogique résultant,

un convertisseur analogique-numérique (19) ayant une sortie, et ayant une entrée connectée pour recevoir ledit signal de lecture analogique,

une horloge (21) connectée en relation de contrôle audit convertisseur analogique-numérique, et adaptée pour que ledit convertisseur analogique-numérique fournisse à ladite sortie une amplitude numérique échantillon à des intervalles prédéterminés de ladite horloge,

un moyen de fonction d'erreurs de lecture (31) connecté à la sortie dudit convertisseur analogique-numérique, et adapté pour comparer lesdites amplitudes numériques échantillons à des intervalles prédéterminés de ladite horloge à des amplitudes numériques attendues pour lesdits échantillons, pour ainsi générer une amplitude de différence numérique pour chacune desdites amplitudes numériques échantillons,

caractérisé en ce qu'il comprend en outre :

une mémoire (33) pour séparer lesdites amplitudes de différence numériques selon leurs différentes valeurs, et

un moyen pour adresser ladite mémoire et pour fournir un affichage de sortie représentant un histogramme de fréquences desdites valeurs de différence numériques séparées.

8. Dispositif d'emmmagasinage de données tel que revendiqué dans la revendication 7, dans lequel ladite mémoire sépare selon la valeur lesdites valeurs de différence numériques, et emmagasine un compte du nombre atteint pour chacune desdites valeurs de différence numériques, et dans lequel ledit moyen pour adresser ladite mémoire traduit ledit compte emmagasiné de valeurs de différence individuelles en une mesure du taux d'erreurs de données dudit dispositif d'emmagasinage de données.

9. Dispositif d'emmagasinage de données tel que revendiqué dans la revendication 7 ou 8, dans lequel ladite mémoire comprend un compteur (51) ayant une pluralité d'emplacements adressables, l'adresse de chaque emplacement dudit compteur correspondant à une valeur de différence numérique individuelle différente, et dans lequel le contenu de chacun desdits emplacements adressables s'incrémente pour chaque cas d'adressage.

10. Dispositif d'emmagasinage de données tel que revendiqué dans l'une des revendications 7 à 9, dans lequel ledit canal d'écriture est adapté pour écrire des données sur ledit support avec lesdites données codées selon une technique de codage à réponse partielle, et dans lequel ledit canal de lecture est adapté pour détecter par échantillons d'amplitude les données contenues dans un signal analogique de lecture à réponse partielle.

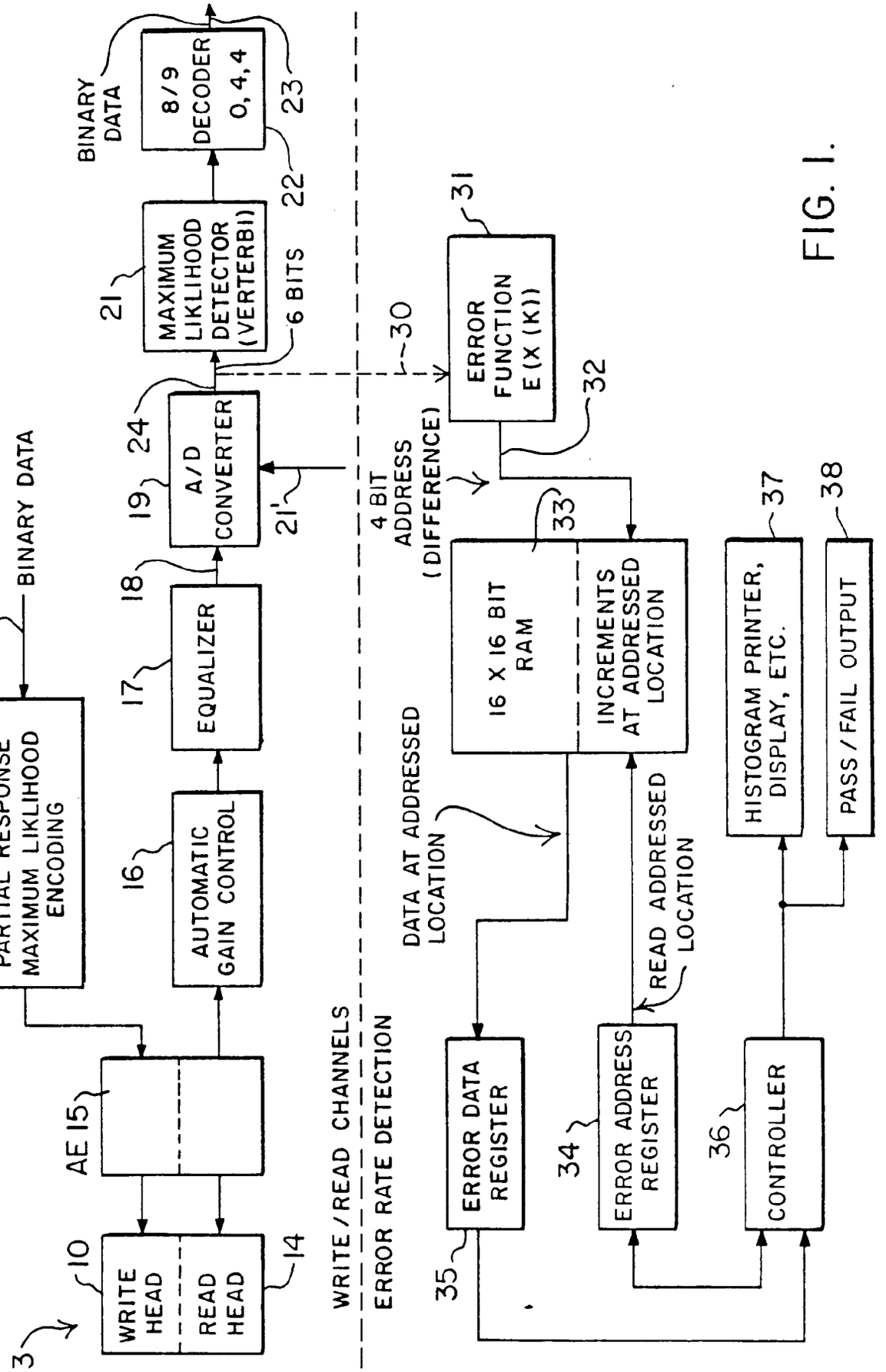

BINARY DATA
8/9 DECODER 0,4,4
23
22
MAXIMUM LIKLIHOOD DETECTOR (VERTERBI)
21
6 BITS
30
ERROR FUNCTION E(X(K))
31
32
A/D CONVERTER
24
19
21'
4 BIT ADDRESS (DIFFERENCE)
EQUALIZER
18
17
AUTOMATIC GAIN CONTROL
16
PARTIAL RESPONSE MAXIMUM LIKLIHOOD ENCODING
12
11
BINARY DATA
16 X 16 BIT RAM
33
INCREMENTS AT ADDRESSED LOCATION
DATA AT ADDRESSED LOCATION
READ ADDRESSED LOCATION
HISTOGRAM PRINTER, DISPLAY, ETC.
37
PASS / FAIL OUTPUT
38
AE 15
WRITE HEAD
10
READ HEAD
14
13
WRITE / READ CHANNELS
ERROR RATE DETECTION
ERROR DATA REGISTER
35
ERROR ADDRESS REGISTER
34
CONTROLLER
36

FIG. 1.

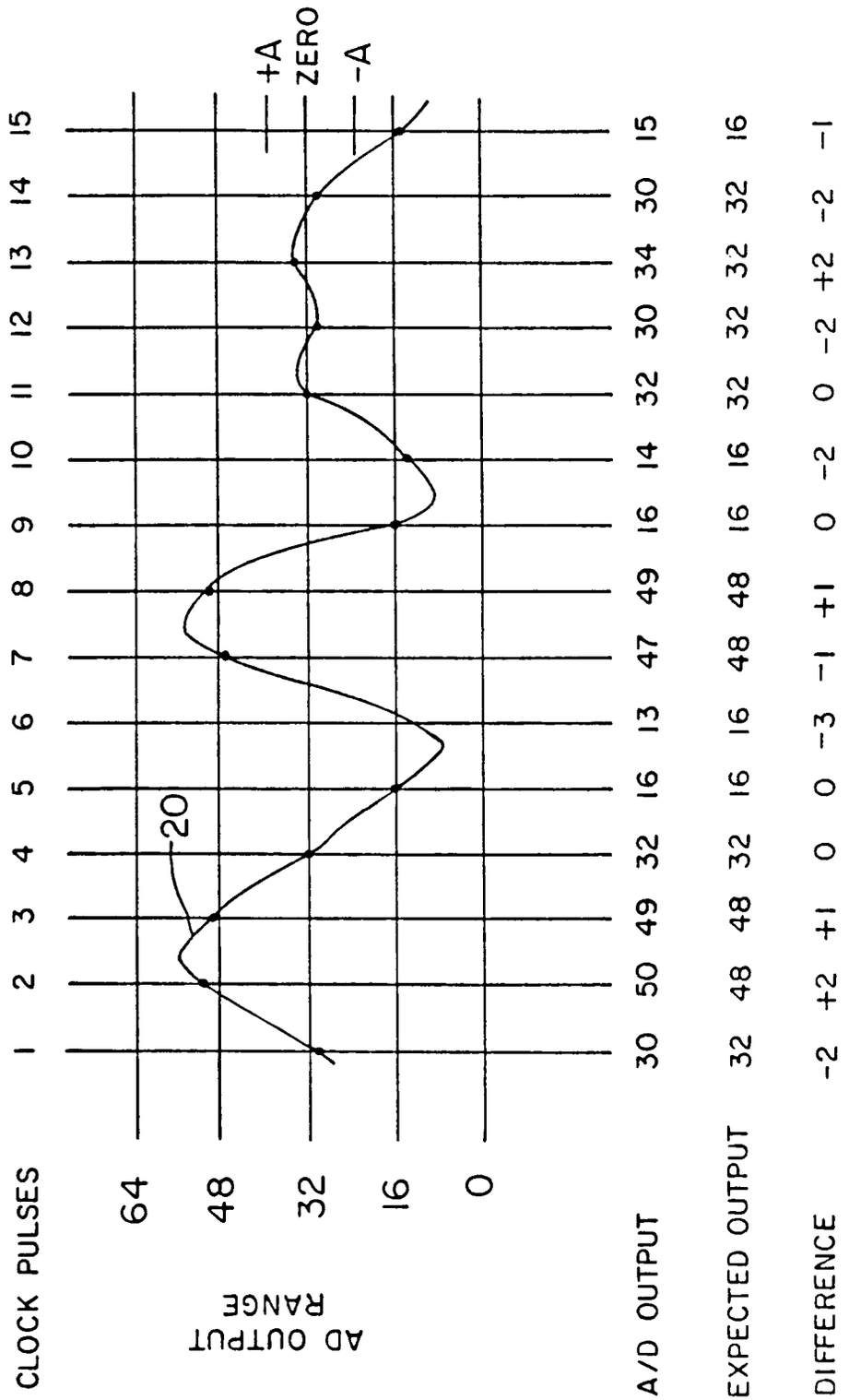

+A
ZERO
-A
20
AD OUTPUT RANGE
64
48
32
16
0
CLOCK PULSES
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
A/D OUTPUT
30 50 49 32 16 16 13 47 49 16 14 32 30 30 34 32 30 32
EXPECTED OUTPUT
32 48 48 32 16 16 48 48 16 16 32 32 32 32 32 32
DIFFERENCE
-2 +2 +1 0 0 -3 -1 +1 0 -2 0 -2 +2 -2 -2 -1

FIG. 2.

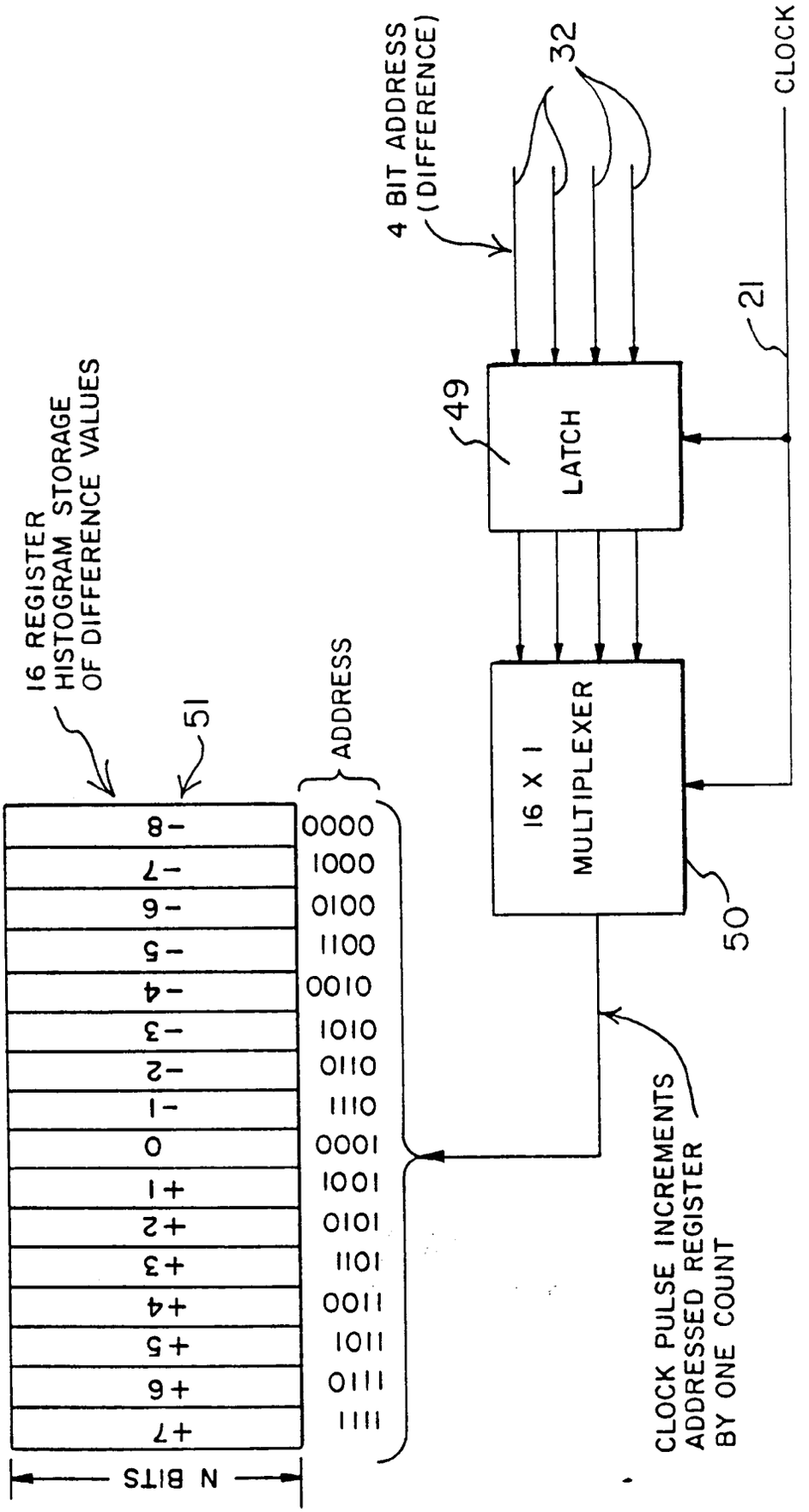

16 REGISTER
HISTOGRAM STORAGE
OF DIFFERENCE VALUES
51
ADDRESS
-8
-7
-6
-5
-4
-3
-2
-1
0
+1
+2
+3
+4
+5
+6
+7
0000
1000
0100
1100
0010
1010
0110
1110
0001
1001
0101
1101
0011
1011
0111
1111
N BITS
4 BIT ADDRESS
(DIFFERENCE)
32
CLOCK
21
49
LATCH
16 X 1
MULTIPLEXER
50
CLOCK PULSE INCREMENTS
ADDRESSED REGISTER
BY ONE COUNT

FIG. 3.

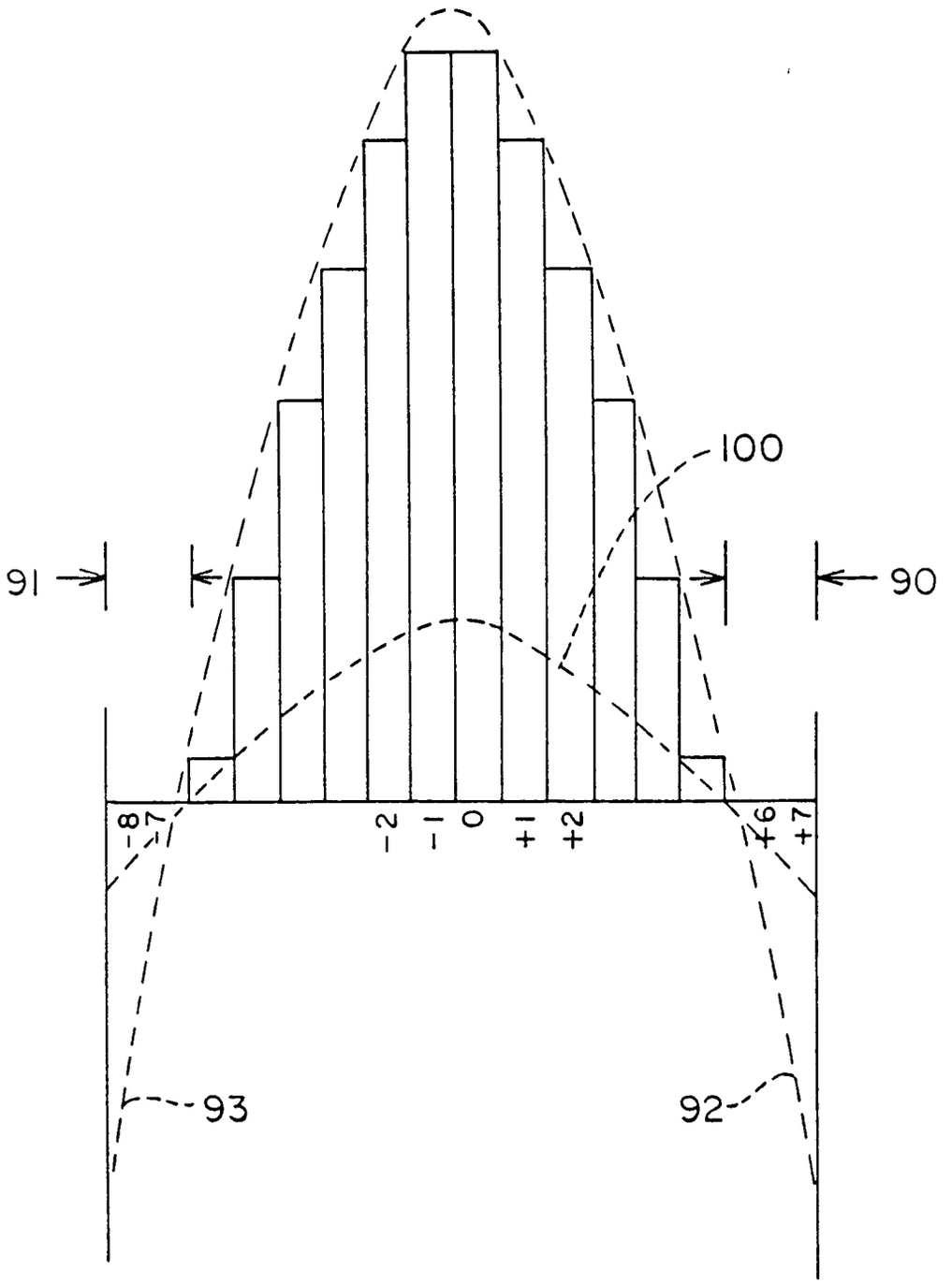


FIG. 4.