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64 Current-mirror circuit with buffering transistor.

(57) A current-mirror (10) circuit includes a pair of NMOS transistors (12 and 14). The first NMOS transistor (12) has a gate electrode, a drain electrode serving as a current input terminal (16) of the current-mirror circuit (10) and a source electrode connected to a pre-selected potential. The second NMOS transistor (14) has a gate electrode connected to the gate electrode of the first NMOS transistor, a drain electrode serving as a current output terminal (20) of the current-mirror circuit (10) and a source electrode connected to the preselected potential. The current-mirror circuit is provided with a buffer circuit. The buffer circuit includes a bipolar transistor which is opposite in polarity to the paired NMOS transistors (12, 14), i.e., a PNP bipolar transistor (22). This transistor is associated with a constant current source (24).

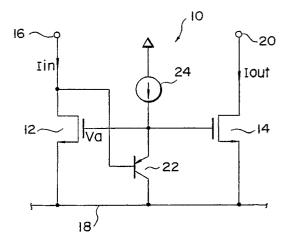


FIG. 1



EUROPEAN SEARCH REPORT

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Y: A: O: P:	CATEGORY OF CITED DOCU particularly relevant if taken alone particularly relevant if combined wit document of the same catagory technological background non-written disclosure intermediate document theory or principle underlying the in	h another	the filing d D: document L: document	ate cited in th cited for	