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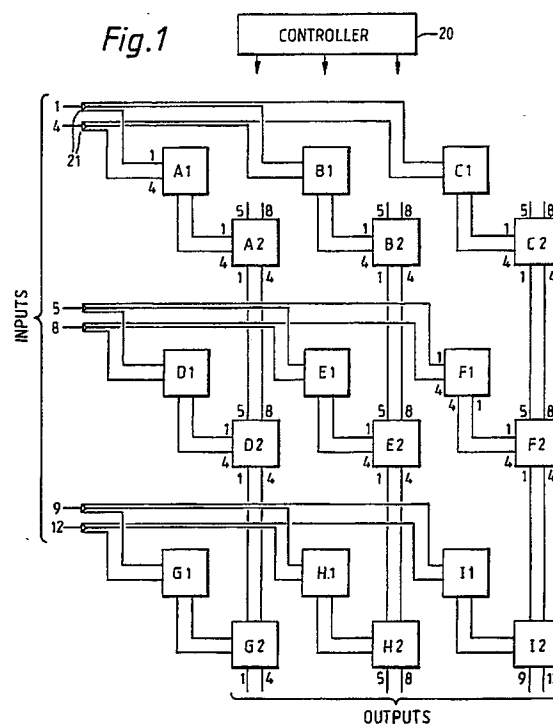
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Digital switcher for routing signals.

A digital switcher routes signals at rates up to or more than 300 MHz between switcher inputs and outputs. The switcher includes an array of n rows and m columns of modules linking n groups of switcher inputs and m groups of switcher outputs. Each module consists of a primary switching unit (A1) for selectively coupling individual ones of its outputs to ones of its inputs and a number of individually-controllable, regenerative, two-input selector switches (A2). The primary and selector switches are controlled by a controller (20). The selector switch outputs form the module outputs. Each selector switch has an input connected to an associated output of the primary switching unit in the same module, and the other connected to an associated output of a module in the previous row of the array (apart from those in the first row). The switcher outputs are derived from the outputs of the last row of modules.

To route a signal from a switcher input to a selected switcher output, the appropriate primary switching unit to which that switcher input is fed links its corresponding input to the selected one of its outputs. The regenerative selector switches in that module and in modules in subsequent rows then cascade the signal from that module through the subsequent rows to the selected switcher output.

Fig.1



EP 0 430 405 A2

DIGITAL SWITCHER FOR ROUTING SIGNALS

BACKGROUND OF THE INVENTION

This invention relates to digital routing switchers for routing signals from a plurality of switcher inputs to a plurality of switcher outputs, and in particular to switchers for high frequency applications.

Conventionally a switcher for digital or analogue signals is constructed as a modular system comprising an array of smaller switching units which may be obtained as standard components. For example a 16 x 16 switcher may comprise a 4 by 4 array of 4-input, 4-output switching units. As larger switchers are required, the number of modular switching units can simply be increased and/or the size of the modules increased.

Such switchers are commonly used in broadcasting applications for analogue video (e.g. PAL or NTSC) or audio signals, the interconnections between modular switching units comprising circuit board tracks or wiring. At frequencies up to 10 MHz the loss of signal quality due to the switcher presenting distributed and inaccurately terminated signal paths is not significant. It is now becoming necessary however to convert analogue video and audio signals to digital serial data at rates as high as 270 Mbit/s or more.

A switcher which employs matched signal paths to maintain signal quality is available, and is used for switching analogue signals (e.g. NTSC and PAL). This switcher comprises a conventional array of primary switching units (corresponding to the switching units described above). A respective group of inputs of the switcher is connected in parallel to the inputs of the primary switching units of each row of the array, the array having N rows where N is a plural integer. Each output of the switcher is output from a N-input, 1-output switching unit, the N inputs of which are connected to respective ones of the outputs of each of the primary switching units in a corresponding column of the array. The signal paths between the primary switching units and the N-input, 1-output switching units can then be matched so that the transmission time for a signal through the switcher from any input to any output is equal.

Certain disadvantages are inherent however in the implementation of this switcher architecture. The first of these is that the arrangement of the lines required to connect the primary switching units to the N-input, 1-output switching units is complex particularly for large switchers comprising arrays of large numbers of primary switching units. The second disadvantage arises if output amplifiers are required to amplify the switcher outputs. In a

practical implementation of this switcher architecture only a small output amplifier density can be achieved because of the low density of the N-input, 1-output switching units. The size and cost of such a switcher are therefore disadvantageously large.

SUMMARY OF THE INVENTION

The invention provides a digital switcher comprising a plurality of switcher inputs arranged in n groups each comprising plural inputs, a plurality of switcher outputs arranged in m groups each comprising plural outputs, and a plurality of n.m modules in an array of n rows by m columns coupling the input groups and the output groups, each module including a primary switching unit for selectively coupling the module inputs to individual ones of the module outputs, wherein at least each module other than those in the first row further comprises a plurality of individually-controllable two-input selector switches, one for each module output, one input of each switch being coupled to an associated output of the primary switching unit of the same module and the other input of each switch being coupled to an associated output of a module in the preceding row.

Preferably each input to the switcher is amplified by an amplifier, each amplifier comprising a number of outputs connected in parallel to the inputs of each of the primary switching units of the corresponding row of the array. In this way the source impedances of each input to the switcher can be controlled accurately.

Preferably also the source impedances of the outputs of each secondary switching unit will be equal and the termination impedances of the inputs of each secondary switching unit will be equal so that the impedance of each connection between components within the switcher is known and constant. This allows the switcher to be used without loss of signal quality at much higher data rates than was possible with prior art switchers. For example the switcher is advantageous for switching signals of data rates higher than 10 MHz.

Preferably also the primary switching units and/or the selector switches are regenerative.

The invention may be of greatest value in switchers having from 64 to 512 inputs, although it is also advantageous in smaller or larger switchers.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described by way of example with reference to the figures in which:

Figure 1 is a block diagram of a 12-input, 12-output switcher according to the invention;

Figure 2A is a front view of a 64 x 64 switcher according to the invention implemented on circuit cards in two frames for rack mounting;

Figure 2B is a rear view of the embodiment of Figure 2A;

Figure 3 is a block diagram of an input channel of the switcher of Figures 2A and 2B;

Figure 4 is a block diagram of a crosspoint card of the switcher of Figures 2A and 2B;

Figure 5 is a block diagram of the switcher of Figures 2A and 2B;

Figure 6 is a block diagram of an output channel of the switcher of Figures 2A and 2B; and

Figure 7 is a front view of a 128 x 128 switcher according to the invention, implemented on circuit cards in five frames for rack mounting.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The digital switcher of the embodiment of Figure 1 is for routing signals from twelve inputs to twelve outputs in any permutation. The switcher is of modular construction, comprising a three by three array of nine modules each comprising a primary switching unit, or crosspoint, (e.g. A1) and a secondary switching unit (e.g. A2).

Each primary switching unit, or crosspoint, (e.g. A1) has four inputs (1-4) and four outputs (1-4). Under the control of a central controller 20 each primary switching unit can connect each of its four outputs to any of its four inputs.

Each secondary switching unit (e.g. A2) comprises four two-input, one-output selector switches and so has eight inputs (1-8) and four outputs (1-4); output 1 is connectable to either input 1 or 5, output 2 to input 2 or 6, output 3 to input 3 or 7 and output 4 to input 4 or 8. These connections are controlled by the central controller 20. The secondary switching units regenerate data signals they receive. In each secondary switching unit the inputs are terminated and the selected received signals regenerated and sent out of the appropriate outputs.

For optimum performance the primary switching units, or crosspoints, will also be regenerative.

The modules are notionally arrayed in three rows and three columns. Each row corresponds to four of the twelve switcher inputs, row 1 to inputs 1 to 4, row 2 to inputs 5 to 8 and row 3 to inputs 9 to 12. Each column corresponds similarly to four outputs of the switcher.

Each column comprises a series of secondary switching units (for example in column 2 these are B2, E2, H2), the outputs 1-4 of each being connected to four of the inputs (5-8) of the unit in the

next row. The outputs 1-4 of E2 in row 2 are therefore, for example, connected to inputs 5-8 of H2.

As noted above, each secondary switching unit regenerates digital signals which it receives. The lines between the secondary switching units can thus all have the same known source and termination impedances independent of conditions within the switching units. If a signal is to be routed through the switcher along a column or part of a column of secondary switching units, it is therefore relayed accurately without loss of signal quality.

Also as noted above each of the three rows of modules in the switcher corresponds to four of the 12 inputs of the switcher. Signals from each input are distributed by an amplifier 21, a separate amplifier output being connected to the appropriate input of each primary switching unit, or crosspoint, requiring access to that signal. For example switcher inputs 5 to 8 correspond to row 2 of the array of switching modules. Each of these inputs therefore enters an amplifier 21 and then separate outputs from each amplifier are sent to the corresponding inputs of the primary switching units D1, E1 and F1. In this way the input impedance of each input into the switcher is tightly controlled.

The outputs of each primary switching unit are connected to four (1-4) of the eight inputs of its associated secondary switching unit. The eight inputs of each secondary switching unit (e.g. E2) are therefore connected as follows: four inputs (1-4) to the outputs of its associated primary switching unit (e.g. E1) and four inputs (5-8) to the outputs of the secondary switching unit in the previous row of the same column (e.g. B2).

A signal may thus be routed from any input of the switcher to any output of the switcher by routing it through the appropriate primary switching unit, or crosspoint, and then cascading or relaying it along the secondary switching units of the appropriate column. For example to route a signal from switcher input 5 to switcher output 11, primary switching unit F1 would connect input 1 of its inputs to output 3 of its outputs, and secondary switching unit F2 would route input 3 of its inputs from the primary switching unit F1 to its output 3. The signal would then be relayed or cascaded along the third column of the switcher from F2 to I2 and thus to output 11 of the switcher.

If required, output amplifiers may be included to amplify each output of the switcher.

The secondary switching units A2, B2, C2 in the first row of the array of modules in the switcher may be omitted, and the outputs from each of the primary switching units or crosspoints A1, B1, C1 in the first row connected directly to the inputs 5-8 of the respective secondary switching units D2, E2, F2 in the second row of the array. However, to

achieve modular construction it may be preferred to have secondary switching units on the outputs of all primary switching units, as shown in the drawing.

Using either of these arrangements, whatever route a signal takes through the switcher, the source and termination impedances of all portions of the route are known and constant regardless of the condition of the switching network in the remainder of the switcher.

The switcher can therefore be used without loss of signal quality for switching pulses at much higher data rates than could be handled by prior art switchers.

In the interests of modular construction it may also be preferred that each associated primary switching unit and secondary switching unit (e.g. D1 and D2) and the links between them could be manufactured as a single component or built on the same circuit board. Alternatively a number of modules may be accommodated on the same component or circuit board.

In a practical switching system for a broadcasting application a switcher may be required to route as many as 200 inputs to a comparable number of outputs and may use primary switching units each having 16 or more inputs and outputs, and secondary switching units each comprising 16 or more, independently controlled, 2 input, 1 output selector switches. Practical implementations of two larger switchers of this type will now be described.

A 64 x 64 switcher according to the invention is shown in Figures 2 to 7. The switcher is implemented on circuit boards, or cards, mounted conventionally in frames A,B for rack mounting, as shown in Figures 2 and 3.

As a result of the modular switcher construction of the invention, only three card types are required in addition to computer and buffer cards to interface the switcher to an external control system. The card types include an 8-channel input card 50, a 32 x 16 crosspoint card 52 and a 16-channel output card 54.

Each input card 50 comprises eight input channels, each channel comprising an input buffer 56 as shown in Figure 3. The input buffer 56 reclocks a digital data stream applied to it from an input cable 58. The cable 58 may be up to 130 metres in length, and forms an unbalanced input to the buffer 56. The buffer comprises a 75 Ohm cable equaliser 60 (for a 0-130m cable) and a data regenerator 62 which regenerates the original digital signal despite degradation of its analogue parameters during transmission along the cable 58. The data regenerator 62 restores the original signal level and reclocks the data using a register timed by a jitter-free clock 64 provided by a phase-locked-loop. The regenerated signal is thus returned to its original

sending end specification. The data regeneration function may be implemented by an integrated analogue/ECL ASIC (emitter coupled logic application specific integrated circuit) to provide repeatability with low cost and high performance. In this embodiment, for example, data rates from 140 to 300 MHz may be used.

The regenerated signal is then buffered to three parallel output drivers 66, 68, 70. Two output drivers 66, 68 feed up to eight crosspoints in the local frame, the remaining output driver 70 being connected to an expansion port 72 of the local frame. The expansion port 72 can then be connected to feed crosspoints in expansion frames, which may be required for a switcher having more than 128 outputs.

A 32 x 16 crosspoint card 52 is shown diagrammatically in Figure 4. Each crosspoint card 52 contains two ASICs each comprising a 16 x 16 crosspoint array, and a secondary switching unit comprising 16 2-input, 1-output selector switches 76. The two 16 x 16 crosspoints are arranged as a balanced 32 x 16 crosspoint array 74 whose outputs are respectively connected to an input of each of the secondary switches 76. The second input of each switch is for connection to an output of another crosspoint card. The 16 outputs from the secondary switches 76 are connected to outputs of the crosspoint card 52.

Each output card 54 carries 16 output buffer channels. One channel is shown diagrammatically in Figure 5. Each channel comprises a data regenerator 80 to recondition the signal. The data regenerator 80 comprises an ASIC as on an input card 50, and uses a phase locked loop 82 and a register to re-clock the signal. This removes any jitter produced by crosstalk in the routing system of the switcher and restores the signal to specification for transmission to the next piece of equipment. Two outputs from each channel are provided, each being fed through a line driving amplifier 84.

The 64 x 64 switcher is shown in Figures 2A and 2B, and in the block diagram of Figure 6. Two 13-card frames A and B each contain a power supply unit (PSU) 90A, 90B, the PSU 90B being used as a back up unit for the PSU 90A. The first rack A also contains a fan and thermostatic sensor powered via socket 92A to cool the switcher. The total power dissipated by the switcher may be as much as 0.5 kW.

Switcher inputs 1 to 32 are fed to the first frame A through BNC connectors on the back of the frame, and are received by four 8-channel input cards 50A mounted in the frame. The input signals are regenerated and balanced by the input cards 50A and are then fed in parallel to four crosspoint cards 52A mounted in frame A. The crosspoint cards 52A correspond to the modules in the first

row of the 12 x 12 switcher shown in Figure 1 in that they form the first row of modules of the switcher, and so the secondary switches on each crosspoint cards 52A may always connect the outputs of the balanced crosspoint array on the card to the card outputs.

The second frame B contains a further four input cards 50B to receive inputs 33-64 of the switcher via BNC connectors. The input cards 50B feed signals in parallel to crosspoints on four crosspoint cards 52B. The two inputs of each secondary switch on each crosspoint card 52B are connected respectively to an output from the crosspoint on the same card and to a corresponding crosspoint card output from the first frame A.

The switcher outputs are derived from the outputs from the crosspoint cards 52B in the second frame B. These crosspoint card outputs are connected to four output cards, 54A, 54B, each carrying 16 output channels to restore the output signals to specification for transmission from the switcher.

Two output cards 54 are mounted in each of the two frames, A and B, although all of the switcher outputs are derived from crosspoint cards 52B in the second frame B. This enables standardisation of the backplane in each frame.

All of the crosspoints and secondary switches are controlled by an external computer system, from which control signals are received at a control connector on the rear of the first frame A. The signals are fed via a computer card 98A in the first frame A to buffer cards 100A, 100B in each frame. Control signals in each frame are then sent from the buffer cards to the crosspoint cards 52A, 52B. In addition an analogue reference signal may be input to a BNC connector 102A to synchronise the switcher to an external system.

This technique of implementing a high speed switcher is extremely flexible. The switcher described provides a 64 input 64 output switcher capable of switching signals at up to 300 MHz using a standard set of cards which may be used in principle to implement a switcher of any size. For example the 64 x 64 switcher described requires 8 input cards, 8 crosspoint cards, 4 output cards, 1 control card and 2 control buffer cards. Two standard frames each capable of holding 13 cards are required. If for example a 40-input, 25-output switcher were required, identical componentry could be used but only 5 input cards (8 inputs per card), 4 crosspoint cards, 2 output cards (16 outputs available per card), 1 control card and 2 control buffer cards would be needed. Two frames would be required, which could use the same backplane circuitry as for the 64 x 64 switcher.

In each case however the same technique of arranging the crosspoints to form a 'cascade' is used, in which the outputs from a first crosspoint

card are fed to two input, one output secondary switches on a second crosspoint card so that the outputs from either crosspoint can be selected and passed on either to a further crosspoint card or, at the end of the 'cascade' to outputs of the switcher.

These standard components can also be used to construct larger switchers. A 128 input, 128 output switcher is shown in Figure 7. This switcher is arranged in five frames V, W, X, Y, Z, mounted in a rack. One frame V is used solely to house six power supply units, comprising three main units 120V and three back up units 122V. Each of the other four frames W-Z can hold up to 19 cards.

Switcher inputs 1 to 32 are input to four 8-channel input cards 50W in the first frame W of the four card holding frames. Similarly, inputs 33-64 are input to the second frame X, 65-69 to the third frame Y, and 97-128 to the fourth frame Z.

Each frame W-Z also contains eight crosspoint cards 52W-52Z. These are fed by two of the three available outputs from each channel of the input cards 50W-50Z, the third output being reserved as an expansion port output for use if an even larger switcher is required. In order to minimise signal path lengths, the input cards 50W-50Z in each frame W-Z are grouped together, with four crosspoint cards 52W-52Z on each side of them. One output of each input card channel then feeds the crosspoint cards on each side.

Each crosspoint card 52 has 16 outputs. The eight crosspoint cards of each of the first three frames therefore pass a total of 128 outputs to the secondary switches of the eight crosspoint cards in the next frame. To minimise signal path lengths, each crosspoint card 52 is positioned in its frame directly beneath the card in the previous frame from which it receives signals.

The third and fourth frames Y,Z each contain four output cards 54Y, 54Z. Output signals are sent to these from the eight crosspoint cards 52Z in the last frame Z. As in the 64 x 64 switcher described above, since the output cards 54Y, 54Z are not all located in the last frame Z, the same backplane circuitry may be used in all frames.

Each frame also contains computer, interface or buffer cards 124W - 124Z to handle control signals sent to the switcher from an external controller.

This form of switcher construction can clearly be extended to any size although if more than 128 outputs were required, more than one 19 card frame would be needed to contain each stage of the 'cascade' of the switcher. The expansion port output on each channel of each input card would then be used to transfer regenerated switcher input signals from one frame to another.

As switchers of larger size are constructed, and equivalently as the frequencies of the signals to be

switched are increased, the delays in propagating signals over different path lengths through the switcher become more significant. For example in the switcher of Figure 7, a signal routed from any of inputs 1 to 32 to an output must travel through all four frames of the switcher while a signal from one of inputs 97 to 128 only has to travel through one frame. Where such differences in path lengths are significant either a short range synchroniser may be used at the output of the switcher to realign the output signals, or the input signal timing may be offset appropriately.

Claims

1. A digital switcher comprising:
 - a plurality of switcher inputs arranged in $\underline{n}$ groups each comprising plural inputs;
 - a plurality of switcher outputs arranged in $\underline{m}$ groups each comprising plural outputs; and
 - a plurality of $\underline{n.m}$ modules in an array of $\underline{n}$ rows by $\underline{m}$ columns coupling the input groups and the output groups, each module including a primary switching unit (A1) for selectively coupling the module inputs to individual ones of the module outputs;
 - characterised in that at least each module other than those in the first row further comprises a plurality of individually-controllable two-input selector switches (B1), one for each module output, one input of each switch being coupled to an associated output of the primary switching unit of the same module and the other input of each switch being coupled to an associated output of a module in the preceding row.
2. A digital switcher according to claim 1, wherein said selector switches are regenerative selector switches.
3. A digital switcher according to claim 2, wherein the termination impedances of all said selector switch inputs are equal.
4. A digital switcher according to claim 2 or 3, wherein the source impedances of all said selector switch outputs are equal.
5. A digital switcher according to any preceding claim, comprising:
 - an amplifier (21) for amplifying signals at each said switcher input, each amplifier comprising a plurality of outputs connected in parallel to said module inputs in the corresponding row of the array.
6. A digital switcher according to any preceding claim, wherein said primary switching units are regenerative.
7. A digital switcher comprising:
 - a plurality of inputs to said switcher;
 - a plurality of outputs from said switcher, and
 - means for routing signals from each of said switcher inputs to any selected switcher output, said routing means comprising:
 - an array of modules connected in rows and columns, each said module comprising:
 - a primary switching unit (p.s.u.) (A1) comprising inputs, outputs and means for regenerating and selectively routing signals to any of said p.s.u. outputs from any of said p.s.u. inputs, said p.s.u. inputs being connected to inputs of said module, and
 - a secondary switching unit (B1) comprising a plurality of individually-controllable, regenerative, two-input, selector switches, outputs of said selector switches being connected to outputs of said module,
 - each selector switch having an input connected to an output of the p.s.u. in the same module and, apart from selector switches in the first row of modules, having a further input connected to an associated module output of the preceding row,
 - a respective group of said switcher inputs being coupled in parallel to the inputs of modules in each row, and
 - respective groups of said switcher outputs being coupled to outputs of modules in said last row.
8. A digital switcher comprising an array of modules arranged in rows and columns, each module comprising a primary switching unit having inputs and outputs and means for connecting its outputs to selected ones of its inputs, the inputs of each of the primary switching units of each row of modules being connected in parallel to a respective group of the switcher inputs, and a respective group of the switcher outputs being derived from the outputs of the primary switching units of modules in each column;
 - characterised by a secondary switching unit in at least each module other than those in the first row and comprising a plurality of individually controllable regenerative switches each with an output, connected to a module output, and two inputs;
 - the switch inputs respectively being connected to an output from the primary switching unit in the same module and to an associated output of a module in the preceding row, and having

means for connecting a selected switch input to the switch output; the switcher outputs being connected respectively to the switch outputs of the last row of secondary switching units.

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9. The use of a digital switcher in accordance with any preceding claim to switch digital signals at a data rate of greater than 10MHz.

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Fig.1

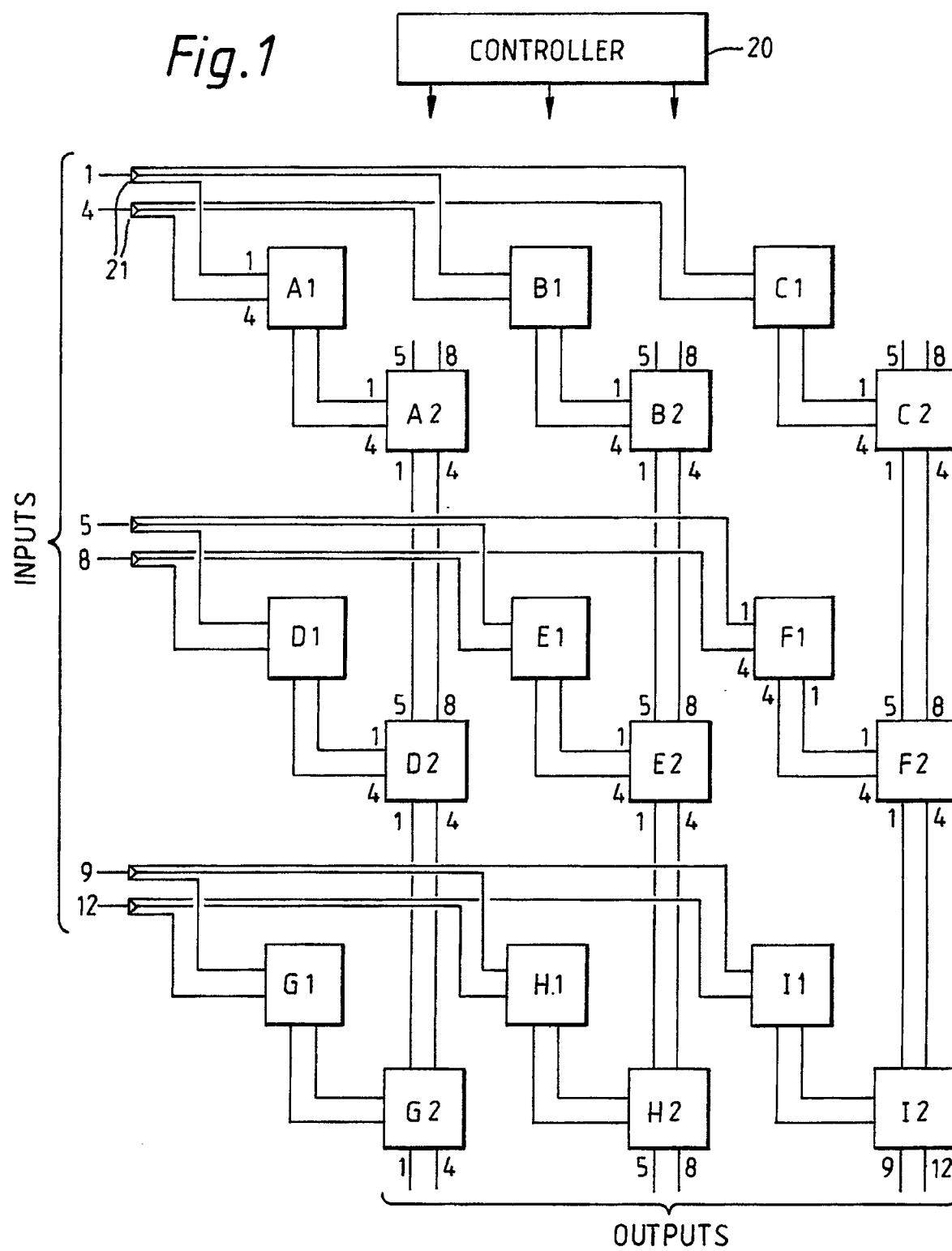


Fig. 2A.

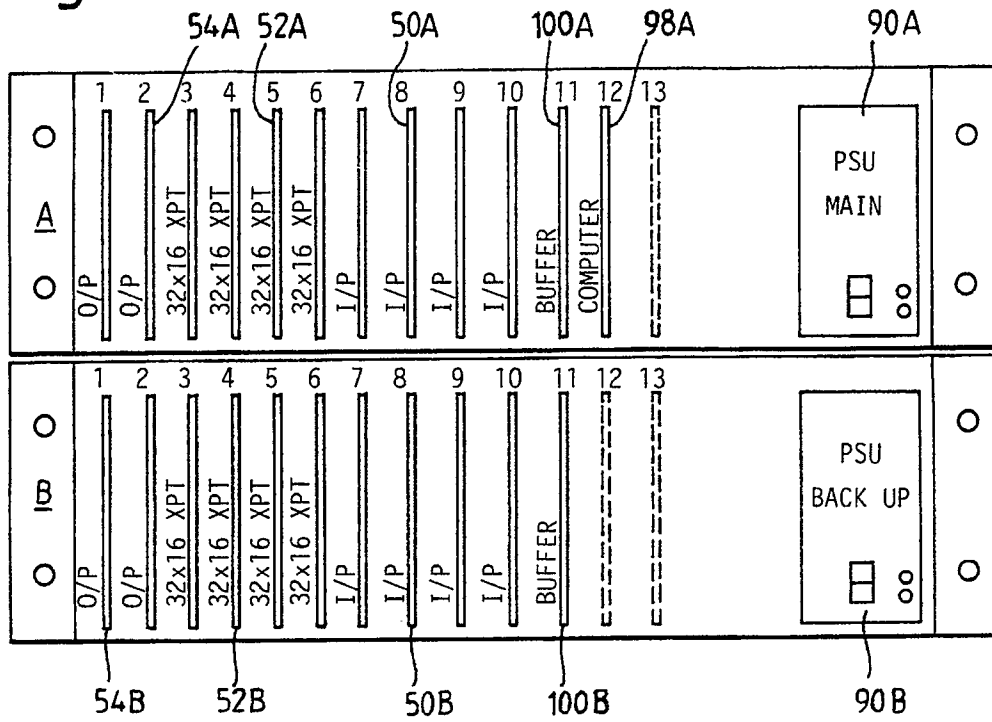
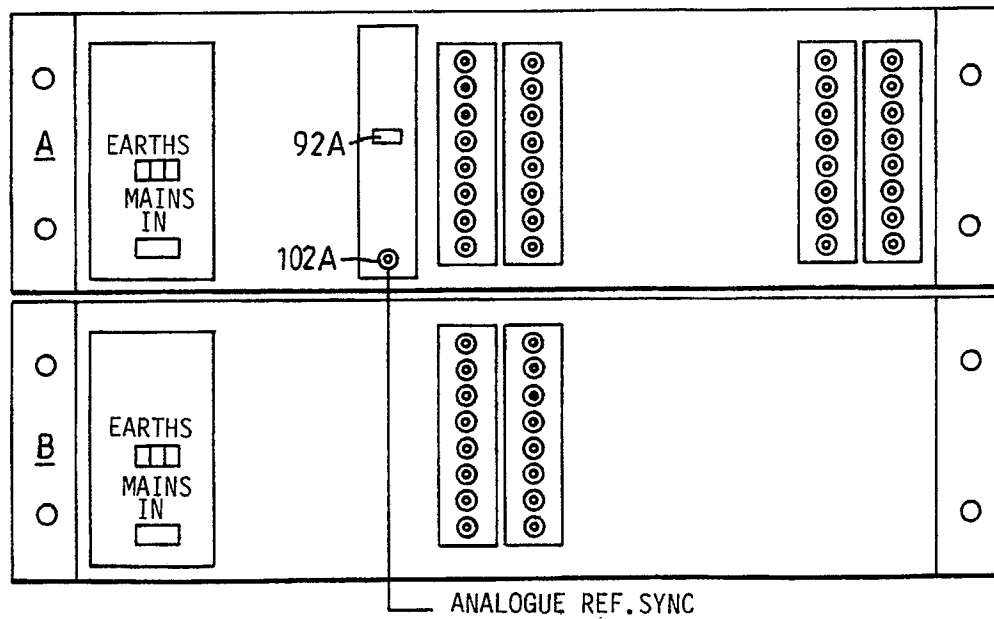
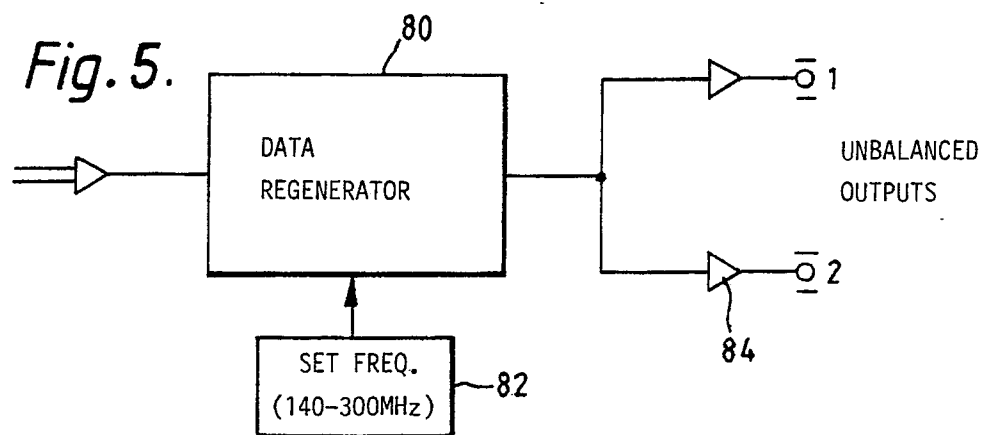
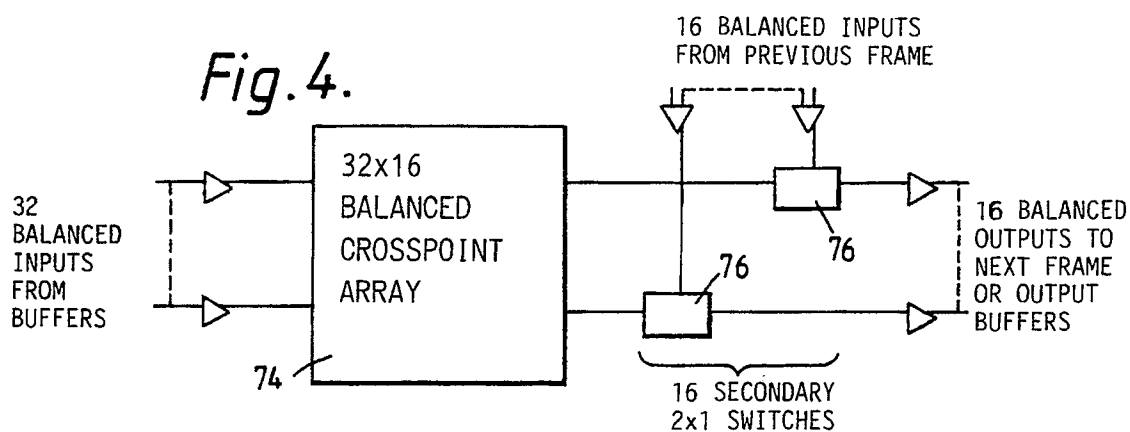
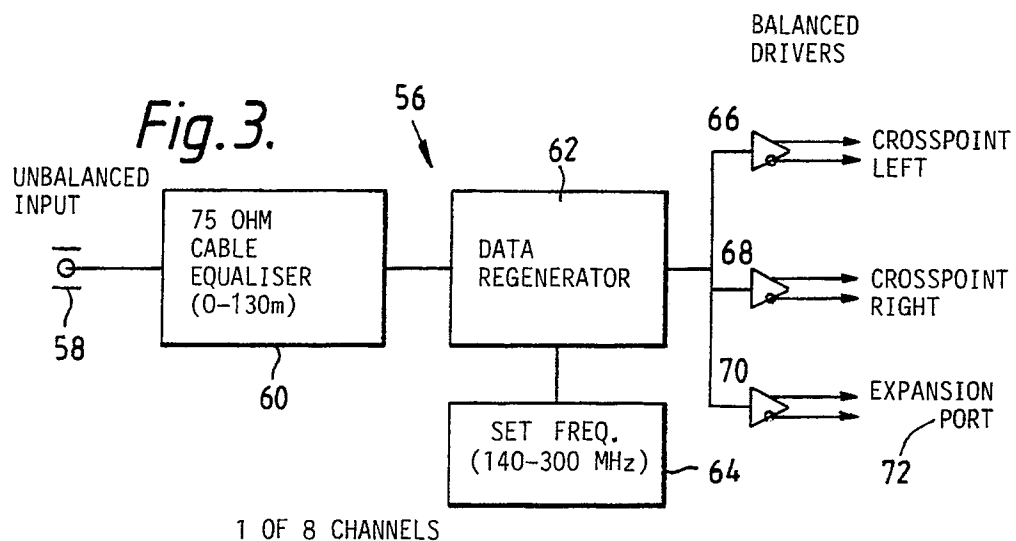


Fig. 2B.





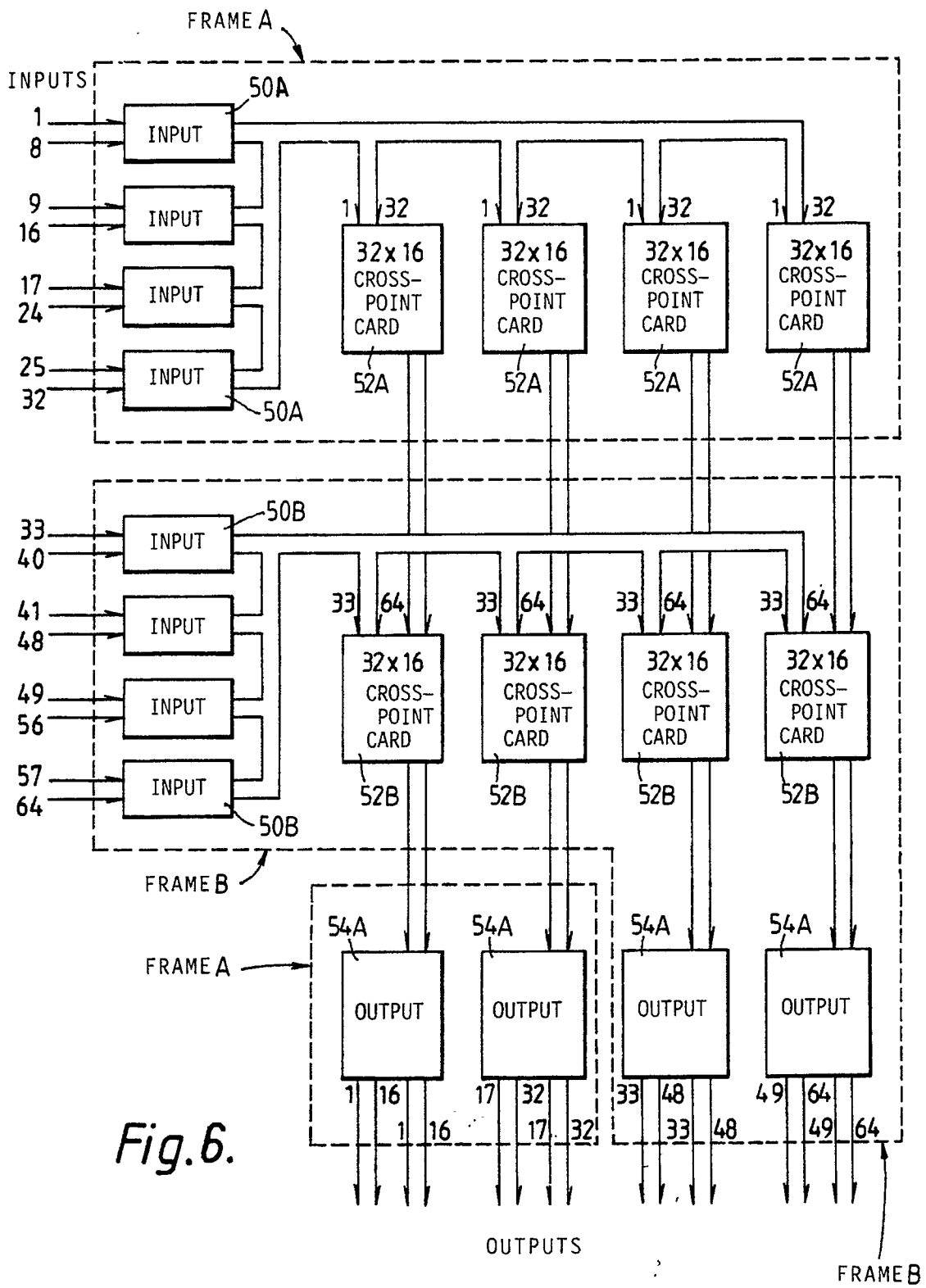


Fig. 7

