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(71) Applicant: **NATIONAL SEMICONDUCTOR CORPORATION**
2900 Semiconductor Drive P.O. Box 58090
Santa Clara California 95051-8090(US)

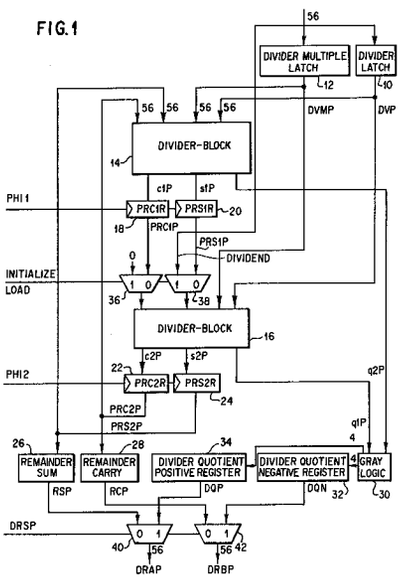
(72) Inventor: **Avnon, Dror**
P.O. Box 3007
Herzlia B 46104(IL)
Inventor: **Greenfeld Zvi**
P.O. Box 3007
Herzlia B 46104(IL)
Inventor: **Yuval, Gideon**
613 151st Pace N.E.
Bellevue, WA 87007(IL)
Inventor: **Baydach, Yair**
P.O. Box 3007
Herzlia B 46104(IL)

(74) Representative: **Sparing Röhl Henseler**
Patentanwälte European Patent Attorneys
Rethelstrasse 123
W-4000 Düsseldorf 1(DE)

(54) **Method and apparatus for SRT divison using gray coded quotient bit signals.**

(57) A method and apparatus for performing SRT division, in which Gray coded quotient bit signals are generated during each iteration from a divisor signal having Gray coded bits, and a dividend signal. Preferably, only the two most significant bits of the divisor signal are encoded into Gray code at the start of the division process, and the Gray coded quotient bit signals are decoded after each iteration, or after the final iteration, for use in generating the final quotient. In a preferred embodiment, the invention is a circuit capable of performing both single-precision and double-precision operations, and includes a pair of alternately operating divider block circuits each for generating a pair of quotient bits during each iteration cycle. The quotient bits emerging from each divider block circuit are decoded, and then shifted into one of two divider result registers depending upon their sign until 56 quotient bits (for double-precision operation) or 28 quotient bits (for single-precision operation) are accumulated in the divider result registers. When sufficient quotient bits have been accumulated, the invention asserts the contents of the divider result registers, a remainder sum register, and a remainder carry register, as output signals which may be combined to generate a final quotient signal.

FIG.1



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EUROPEAN SEARCH REPORT

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EP 90 12 2384

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	17th Annual ACM Computer Science Conference, February 1989, p441; YUEN: "Binary Division and Square-Rooting using Gray Code" * the whole document * ---	1	G 06 F 7/52
A	IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, vol. EC-8, December 1959, New York, US, pages 449-458; LUCAL: "Arithmetic Operations for Digital Computers Using a Modified Reflected Binary Code" * abstract; pages 454-455; paragraph: "Multiplication and Division" * ---	1	
A	Proceedings, 7th Symposium on Computer Arithmetic, June 1985, Illinois, pp. 64-71; TAYLOR: "Radix 16 SRT Dividers With Overlapped Quotient Selection Stages" * pages 65-66, paragraph 4 * ---	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN, vol. 7, no. 238 (P-231), 26 July 1983; & JP-A-58 125 188 (CANON) * abstract * ---	1	G 06 F
A	IEEE INT. SYMP. ON COMPUTER ARCHITECTURE AND DIGITAL SIGNAL PROCESSING, 1989, pages 217-220; C.K. YUEN: "Binary division and square-rooting using gray code" * pages 217,218 * -----	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-08-1992	COHEN B.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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