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(73) Proprietor : **SEIKO EPSON CORPORATION**
4-1, Nishishinjuku 2-chome
Shinjuku-ku Tokyo-to (JP)

(72) Inventor : **Katsunori, Yamazaki, c/o Seiko Epson Corporation**
3-5, Owa 3-chome
Suwa-shi, Nagano-ken (JP)

(74) Representative : **Hoffmann, Eckart, Dipl.-Ing. et al**
Patentanwalt
Bahnhofstrasse 103
D-82166 Gräfelfing (DE)

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Description

The present invention relates to a liquid crystal display device.

Heretofore, for driving a simple matrix type liquid crystal display device a driving method called average voltage driving method has generally been used. This driving method leads to an unevenness of the display for the following reasons. A matrix type liquid crystal display device is provided with scanning electrodes and signal electrodes forming picture elements (pixels) at each crossing point between a scanning electrode and a signal electrode. In practice, the electrical resistance of the scanning electrodes and the signal electrodes is not zero and a capacitor is formed at those crossing points with the liquid crystal layer forming the dielectric. Therefore, the effective voltage applied via the scanning electrodes and the signal electrodes to the individual pixels changes in accordance with the content of the display, i.e. the displayed image.

To solve the problem of an uneven display due to the above reason it is known to reverse the polarity of the voltage applied to the liquid crystal panel several times within one frame period. This prior art which is called the "line reverse driving method" is disclosed in the documents JP-A-62-31825, JP-A-60-19195 and JP-A-63-19196. This line reverse driving method is effective for improving the evenness of the display due to the variation of the optical characteristics of the liquid crystal changed by the frequency component of the applied voltage. However, the unevenness cannot be sufficiently removed.

The unevenness of the display can be further improved by a voltage correcting method suggested in the document EP-A-0 303 510, although even with this method the display is still not sufficiently uniform as will be explained below.

The reason why an unevenness of the display remains even with said voltage correcting method will be explained with reference to Fig. 14. Fig. 14 shows a liquid crystal panel 1 representing a specific display pattern which will be used for the following explanation. The liquid crystal panel comprises a pair of substrates 2, 3 sandwiching a liquid crystal layer (not shown). A plurality of scanning electrodes Y1 through Y6 is provided on the side of the substrate 2 facing the liquid crystal layer and a plurality of signal electrodes X1 through X6 is provided on the opposing side of the substrate 3, the signal electrodes extending perpendicularly with respect to the scanning electrodes. At each crossing area between a scanning electrode Y1 through Y6 and a signal electrode X1 through X6 a pixel (display dot) is formed. The example shown in Fig. 14 comprises 6 x 6 pixels for the sake of simplification of the explanation only. In a practical liquid crystal panel the number of pixels is substantially higher. In the display pattern shown in Fig. 14, the hatched pixels are lighting pixels whereas the other pixels are non-lighting pixels. The display pattern shown in Fig. 14 is a chequered pattern. To the left side of the scanning electrodes Y1 through Y6 a corrected scanning voltage wave is applied to every other scanning electrode, said corrected scanning voltage wave varying dependent on the display pattern in accordance with the voltage correcting method disclosed in the Japanese patent application No. 63-159914. That means, the non-selective voltage is superimposed with a correcting voltage in accordance with the difference between the number of lighting pixels on a scanning electrode and the number of lighting pixels on the following scanning electrode when the selection is moved from one scanning electrode to the following one. However, in the case of the display pattern shown in Fig. 14, since the said difference is always zero, no correcting voltage is superimposed on the non-selective voltage.

The signal electrodes X1 through X6 are divided into two groups, a first group of signal electrodes X1, X3 and X5 having applied the signal voltage wave at the upper end of the liquid crystal display panel 1 in Fig. 14, and a second group of signal electrodes X2, X4 and X6 having applied the signal voltage wave at the lower end of the liquid crystal display panel in Fig. 14. As an example, the following description assumes that the liquid crystal panel 1 is of the so-called "positive display" type where a pixel turns dark when the applied effective voltage exceeds a certain threshold value.

When the display pattern shown in Fig. 14 is actually displayed, the pixels on the signal electrodes X3 and X5 will be brighter (less dark) in the upper portion and darker in the lower portion of the display panel. By contrast, the pixels formed on the signal electrodes X2, X4 and X6 will become brighter in the lower portion and darker in the upper portion of the display panel. In other words, the actually applied effective voltage becomes lower the nearer a pixel is located to the driving end of a signal electrode, i.e. the side to which the signal voltage wave is applied. By experiments on the unevenness of the display the following details have been found out.

Figs. 15(a) through (c) show each a voltage wave used to drive the liquid crystal panel of Fig. 14. In Fig. 15(a), the full line shows the voltage wave at the signal electrode X3 in the position of the pixel D31 in Fig. 14. The dotted line shows the voltage wave at the signal electrode X2 in the position of the pixel D21. In Fig. 15(a) and (c) the full line and the dotted line are drawn side by side to make them distinguishable, although they would be actually overlapping. Fig. 15(b) shows the voltage wave at the signal electrode X1 in the position of the scanning electrode Y1, i.e. corresponding to the position of pixels D21 and D31. Fig. 15(c) shows the vol-

tage difference between the voltage wave at the scanning electrode Y1 and the two voltage waves of Fig. 15(a), respectively, i.e. the full line in Fig. 15(c) corresponds to the voltage applied to the pixel D31 and the dotted line corresponds to the voltage applied to the pixel D21. The hatched portions in Fig. 15(c) show the difference between the voltages applied to the lighting pixel D31 and the non-lighting pixel D21, which is not the voltage difference causing the unevenness of display. In Fig. 15, V5, V3, V0 and V4 are lighting, non-lighting, selective and non-selective voltages of a first group of voltages, and V0, V2, V5 and V1 are the lighting, non-lighting, selective and non-selective voltages of a second group of voltages. The selective and non-selective voltages are applied to the scanning electrodes as scanning voltage wave, and the lighting and the non-lighting voltages are applied to the signal electrodes as the signal voltage wave. The first and second voltage groups are periodically switched. In this example, switching is performed each time when all the scanning electrodes Y1 through Y6 have been applied with the selective voltage (this cycle is called one frame, and two frames F1 and F2 are shown in the Fig.).

As shown in Fig. 15(a), since the distance between the pixel D31 and the driving end of the signal electrode X3 is short, in the position of pixel D31 there is almost no damping of the voltage wave, i.e. the signal voltage wave at the position of the pixel D31 substantially corresponds to the signal voltage wave applied to the driving end of the signal electrode X3. However, since the distance between the pixel D21 and the driving end of the signal electrode X2 is long, the signal voltage wave at the position of the pixel D21 exhibits a substantial damping or rounded edges. This damping is caused by an integrating circuit formed by the electrical resistance of the signal electrodes and the pixel capacitances having the liquid crystal as the dielectric. Therefore, when the voltage at the signal electrodes X1, X3 and X5 changes from the lighting (non-lighting) voltage to the non-lighting (lighting) voltage, a spike type noise is generated in the scanning electrode Y1 which is larger than that when the voltage at the signal electrodes X2, X4 and X6 is changed from the lighting (non-lighting) voltage to the non-lighting (lighting) voltage. The spike type noise generated in the scanning electrode Y1 by the said switching of the voltage at the signal electrodes X1, X3 and X5 dominates the spike type noise generated in the scanning electrode Y1 by the corresponding switching of the voltage at the signal electrodes X2, X4 and X6. Therefore, as shown by the full line voltage wave in Fig. 15(c), the effective voltage applied to the pixel D31 becomes lower than that applied to the pixel D21 which is represented by the dotted line.

The corresponding noise generated in the scanning electrode Y6 of Fig. 14 is dominated by the voltage switching at the signal electrodes X2, X4 and X6. Therefore, the effective voltage applied to the pixel D26 becomes lower than that applied to the pixel D36.

This will be explained in more general terms. The following definitions will be used: Yn designates the n-th scanning electrode from the upper side in Fig. 14. Xm designates the m-th signal electrode from left side in Fig. 14. Dmn designates the pixel formed at the crossing point of the signal electrode Xm and the scanning electrode Yn. As has been explained before, the signal electrodes are divided into two groups, a first group having the driving end at the upper side in Fig. 14 and a second group having the driving end at the lower side. When the pixels (Dmn, Dmn+1) formed between any of the signal electrodes (X1, X3, X5) of the first group and the scanning electrodes Yn and Yn+1 are both lighting, this is defined as a1, when both are non-lighting it is defined as b1. When of these pixels the pixel Dmn is lighting and the pixel Dmn+1 is non-lighting, it is defined as c1 and if the pixel Dmn is non-lighting and the pixel Dmn+1 is lighting, it is defined as d1.

Similarly, when the pixels (Dmn, Dmn+1) formed between any of the signal electrodes (X2, X4, X6) of the second group and the scanning electrodes Yn and Yn+1 are both lighting, it is defined as a2 and when they are both non-lighting it is defined as b2. When the pixel Dmn is lighting and the pixel Dmn+1 is non-lighting, it is defined as c2 while, when the pixel Dmn is non-lighting and the pixel Dmn+1 is lighting, it is defined as d2.

$N1_{ON}$ and $N1_{OFF}$ are the number of those pixels formed by the scanning electrode Yn and all signal electrodes of the first group, which are lighting and non-lighting, respectively. $M1_{ON}$ and $M1_{OFF}$ are the corresponding numbers of lighting and non-lighting pixels formed between the scanning electrode Yn+1 and the signal electrodes of the first group. $N2_{ON}$, $N2_{OFF}$, $M1_{ON}$ and $M2_{OFF}$ are the corresponding numbers of pixels formed with the signal electrodes of the second group.

With the above definitions, the following formulas hold true.

$$N1_{ON} = S(a1) + S(c1)$$
$$N1_{OFF} = S(b1) + S(d1)$$
$$M1_{ON} = S(a1) + S(d1)$$
$$M1_{OFF} = S(b1) + S(c1)$$

(S(a1) ... S(d1), S(a2) ... S(d2) means the number of the respective status a1, b1, etc.).

A numeric value I1 is defined as

$$I1 = S(c1) - S(d1)$$
$$= N1_{ON} - M1_{ON}$$

Similarly, with respect to the second group of signal electrodes

$$N2_{ON} = S(a2) + S(c2)$$
$$N2_{OFF} = S(b2) + S(d2)$$
$$M1_{ON} = S(a2) + S(d2)$$
$$M1_{OFF} = S(b2) + S(c2)$$

A numeric value I2 is defined as

$$I2 = S(c2) - S(d2) = N2_{ON} - M2_{ON}$$

Further, a function I(k) is defined as

$$I(k) = f(k) * I1 + f(L - k) * I2.$$

Herein, f(k) is a weighting function becoming smaller as k becomes larger. By the weighting function f(k) it is considered that the spike type noise generated by a signal electrode in a scanning electrode is the larger the nearer the scanning electrode is to the driving end of the respective signal electrode. L indicates the total number of scanning electrodes and k is $1 \leqq k \leqq L$.

A spike type noise according to the absolute value of the function I(k) is generated in the k-th scanning electrode Yk when the selection is moved from the scanning electrode Yn to the scanning electrode Yn+1. Namely, when the value of the function I(k) becomes larger, the noise will be larger. The direction of this noise depends on whether the value of the function I(k) is positive or negative. If the direction of the voltage of the spike type noise according to the function I(k) and the variation of the voltage wave applied to a signal electrode are in phase, the effective voltage applied to the pixel formed between this signal electrode and this scanning electrode Yk becomes lower to brighten the display. If the phases are opposite, the effective voltage becomes higher to darken the display.

With reference to Figs. 16 and 17 a further reason why even with the voltage correcting method an unevenness of the display remains will be explained.

Figs. 16 and 17 show the same liquid crystal panel with different display patterns. The liquid crystal panel 1 has the same structure as that of Fig. 14 and the same reference numerals are used. The scanning voltage wave is applied to the left side of the scanning electrodes Y1 through Y6 in Figs. 16 and 17. The scanning voltage wave varies dependent on the display pattern to improve an unevenness due to the "weft pulling" in accordance with a method described in the Japanese patent application 63-159914. That is, a correcting voltage is superimposed to the selective voltage in accordance with the number Z of lighting pixels on the scanning electrode to be selected. The display patterns in Fig. 16 and 17 are congruent quadrangles, positioned at the left end in Fig. 16 and at the right end in Fig. 17. Therefore, in order to achieve the display patterns of Figs. 16 and 17 according to the above method, completely the same correcting voltage will be applied to each scanning electrode Y1 through Y6.

In the case of Fig. 16 an unevenness in the displayed quadrangle will occur because of an excessive correcting voltage, that is the display will become darker horizontally. Contrary, in the case of Fig. 17, the correcting voltage is not sufficient so that the unevenness due to "weft pulling" cannot be avoided. In this case the display will become brighter horizontally. The reason for the above mentioned unevenness of the display is that the electrical resistance of each scanning electrode Y1 through Y6 together with the pixel capacitances form integration circuits influencing the voltage waveform along the scanning electrodes. The capacitance of a lighting pixel is larger than that of a non-lighting pixel. The influence of those integrating circuits causing a rounding of the edges of the voltage wave is the larger the farther the pixel is away from the driving end of the scanning electrode. Thus, for lighting pixels positioned at a distance from the driving end of the scanning electrode, the scanning voltage wave including the correcting voltage is rounded and the effective voltage applied to the pixel becomes lower.

This will be explained in more general terms in the following. If s is the number of scanning electrodes Y1 through Ys, an unevenness of the display by the "weft pulling" according to a numerical value Z′ calculated from the following formula is generated at the selected scanning electrode:

$$Z' = \sum_{i=1}^{p} q(i) * \delta(i)$$

wherein i designates the position of the pixel formed by the scanning electrode and the signal electrode Xi (i = 1, 2, 3, ... p), and p is the number of signal electrodes X1 through Xp.

The function q(i) is a weighting function increasing as i increases. The function $\delta(i)$ becomes 1 when the

pixel formed by the selected scanning electrode and the signal electrode Xi is lighting, and it becomes 0 when this pixel is non-lighting. Therefore, the numerical value Z′ represents the number of lighting pixels each weighted by its distance from the driving end of the scanning electrode.

As a result, a correcting voltage determined on the basis of the value Z obtained by the following formula cannot completely remove the unevenness of the display caused by the so-called "weft pulling".

$$Z = \sum_{i=1}^{p} \delta(i)$$

The unevenness of the display which is due to the above described reasons has caused a decrease in the quality of the display.

The document EP-A-0 345 399 discloses a drive method and a drive apparatus for gradation display on a capacitive display device such as an electroluminescence display device. This prior art aims at solving the problem caused by a high line resistance of transparent data signal electrodes. To that end the pulse width of the scanning pulses sequentially selecting the scanning electrodes increases as the selection progresses from the side at which the data signals are applied to the data signal electrodes to the opposite side.

The document JP-A-63-240528 discloses a method of driving a liquid crystal display panel wherein a display unevenness due to the display pattern is compensated for by applying a correction voltage to the scanning electrodes.

The invention as claimed is intended to remedy the above explained drawbacks of the prior art and to provide a liquid crystal display device having an improved evenness of the display and, thus, a better display quality, irrespective of the pattern or subject to be displayed.

According to a first aspect of the present invention, the liquid crystal display device comprises a liquid crystal panel having a pair of substrates sandwiching a liquid crystal layer therebetween, wherein one of the substrates is provided with a group of scanning electrodes and the other with a group of signal electrodes. The liquid crystal display device further comprises means for applying a scanning voltage wave to at least one end of the scanning electrodes and for applying a signal voltage wave to at least one end of the signal electrodes to display images, characters, etc. (display pattern), and means for superimposing a correcting voltage to at least one of the scanning voltage wave and the signal voltage wave in accordance with the display pattern, and means for varying the value of the correcting voltage in accordance with pixels' or the scanning electrode's distance from the driving end of the scanning electrodes and/or from the driving end of the signal electrodes.

According to a second aspect of the invention, the value of the correcting voltage is varied for each scanning electrode or each signal electrode.

The invention allows to supply a correcting voltage considering the relation between a display position within a display pattern and the driving end of an electrode.

Ways of carrying out the invention are described in detail below with reference to drawings which illustrate only specific embodiments, and in which:

Fig. 1	is a block diagram of a first embodiment of the invention,
Fig. 2	is a more detailed diagram showing the structure of the liquid crystal unit,
Fig. 3	is a diagram showing the structure of the scanning electrode driving circuit,
Fig. 4	is a block diagram showing the structure of the voltage correcting circuit,
Fig. 5	shows the power source circuit,
Fig. 6	is a perspective view of a liquid crystal panel displaying a specific display pattern,
Figs. 7(a) through (g)	show voltage waves applied to the liquid crystal panel to obtain the display pattern shown in Fig. 6,
Fig. 8	is a block diagram of a second embodiment of the invention,
Fig. 9	is a more detailed diagram of the liquid crystal unit of the second embodiment,
Fig. 10	is a block diagram showing the structure of the voltage correcting circuit,
Fig. 11	is a diagram of the power source circuit,
Fig. 12	is a perspective view of the liquid crystal panel displaying a specific display pattern,
Fig. 13	is a perspective view of the liquid crystal panel displaying a different display pattern,
Fig. 14	is a perspective view of a liquid crystal panel displaying a specific display pat-

tern, which is used for explaining the prior art,

Figs. 15(a) through (c) are voltage waves which according to the prior art are applied to the liquid crystal panel to obtain the display pattern of Fig. 14, and

Figs. 16 and 17 are perspective views of a liquid crystal panel showing two different display patterns which are used for explaining the prior art.

A first embodiment of the present invention will be described with reference to Figs. 1 to 7. As an example it will be shown how the present invention avoids an unevenness of the display when a chequered pattern is displayed.

Fig. 1 shows a block diagram of the first embodiment. In Fig. 1, 101 designates a liquid crystal unit details of which are shown in and will be explained with reference to Fig. 2. Numeral 102 designates a sequential control signal for controlling the operation of the liquid crystal display device, the sequential control signal including a latch signal LP, a frame signal FR, a data-in signal DIN, an X driver shift clock signal XSCL and others. Numeral 103 designates a data signal which determines the display pattern. Changes in the data signal 103 are synchronized with the leading edges of the signal XSCL. The data signal 103 is supplied to the liquid crystal unit 101 and to a voltage correcting circuit 104 at the trailing edges of the signal XSCL. Numeral 105 designates a power source circuit and numeral 108 a divider circuit for providing a clock signal 110 (referred to as correcting clock hereinafter) which is synchronized with the signal LP. Numeral 106 designates Y voltages, i.e. voltages for driving the scanning electrodes. Numeral 107 designates X voltages, i.e. voltages for driving the signal electrodes. Numeral 109 designates correcting signals output from the voltage correcting circuit 104.

Referring now to Fig. 2, the liquid crystal unit 101 is shown to comprise a liquid crystal panel 201, an Y driver 205 which is a circuit for driving the scanning electrodes, and an X driver 213 which is a circuit for driving the signal electrodes. The liquid crystal panel 201 comprises a pair of substrates 202 and 203 sandwiching a liquid crystal layer therebetween. Scanning electrodes Y1 through Y6 are arranged on the substrate 202 and signal electrodes X1 through X6 on the substrate 203. The signal electrodes X1 through X6 extend perpendicularly to the scanning electrodes Y1 through Y6. The signal electrodes X1, X3 and X5 have respective terminals for applying the signal voltage wave on the upper side of the liquid crystal panel (in Fig. 2), while the signal electrodes X2, X4 and X6 have their respective terminals on the lower side. A pixel 204 is formed at each crossing point between the scanning electrodes Y1 through Y6 and the signal electrodes X1 through X6. In the present embodiment, the liquid crystal panel is described to have six scanning electrodes and six signal electrodes forming 6 x 6 pixels. This is a relatively small number used for the sake of simplification of the explanation. In a practical embodiment, the number of signal and scanning electrodes may be higher.

The Y driver 205 comprises a shift register circuit 206, a shift register circuit 207, a latch circuit 208, a counter circuit 209, a coincidence detector circuit 210, a switch circuit 211 and a level shifter circuit 212. Each stage of the shift register circuit 207 has a plurality of bits which are shifted simultaneously, i.e. in parallel (in the present embodiment each stage has five bits).

A detailed diagram of the Y driver 205 is shown in Fig. 3. The shift register 206 is supplied with the signal DIN at the trailing edge of the signal LP and transfers the signal DIN sequentially into each of its stages at the following trailing edges of the signal LP. The signal DIN assumes a high electric potential "H" as the active "1" and is usually output once within an interval corresponding to the number of scanning electrodes Y1 through Y6 or the number of pulses of the signal LP which is equal to or higher than the number of scanning electrodes. Therefore, the data "1" is passed through the shift register 206 so that any time a control signal C0 output from one of the stages has the state "1" while those of the other stages have the state "0".

As mentioned before, each stage of the shift register 207 comprises five bits. This shift register is operated by a Y correcting shift clock (referred to a signal "YCSCL" hereinafter) to sequentially take in and shift the correcting signals 109. The correcting signals contain four bits IB0 through IB3 of an intensity signal and one sign bit F. The intensity signal determines the value of the correcting voltage and the sign bit determines the polarity of the correcting voltage.

The outputs of the shift register circuit 207 are taken into the latch circuit 208 under the control of the signal LP.

The counter circuit 209 is an up-counter, having a number of bits corresponding to the number of the intensity signal bits IB0 through IB3. The counter circuit 209 counts up the correcting clock 110 and is reset by the signal LP.

The coincidence detector circuit 210 includes a number of coincidence detectors corresponding to the number of stages of the shift register 207 and the latch circuit 208. Each coincidence detector compares the value in the respective stage of the latch circuit 208 with the output of the counter circuit 209. Each coincidence detector outputs a control signal C2 which changes from "0" to "1" when coincidence is detected. When the sign bit F which is output as control signal C1 is "1" indicating a negative value, the coincidence detectors detect the coincidence between the two's complement of the respective shift register value and the value of the output

of the counter circuit 209. The result of the detection is held until the following signal LP is received.

The switching circuit 211 receives the Y voltages 106 which are voltages V0, V1U, V1, V1L, V2, V3, V4U, V4, V4L and V5. These voltages are divided into a first voltage group consisting of V0, V4U, V4 and V4L, and a second voltage group consisting of V5, V1L, V1 and V1U. The switching circuit 211 switches from one to the other of the two voltage groups under the control of the signal FR.

The voltages V0, V4U, V4 and V4L are the selective voltage, the correcting voltage (U), the non-selective voltage and the correcting voltage (L) of the first voltage group. The voltages V5, V1L, V1 and V1U are the selective voltage, the correcting voltage (U), the non-selective voltage and the correcting voltage (L) of the second voltage group. The correcting voltages (U) and (L) are simply called the correcting voltage.

The level shifter circuit 212 contains a number of switches corresponding to the number of scanning lines Y1 to Y6, each switch having four input terminals S1 to S4 to be selectively connected to one output terminal.

When the control signal C0 is "1", each switch selects S1, namely the selective voltage. When the control signal C0 is "0" and the control signal C2 is "1", each switch selects S3, namely the non-selective voltage. When the control signals C0 and C2 are both "0", each switch selects S2 when the control signal C1 is "0" and selects S4, when the control signal C1 is "1".

The shift register circuit 207 has been described to be a five bit shift register for the intensity signal bits IB0 through IB3 and the sign bit F. It is possible, however, to increase or decrease the number of bits by varying the bit number of the intensity signal.

As shown in Fig. 3, the number of stages of the shift register circuits 206 and 207, the latch circuit 108, the coincidence detector circuit 210 and the switching circuit 211 is the same as the number of scanning electrodes Y1 through Y6 of the liquid crystal panel.

In the following the operation of the Y driver 205 constructed as explained above will be described.

In Fig. 3, the signal DIN is taken into the shift register 206 in synchronism with the signal LP and is then shifted to the respective next stage of the shift register circuit 206 with each following signal LP, that is in a cyclically changing manner the output (control signal C0) of one of the stages of the shift register circuit 206 is "1" while the outputs of the other stages are "0". That one of the switches of the switching circuit 212 receiving a "1" as control signal C0 outputs the selective voltage and is called the "selected switch", while the switches outputting other voltages are called "non-selected switches". In correspondence with the sequentially changing status of the shift register circuit 206, the level shifter circuit 212 outputs the selective voltage to a selected one of the scanning electrodes Y1 through Y6 and other voltages to the non-selected scanning electrodes.

The intensity signal IB0 through IB3 and the sign bit F are taken into the shift register circuit 207 under the control of the signal YCSCL. The correcting voltage (U) or (L) is output from each non-selected switch until the absolute value of the intensity signal IB0 through IB3 coincides with the count value of the counter 209 clocked by the correcting clock signal. The control signal C1 determines whether the correcting voltage (U) or the correcting voltage (L) is output. In other words, it is determined whether the sign bit F is "0" or "1". When the count value of the counter circuit 209 has reached the numerical value of the intensity signal, each non-selected switch outputs the non-selective voltage. Therefore, the non-selected switches output the correcting voltage for a time period which corresponds to the absolute value of the intensity signal.

Reference is made to Fig. 2 again to explain the X driver 213. It contains a shift register circuit 214, a latch circuit 215, and a level shifter circuit 216, each having a number of stages corresponding to the number of signal electrodes X1 through X6. The outputs of the level shifter circuit 216 are supplied to the signal electrodes X1 through X6, respectively.

The shift register circuit 214 receives the data signal 103 under the control of the signal XSCL as the clock. As mentioned before, the data signal 103 determines the display pattern, i.e. indicates lighting or non-lighting of the pixels (herein, lighting is referred to as active "1" and non-lighting as non-active "0"). When all the data corresponding to the signal electrodes X1 through X6, namely corresponding to one row of pixels, have been input into the shift register circuit 214, these data are taken into the latch circuit 215 under the control of the signal LP. The level shifter circuit 216 outputs predetermined voltages in accordance with the contents of the latch circuit 215 and the status of the frame signal FR. The X voltages 107 comprise voltages V0, V2, V3 and V5. Like the scanning voltages the X voltages are divided into a first voltage group of voltages V5 and V3 and a second voltage group of voltages V0 and V2. Depending on the status of the frame signal FR either the first or the second voltage group is selected corresponding to the selection of the first or second voltage group in the Y driver 205. The voltages V5 and V3 are the lighting voltage and the non-lighting voltage of the first voltage group and the voltages V0 and V2 are the lighting voltage and the non-lighting voltage of the second voltage group. If any of the stages of the latch circuit 215 outputs a "1", the corresponding stage of the level shifter circuit 216 outputs the lighting voltage of either voltage group depending on the signal FR to the respective signal electrode. If the output of the latch circuit is "0" the non-lighting voltage will be applied to the corresponding signal electrode.

As will be appreciated from the above description of the liquid crystal unit 101, it is synchronized with the signals DIN and LP and the scanning electrodes Y1 through Y6 are sequentially supplied with the selective voltage while the lighting or the non-lighting voltage, corresponding to the display pattern, is synchronously supplied to the signal electrodes X1 through X6 in order to achieve the display by means of the liquid crystal panel 201. To the scanning electrodes Y1 through Y6 which are not supplied with the selective voltage are instead of the non-selective voltage supplied the correcting voltage, having a length and polarity corresponding to the intensity signal I0 through I3 and the sign bit F of the correcting signal 109.

Having now described the structure and operation of the liquid crystal unit, the voltage correcting circuit 104 of Fig. 1 will be explained in more detail. The voltage correcting circuit counts the number of lighting pixels on a certain scanning electrode Yn and the number of lighting pixels on the following scanning electrode Yn+1 (n = 1, 2, ..., 5; n is cyclically changing so that if n = 6, n+1 will be 1 again). The difference between these two numbers is then obtained and individually output as the correcting signal for each scanning electrode Y1 through Y6 after having been weighted in consideration of the distance between the respective scanning electrode and the driving ends of the signal electrodes. A concrete example of the voltage correcting circuit 104 is given in Fig. 4 and will be explained in the following.

In Fig. 4, numeral 401 designates a toggle flipflop circuit (referred to as T-F/F hereinafter), numerals 402U and 402L designate gate circuits, numerals 403 and 404 counter circuits, numerals 405U and 405L function generator circuits, numerals 406U and 406L counter circuits, numerals 407U and 407L latch circuits, numerals 408U and 408L arithmetic circuit for carrying out a subtraction, numerals 409U and 409L memory elements, numerals 410U and 410L latch circuits, numerals 411U and 411L arithmetic circuits for carrying out a multiplication, and numeral 412 an arithmetic circuit for carrying out an addition and division.

The T-F/F circuit is reset to "0" by the signal LP. Its output terminal is connected to a non-inverting input terminal of the gate 402U and to an inverting input terminal of the gate 402L. The status of the T-F/F circuit is reversed each time a clock signal XSCL is input. Therefore, when a data signal corresponding to any of the even number signal electrodes X2, X4 and X6 is entered into the gate circuits 402U and 402L in Fig. 4, it is passed only by the gate circuit 402L since the gate circuit 402U is blocked by the output of the T-F/F circuit. Contrary, when a data signal corresponding to any of the odd number signal electrodes X1, X3 and X5 is entered into the gate circuits 402U and 402L in Fig. 4, it is passed only by the gate circuit 402U since in this case the gate circuit 402L is blocked by the output of the T-F/F circuit. The T-F/F circuit and the gate circuits 402U and 402L thus serve to separate the data signals corresponding to the top driven signal electrodes from the data signals corresponding to the bottom driven signal electrodes. (The top driven signal electrodes are those having their driving end in the upper portion of the liquid crystal panel 201 in Fig. 2, while the bottom driven signal electrodes have their driving end in the lower portion.) The separated data signals are defined as "upper data signal" and "lower data signal".

For each portion of the data signal corresponding to one row of pixels, the counters 406U and 406L separately count the number of the condition "1", i.e. the lighting condition, in the separated data signals. At the trailing edge of the signal XSCL the counters 406U and 406L carry out an addition only when the output of the gate 402U and the gate 402L, respectively, is "1". The count values of the counters 406U and 406L are defined as $M1_{ON}$ and $M2_{ON}$. These values are taken into the latch circuit 407U and 407L in synchronism with the signal LP. The values in the latch circuits 407U and 407L are defined as $N1_{ON}$ and $N2_{ON}$. Immediately before the count values of the counters 406U and 406L are transferred to the latch circuits 407U and 407L the arithmetic circuits 408U and 408L carry out a subtraction to obtain the differences:

$$I1 = N1_{ON} - M1_{ON},$$
$$I2 = N2_{ON} - M2_{ON}.$$

These differences are separately obtained and stored for each pair of successive scanning electrodes to be used for determining the correcting voltages applied to the non-selected scanning electrodes when the second one of a respective pair of successive scanning electrodes is selected.

The counter 403 is an up-counter circuit serving as an address generator for generating addresses for the memory elements 409U and 409L corresponding to the number of scanning electrodes Y1 through Y6. In the present example the counter counts from 0 to 5 and is reset to 0 by the signal DIN. The address output from the counter 403 is 0 when the differences I1 and I2 calculated by the arithmetic circuits 408U and 408L are those for the first and the second scanning line, i.e. Y1 and Y2 in the present example. Similarly, the address output from the counter 403 is 1 when the differences I1 and I2 are those for the second and the third scanning lines Y2 and Y3, etc. The above mentioned numerical values I1 and I2 are thus written in the memory elements 409U and 409L under the addresses indicated by the counter 403.

This operation will be explained in more detail. The counters 406U and 406L count the number of lighting pixels $M1_{ON}$ and $M2_{ON}$ on the scanning electrode Yn+1 while the selective voltage is applied to the scanning electrode Yn. At this time the number of lighting pixels $N1_{ON}$ and $N2_{ON}$ on the scanning electrode Yn is held

in the latch circuits 408U and 408L. Shortly before the selective voltage is applied to the scanning electrode Yn+1, the differences I1 and I2 are calculated and written into the memory elements 409U and 409L under the address of n-1. This operation is repeated by cyclically changing the value of n through 1 to 6, that is, in the memory elements 409U and 409L the differences I1 and I2 of the number of lighting pixels on the scanning electrodes Y1 and Y2 are stored under the address of 0. Under the addresses of 1 through 5 the differences I1 and I2 between the numbers of lighting pixels on each pair of scanning electrodes Y2 and Y3, Y3 and Y4, Y4 and Y5, and Y5 and Y1 are stored.

The counter 404 is an up-counter circuit which in the present example counts from 0 to 5 and is reset to 0 by the signal LP. In other words, the possible number of count values of the counter 404 corresponds to the number of scanning electrodes Y1 through Y6. The clock input to the counter 404 (this clock is referred to as "signal YCSCL") can be any clock whose frequency relation with respect to the signal LP is s:1 when s is the number of scanning electrodes (s = 6 in the present example). In the present embodiment, the signal XSCL fulfils this condition and is used as the signal YCSCL. The output of the counter 404 is used as a variable for the function generator circuit 405U and 405L.

The function generator circuits 405U and 405L contain a numerical value table provided in a read-only memory (referred to as "ROM" hereinafter) and a diode matrix. The output of these circuits is the value of a function of the input variable. The function generator circuit 405U contains the table for returning the value of the function f(k) (wherein k designates the variable which may also be considered as an address). The value of the function f(k) decreases as the variable k increases. f(k) is the weighting function used for considering the influence of the distance between a respective scanning electrode and the driving ends of the signal electrodes. The function values may be obtained, for example, from an experiment. For the sake of simplification, the function as described below varies linearly with the input variable k:

k = 0, f(0) = 15
k = 1, f(1) = 14
k = 2, f(2) = 13
k = 3, f(3) = 12
k = 4, f(4) = 11
k = 5, f(5) = 10

Similarly, the function generator circuit 405L returns upon input of a variable k the value of the function f(L-k). Herein, L designates the number of the scanning electrodes minus 1, i.e. in the present example L = 5.

While the selective voltage is applied to the scanning electrode Yn of the liquid crystal panel 201, the arithmetic circuits 411U and 411L in Fig. 4 multiply the values stored in the memory elements 409U and 409L under the address (n-1) indicated by the counter 403 with the values returned by the function generator circuits 405U and 405L, respectively. Since the counter 404 is up-counted by the signal YCSCL, the value output from the function generator circuits 405U and 405L is varied in synchronism with the signal YCSCL. In other words, the result of the operation of the arithmetic circuits 411U and 411L becomes as listed below and is synchronized with the signal YCSCL.

f(0) * I1, f(5) * I2
f(1) * I1, f(4) * I2
f(2) * I1, f(3) * I2
f(3) * I1, f(2) * I2
f(4) * I1, f(1) * I2
f(5) * I1, f(0) * I2

These results are added by the arithmetic circuit 412 and then divided by four. Thus, during the period during which the selective voltage is applied to the scanning electrode Yn, the following results I synchronized with the signal YCSCL are obtained.

$$I = \{f(0) * I1 + f(5) * I2\}/4$$
$$I = \{f(1) * I1 + f(4) * I2\}/4$$
$$I = \{f(2) * I1 + f(3) * I2\}/4$$
$$I = \{f(3) * I1 + f(2) * I2\}/4$$
$$I = \{f(4) * I1 + f(1) * I2\}/4$$
$$I = \{f(5) * I1 + f(0) * I2\}/4$$

The reason why the division by four is made is because the shift register circuit 107 in Fig. 3 is structured with only four bits, excepting the sign bit F, to store the intensity signal within the range of 0 to 15. The division by four, thus, is related to the specific embodiment only and not substantial.

In more general terms, the differences I1 and I2 of the number of lighting pixels on the scanning electrodes Yn and Yn+1 are multiplied with f(n-1) and f(L-n+1), respectively, the results of the multiplication are added to I = f(n-1) * I1 + f(L-n+1) * I2 under the timing of the signal YCSCL while the scanning electrode Yn of the

liquid crystal panel 201 is selected. The result comprising the intensity signal with bits IB0 through IB3 and the sign bit F is then output as the correcting signal 109 synchronized with the signal YCSCL. It should be noted that the structure of the voltage correcting circuit 104 is not limited to the above explained one. For example, instead of calculating the result I on a real-time basis, it would be possible to calculate it previously by a CPU, write it into a memory provided for this purpose and read out the correcting signal 109 under the control of the address counter 404.

An example of a concrete structure of the power source circuit 101 of Fig. 1 is shown in Fig. 5. In this Figure, numerals 501 through 509 designate resistors which are connected in series to form a voltage divider circuit. Voltages V0 and V5 are applied to the ends of this series connection. The voltages V1U, V1, V1L, V2, V3, V4U, V4 and V4L are taken off the taps of the voltage divider circuit. The resistors are selected to fulfil the following conditions:

$$\begin{aligned} V &= V0 - V1 \\ &= V1 - V2 \\ &= V3 - V4 \\ &= V4 - V5 \\ V1U - V1 &= V4 - V4L \\ V1 - V1L &= V4U - V4 \end{aligned}$$

(wherein V2 - V3 = a x V, a is a constant value in the range of 1 through 50).

510 in Fig. 5 designates voltage stabilizing circuits used to decrease the impedance of the voltage sources provided by the resistors 501 through 509. The voltage stabilizing circuits are provided with a voltage follower circuit comprising an operation amplifier and a transistor emitter follower. As shown in Fig. 5, a voltage stabilizing circuit 510 is connected between each tap of the voltage divider circuit and the output.

The voltages V1U, V1, V1L, V4U, V4 and V4L are supplied to the liquid crystal unit 101 in Fig. 1 as the Y voltages 106 and the voltages V0, V2, V3 and V5 as the X voltages 107.

The circuit 108 in Fig. 1 generates the correcting clock 110 synchronized with the signal LP. The correcting clock 110 may be formed for example by dividing the signal XSCL or by means of a PLL circuit. The correcting clock 110 is not required to have a specific cycle, for example it is possible to change the cycle being however synchronized with the signal LP. The cycle of the correcting clock can be obtained, for example, by an experiment. In the present example it is formed to have sixteen cycles within one cycle of the signal LP.

Having now described the construction and the operation of the different units of the first embodiment of the present invention, the operation will now be explained with respect to a specific case, namely the display of a chequered pattern on the liquid crystal panel 201, as it is shown in Fig. 6 . In Fig. 6, the hatched pixels are lighting while the others are non-lighting.

The voltage correcting circuit 104 in Fig. 1 separately counts the number $M1_{ON}$ of lighting pixels among the pixels formed by the scanning electrode Yn+1 and the top driven signal electrodes X1, X3 and X5 on the one hand and the number $M2_{ON}$ of the lighting pixels among the pixels formed by the scanning electrode Yn+1 and the bottom driven signal electrodes X2, X4 and X6 on the other hand during the time during which the signal electrode Yn is selected. At that time, the corresponding numbers $N1_{ON}$ and $N2_{ON}$ separately counted during the previous period are held in the latch circuits 407U and 407L, respectively. The voltage correcting circuit 104 calculates the differences I1 and I2 between these numbers as follows

$$\begin{aligned} I1 &= N1_{ON} - M1_{ON} \\ I2 &= N2_{ON} - M2_{ON} \end{aligned}$$

and writes these differences into the memory elements 409U and 409L under the address of (n-1). This is repeated for n = 1, 2, 3, 4, 5 and 6. Therefore, the corresponding differences I1 and I2 for all scanning electrodes Y1 through Y6 are written into the memory elements 409U and 409L. In the case of the display pattern in Fig. 6, the values written into the memory element 409U are -2, 2, -2, 2, -2, 2, and those written into the memory element 409L are 2, -2, 2, -2, 2, -2, in each case sequentially from the address 0 to 5. The arithmetic operation {f(k-1) * I1 + f(L-k+1) * I2 (wherein k = 1, 2, ..., 6) is carried out on the differences I1 and I2 in parallel to the writing operation in the memory elements 409U and 409L, and the results are sequentially transferred to the shift register circuit 207 in the Y driver 205 in Fig. 2.

Taking n = 3 as an example, the difference values in the memory elements 409U and 409L under the address n-1 = 2 are -2 and 2, respectively. Then, the following calculations are performed and the results are transferred to the shift register circuit 207 shortly before the scanning electrode Y4 is selected:

$$\begin{aligned} I &= \{f(0) * I1 + f(5) * I2\}/4 \\ &= \{15 * (-2) + 10 * 2\}/4 \\ &\approx -3 \\ I &= \{f(1) * I1 + f(4) * I2\}/4 \\ &= \{14 * (-2) + 11 * 2\}/4 \end{aligned}$$

$$\approx -2$$

$$I = \{f(2) * I1 + f(3) * I2\}/4$$
$$= \{13 * (-2) + 12 * 2\}/4$$
$$\approx -1$$

$$I = \{f(3) * I1 + f(2) * I2\}/4$$
$$= \{12 * (-2) + 13 * 2\}/4$$
$$\approx 1$$

$$I = \{f(4) * I1 + f(1) * I2\}/4$$
$$= \{11 * (-2) + 14 * 2\}/4$$
$$\approx 2$$

$$I = \{f(5) * I1 + f(0) * I2\}/4$$
$$= \{10 * (-2) + 15 * 2\}/4$$
$$\approx 3$$

As will be appreciated, in the above calculations the absolute values are rounded to integers.

The above values are taken in the latch circuit 208 when the scanning electrode Y4 is selected at the leading edge of the signal LP. The counter 209 is reset to 0 simultaneously and then counted up by the correcting clock 110.

In the present example, when the scanning electrode Yn+1, i.e. the scanning electrode Y4 is selected, the switches of the level shifter circuit 204 select S4 (correcting voltage (L)), S2 (correcting voltage (U)), S4 (correcting voltage (L)), S1 (selective voltage), S4 (correcting voltage (L)) and S2 (correcting voltage (U)) to output these voltages to the scanning electrodes Y1 through Y6 of the liquid crystal panel 201, respectively.

Each switch selecting S2 or S4 keeps this selection until the output of the counter 209 coincides with the value indicated by the associated stage of the latch circuit 208. When this coincidence occurs, each switch selects S3 to output the non-selective voltage. As mentioned earlier, whether the correcting voltage (U) or (L) is output depends on the sign bit F, i.e. on whether the numerical value I is positive or negative. The correcting voltages are applied instead of the non-selective voltage for the period of time for which the absolute value of I is larger than the count value of the counter 209.

The X driver 213 operates to supply the lighting voltage if the pixel formed by the respective one of the signal electrodes X1 through X6 on the selected scanning electrode Y4 is lighting and to supply the non-lighting voltage if it is non-lighting.

The voltage wave applied to the scanning electrodes Y1 through Y6 and the signal electrodes X1 through X6 of the liquid crystal panel 201 when the display pattern is as shown in Fig.6, are shown in Fig. 7(a) through (g) to explain the operation in more detail. In Fig. 7(a) the full line shows the voltage wave at the signal electrodes X3 and X5 in the positions of the pixels D31 and D51 in Fig. 6. The broken line shows the voltage wave at the signal electrodes X2 and X4 in the positions of the pixels D21 and D41. In Fig. 7(b) the full line shows the voltage wave applied to the scanning electrode Y1, and the broken line shows the noise occurring at the scanning electrode Y1 in the position of the pixel D31. Similarly, Fig. 7(c) shows the voltage wave applied to the scanning electrode Y2 and the noise occurring at this scanning electrode in the position of the pixel D32. Figs. 7(d) to (g) show the corresponding voltage waves at the scanning electrodes Y3 to Y6 and the noises occurring at these scanning electrodes in the position of the pixels D33 to D36, respectively. As can be seen from Figs. 7(a) to (g), the variation of the voltage wave shown by the full line in Fig. 7(a) induces noises in the scanning electrodes Y1, Y2 and Y3 positioned on the upper side of the liquid crystal panel of Fig. 6, the noises being strongest in the scanning electrode Y1 and are decreasing in the order of Y1, Y2 and Y3. Similarly, the variations of the voltage wave at the bottom driven signal electrodes X2 and X4 induce noises in the scanning electrodes Y6, Y5 and Y4 positioned on the lower side of the liquid crystal panel, the noises being strongest in the scanning electrode Y6 and are decreasing in the order of Y6, Y5 and Y4. As is shown by the full line in Fig.7(b) through (g), the noises or wave turbulences occurring at the scanning electrodes Y1 through Y6 are compensated for by the Y driver 205 outputting instead of the non-selective voltage the correcting voltage (U) or (L) in a direction opposite to that of the noise. The time during which the non-selective voltage is replaced by the correcting voltage is increased or decreased in accordance with the degree of the respective noise in each of the scanning electrodes Y1 through Y6. That is, the correcting voltage is supplied for a long period of time in case of a large noise or turbulence and is supplied for a short period of time in case of a small noise or turbulence. After that time, the non-selective voltage is applied. Therefore, the noises generated in each scanning electrode Y1 through Y6 can be substantially reduced. Thereby, the difference of the effective voltage applied to each pixel of the liquid crystal panel can be reduced and the problem of an uneven display solved.

The above description of the first embodiment of the invention has been given in connection with a liquid crystal panel in which the signal electrodes X1 through X6 are alternately top and bottom driven, i.e. the odd number signal electrodes are top driven and the even number signal electrodes are bottom driven. A possible

modification of this first embodiment of the invention is to have all signal electrodes either top driven or bottom driven. Assuming the case of exclusively top driven signal electrodes as an example, the explained first embodiment of the invention could be easily adapted to such case by supplying a signal which is constantly "1" to the gate circuits 402U and 402L in Fig. 4 instead of the output of the T-F/F 401. In fact, the circuits 402L and 406L through 410L are superfluous in such a case and could either be made inoperative or omitted. Also, the circuit 405L would not be necessary in this case and even the circuit 412 could be omitted since the output from the circuit 411L would be always "0". Thus, the numerical value I output from the voltage correcting circuit 104 would be

$$I = (I1 + I2) * f(k).$$

The remaining construction and operation of this modification would be the same as with the first embodiment.

Instead of using either alternately arranged top and bottom driven signal electrodes according to the first embodiment of the invention or exclusively top or bottom driven signal electrodes as with the above first modification of the first embodiment, the signal voltage wave could be supplied to both ends of each signal electrode according to a second modification of the first embodiment of the present invention. In this case, for calculating the value I, a function $g(|k-L/2|)$ can be substituted for the function f(k) of the first embodiment. The function g(x) is a function which increases as the variable x ($x \equiv |k-L/2|$) increases. With the value I obtained in this way, the remaining operation of the second modification is the same as with the first embodiment.

In the first embodiment the noise compensation or elimination is performed by using a method for adjusting the correcting amount, in which the difference between the correcting voltage and the non-selective voltage is constant and the time period during which the correcting voltage is applied is increased or decreased depending on the strength of the noise. This correction is referred to as "time axis correction". Instead of such time axis correction a "voltage axis correction" could be employed by keeping the time period during which the correcting voltage is applied constant and varying the difference between the correcting voltage and the non-selective voltage in accordance with the strength of the noise. It is also possible to vary both, the time of application of the correcting voltage and the voltage itself which would be a "time voltage axis correction". It is also possible to use as the correction voltage a waveform following an exponential function and to vary the wave height in accordance with the required correction amount, and the waveform of a triangle (this is defined as "function waveform correction").

Referring to Figs. 8 to 13, a second embodiment of the invention will be explained next to show how the unevenness of the display caused by the weft pulling can be avoided.

As described above, the degree of the unevenness of the display on a scanning line Yn caused by the weft pulling corresponds to the value Z′(Yn) defined by the following formula:

$$Z'(Yn) = \sum_{i=1}^{p} q(i) * \delta(i)$$

(wherein i designates the position of the pixel formed by the scanning electrode Yn and the signal electrode Xi (i = 1, 2, ..., p) and Yn is the selected scanning electrode among the scanning electrodes Y1 through Ys). In other words, the effective voltage applied to a pixel on the scanning electrode is lower than a desired value by a value corresponding to Z′. Therefore, a correction can be carried out by calculating the value Z′ for each of the scanning electrodes Y1 through Ys and by correcting the applied voltage in correspondence with the calculated value Z′ when the liquid crystal display device is operated.

Fig. 8 is a block diagram of a second embodiment of the present invention which is based on this principle. Numerals 102 and 103 in Fig. 8 designate the control signal and the data signal which correspond to those of the first embodiment so that any further explanation will be omitted here. Numeral 801 designates the liquid crystal unit. Numeral 804 is a voltage correcting circuit which calculates the value Z′ and generates a correcting signal 809 which becomes active during a time period corresponding to the calculated value Z′. Numeral 805 is the power source circuit. It supplies Y voltages 806 and X voltages 107 to the liquid crystal unit 801.

An example of a concrete structure of the liquid crystal unit 801 is shown in Fig. 9. Herein, 201 designates the liquid crystal panel which is the same as that of the first embodiment. 805 is the scanning electrode driving circuit (referred to as "Y driver" hereinafter) comprising the shift register circuit 206, a switch circuit 911 and a level shifter circuit 912. The output terminals of the individual stages of the level shifter circuit 912 are connected to the scanning electrodes Y1 through Y6 of the liquid crystal panel 201, respectively. The shift register circuit 206 is the same as that of the first embodiment and, therefore, its explanation is omitted. According to

the frame signal FR, the switch circuit 911 selects one of two groups of voltages which form the Y voltages 806.

The Y voltages include the voltages V0′, V1, V4 and V5′ of which V0′ and V4 form the first voltage group and V5′ and V1 the second voltage group. V0′ and V4 are the selective voltage and the non-selective voltage, respectively, of the first voltage group. Similarly, V5′ and V1 are the selective voltage and the non-selective voltage, respectively, of the second voltage group. The voltages of the selected group are supplied by the switch circuit 911 to the level shifter circuit 912.

The level shifter circuit 912 comprises a number of switches corresponding to the number of scanning electrodes, each switch having two input terminals and one output terminal. Which of the input terminals is connected to the output terminal depends on the state of the control signal applied from the shift register 206 to the respective switch. When the state is "1" each switch selects the selective voltage to apply it to the corresponding one of the scanning electrodes Y1 through Y6. When the state is "0" each switch selects the non-selective voltage and applies this to the respective scanning electrode.

Having described the structure of the Y driver, its operation will be explained next.

The signal DIN is taken into the shift register 206 in synchronism with the signal LP and is then successively shifted to each stage of the shift register by the following signals LP. In response thereto, the switches of the level shifter circuit 912 are sequentially selected to output the selective voltage while the non-selected switches output the non-selective voltage.

The signal electrode driving circuit 213 (referred to as "X driver" hereinafter) is the same as that of the first embodiment and, therefore, its explanation is omitted.

The liquid crystal unit 801 is synchronized with the signals DIN and LP, and the scanning electrodes Y1 through Y6 are sequentially supplied with the selective voltage while the lighting or non-lighting voltage corresponding to the display pattern is applied to the signal electrodes X1 through X6 in synchronism with the selection of the scanning electrodes to display the display pattern on the liquid crystal panel 201.

The voltage correcting circuit 804 calculates the following formula for each of the scanning electrodes Y1 to Y6:

$$Z' = \sum_{i=1}^{6} q(i) * \delta(i) \qquad \ldots (1)$$

wherein i designates the position of the pixel formed between the scanning electrode for which Z′ is calculated and the signal electrode Xi (i = 1, 2, ..., 6). In the time period during which the scanning electrode Yn is selected, Z′ is calculated for the scanning electrode Yn+1 which is the next to be selected. The voltage correcting circuit 804 outputs an active correcting signal 809 for a duration corresponding to the value Z′ in synchronism with the signal LP when the scanning electrode Yn+1 is selected.

A concrete example of the voltage correcting circuit 804 is shown in Fig. 10. Herein, numeral 1001 designates a counter, numeral 1002 a function generator circuit, numeral 1003 a gate circuit, numeral 1004 an arithmetic circuit, numeral 1005 a first latch circuit, numeral 1006 a second latch circuit and numeral 1007 a correcting signal generator circuit.

The counter 1001 is reset to 0 by the signal LP and counted up by the signal XSCL. The output of the counter 1001 is supplied as an address or as a variable to the function generator circuit 1002.

The function generator circuit 1002 is provided with a ROM and a diode matrix and outputs predetermined values depending of the count value of the counter 1001. The value output by the function generator circuit 1002 corresponds to the function q(i) in the formula (1), i.e. to the weighting function. The output of the function generator 1002 increases as the count value of the counter 1001 increases. It should be noted that i corresponds to the count value of the counter 1001 plus 1.

The values returned by the function generator 1002 can be obtained from an experiment and, in the present example, are simply defined as follows:

i = 1, q(1) = 1
i = 2, q(2) = 1.1
i = 3, q(3) = 1.2
i = 4, q(4) = 1.3
i = 5, q(5) = 1.4
i = 6, q(6) = 1.5

The gate circuit 1003 generates the logical product of the value output from the function generator circuit 1002 and the data signal 1003. Namely, it outputs the value of the function generator circuit 1002 when the data signal is "1" and outputs 0 when the data signal is "0". The gate circuit 1003 thus produces the product $q(i) * \delta(i)$ of the formula (1). Herein, i is the number of trailing edges occurring in the signal XSCL after a trailing edge of the signal LP, and it corresponds to the count value of the counter 1001 plus 1.

The arithmetic circuit 1004, in synchronism with the signal XSCL, adds the value output from the gate circuit 1003 to the value kept in the first latch circuit 1005 and returns the result into the first latch circuit 1005.

The first latch circuit 1005 holds the result from the arithmetic circuit 1004. The first latch circuit 1005 is reset to 0 by the signal LP. Immediately before it is reset, the contents of the latch circuit 1005 corresponds to the value Z′ of the above formula (1), namely to the number of lighting pixels on the scanning electrode which is to be selected next, each lighting pixel being weighted according to its position on the scanning electrode.

Immediately before the first latch circuit is reset at the trailing edge of the signal LP, its contents is taken into the second latch circuit 1006. Since the following scanning electrode is selected at the trailing edge of the signal LP, the value kept by the second latch circuit 1006 corresponds to the weighted number of lighting pixels on the currently selected scanning electrode.

The correcting signal generator circuit 1007 outputs in synchronism with the signal LP a correcting signal 809 of active "1" during a period of time corresponding to the value kept by the second latch circuit 1006.

To achieve such function, the circuit 1007 comprises for example a counter 1008 which is used to generate a correcting clock signal which may be either the signal XSCL, a signal obtained by dividing or doubling the signal XSCL or another clock signal. A counter 1009 is reset to 0 by the signal LP and then counts the correcting clock. A coincidence detector circuit 1010 generates the active "1" correcting signal 809 until the count value of the counter 1009 coincides with the value kept by the second latch circuit 1006. It should be noted that the interval of the cycle of the correcting clock is not required to be constant and may be determined by an experiment for example.

With the above described construction of the voltage correcting circuit, the number of lighting pixels on the scanning electrode to be selected next is counted wherein each lighting pixel is weighted in the manner explained above, and the correcting signal assumes the active state "1" for a period corresponding to the value Z′ synchronized with the signal LP by which the next scanning electrode is selected.

Fig. 11 shows an example of the concrete structure of the power source circuit 805 of Fig. 8. 1101 through 1107 designate resistors which are connected in series to form a voltage divider circuit. Voltages V0U and V5L are applied to the two ends of this series connection. Voltages V0, V1, V2, V3, V4 and V5 are derived from the taps of the voltage divider circuit. The resistance values of the resistors 1101 through 1107 are selected to fulfil the following conditions:

$$\begin{aligned} V &= V0 - V1 \\ &= V1 - V2 \\ &= V3 - V4 \\ &= V4 - V5 \\ V0U - V0 &= V5 - V5L \end{aligned}$$

wherein $V2 - V3 = a * V$, a is a constant value in the range of 1 through 50.

510 in Fig. 11 designates voltage stabilizing circuits which are the same as those of the first embodiment and, thus, will not be further explained.

Numerals 1108 and 1109 are switch circuits of which the switch circuit 1008 selects the voltage V0U when the correcting signal 809 is "1" and selects the voltage V0 when it is "0" and outputs the selected voltage as voltage V0′. Similarly, the switch 1109 selects the voltage V5L when the correcting signal 809 is "1" and selects the voltage V5 when it is "0" and outputs the selected voltage as voltage V5′. The voltages V0U and V5L are the correcting voltages.

The voltages V0′, V4, V5′ and V1 are supplied to the liquid crystal unit 801 as the Y voltages 806, and the voltages V0, V2, V3 and V5 are supplied to the liquid crystal unit as the X voltages 107.

The operation of the second embodiment of the present invention will now be explained with reference to the specific display patterns shown in Figs. 12 and 13 as an example. Figs. 12 and 13 show the liquid crystal panel 201 of Fig. 9 displaying a quadrangle. In Figs. 12 and 13, the lighting pixels are hatched and the non-lighting pixels are not hatched. In Fig. 12 the quadrangle is displayed on the left side and in Fig. 13 on the right side.

When the display pattern of Fig. 12 or Fig. 13 is displayed, the voltage correcting circuit 804 in Fig. 8 counts the number of lighting pixels on each of the scanning electrodes Y1 through Y6 with each lighting pixel being weighted according to its position, to obtain the value Z′. The following values Z′ are obtained (in the following, Z′(Yn) refers to the value Z′ for the scanning electrode Yn with n = 1, 2, ..., 6).

Fig. 12:

$$Z'(Y1) = 0 + 0 + 0 + 0 + 0 + 0 = 0$$
$$Z'(Y2) = 1.0 * 1 + 1.1 * 1 + 0 + 0 + 0 + 0 = 2.1$$
$$Z'(Y3) = 1.0 * 1 + 1.1 * 1 + 0 + 0 + 0 + 0 = 2.1$$
$$Z'(Y4) = 1.0 * 1 + 1.1 * 1 + 0 + 0 + 0 + 0 = 2.1$$
$$Z'(Y5) = 1.0 * 1 + 1.1 * 1 + 0 + 0 + 0 + 0 = 2.1$$
$$Z'(Y6) = 0 + 0 + 0 + 0 + 0 + 0 = 0$$

Fig. 13:

$$Z'(Y1) = 0 + 0 + 0 + 0 + 0 + 0 = 0$$
$$Z'(Y2) = 0 + 0 + 0 + 0 + 1.4 * 1 + 1.5 * 1 = 2.9$$
$$Z'(Y3) = 0 + 0 + 0 + 0 + 1.4 * 1 + 1.5 * 1 = 2.9$$
$$Z'(Y4) = 0 + 0 + 0 + 0 + 1.4 * 1 + 1.5 * 1 = 2.9$$
$$Z'(Y5) = 0 + 0 + 0 + 0 + 1.4 * 1 + 1.5 * 1 = 2.9$$
$$Z'(Y6) = 0 + 0 + 0 + 0 + 0 + 0 = 0$$

Each scanning electrode receives as the selective voltage the correcting voltage V0U and V5L instead of the voltages V0 and V5, respectively, for a period of time which corresponds to the respective value of Z′, i.e. as long as the correcting signal 809 is "1".

The value Z′ for the scanning electrodes Y2 through Y5 in case of the display of Fig. 12 is smaller than that in case of the display of Fig. 13. Therefore, under the display in Fig. 12 the time period during which the correcting voltages V0U and V5L are applied as the selective voltage becomes shorter than that in case of the display of Fig. 13, when the scanning electrodes Y2 through Y5 are selected. The Y driver 905 sequentially applies the selective voltage to the scanning electrodes Y1 through Y6 while the X driver 213 applies the lighting or the non-lighting voltage to the signal electrodes in accordance with the display pattern.

With the second embodiment of the present invention, to display a display pattern as shown in Fig. 12, a selective voltage having a smaller amount of correction is supplied to the selected scanning electrode in accordance with the fact that the rounding of the voltage wave at the scanning electrode is not so strong when the lighting pixels are positioned near to the driving end of the scanning electrode as is the case with the scanning electrodes Y2 through Y5 in Fig. 12. That is, the correcting voltages V0U and V5L are supplied instead of the voltages V0 and V5, respectively, for a relatively short time only. Contrary, in the example of Fig. 13 a selective voltage having a larger amount of correction is supplied to the selected scanning electrode since in this case the rounding of the voltage wave at the scanning electrode is stronger because the lighting pixels are positioned farther away from the driving end of the scanning electrode in case of the scanning electrodes Y2 through Y5. Thus, in this case, the correcting voltages V0U and V5L are supplied instead of the voltages V0 and V5, respectively, for a longer time. The position of lighting pixels can thus be taken into account and compensated for in order to obtain a display without unevenness.

The second embodiment of the invention has been described in connection with a liquid crystal panel in which the scanning voltage wave is supplied to one end of each scanning electrode. As a modification of the second embodiment, the scanning voltage wave can be applied to both ends of each scanning electrode. In such a case, the function $p(|i-S/2|)$ must be substituted for the function q(i) for calculating the value Z′. The function p(x) is a weighting function which decreases as i ($i \equiv |i-S/2|$) increases. With such a modification of the second embodiment of the invention, similar effects will be obtained.

As a method for adjusting the correction amount in the second embodiment of the invention, it has been described to increase or decrease the time period during which the normal selective voltage is replaced by a predetermined correcting voltage, i.e. a time axis correction has been described. It should be noted that instead of such time axis correction a voltage axis correction, a time voltage axis correction or a function waveform correction could be employed.

According to the first embodiment of the invention and its modifications, the non-selective voltage is varied, whereas according to the second embodiment and its modifications the selective voltage is varied. Therefore, the two embodiments can be used together in order to achieve optimum results for varyious display patterns.

Claims

1. A liquid crystal display device, comprising:

a liquid crystal panel (201; 801) provided with a pair of substrates (202, 203) sandwiching a liquid crystal layer therebetween,

a scanning electrode group (Y1-Y6) on one of said substrates,

a signal electrode group (X1-X6) on the other of said substrates, a pixel being formed at each crossing point between a scanning electrode and a signal electrode, and

means (205, 213; 905, 213) for applying a scanning voltage wave to at least one end of said scanning electrode group and for applying a signal voltage wave to at least one end of said signal electrode group to display a display pattern and for superimposing a correcting voltage to the scanning voltage wave and/or the signal voltage wave in accordance with the display pattern,

characterized by

means (104; 804) for varying the value and/or the time of application of said correcting voltage in accordance with the pixel positions from said at least one end of said scanning electrode group and/or in accordance with the pixel positions from said at least one end of the signal electrode group.

2. The liquid crystal display device according to claim 1, wherein the value and/or the application time of said correcting voltage is selectively varied for each electrode of said scanning electrode group and/or for each electrode of said signal electrode group.

3. The liquid crystal display device according to claim 2, wherein a selective voltage is successively and periodically applied to each electrode of said scanning electrode group (Y1-Y6), a non-selective voltage being applied to the other electrodes of said scanning electrode group, and wherein said correcting voltage is superimposed on the non-selective voltage, the voltage times time area of the correcting voltage being separately controlled for each scanning electrode (Y1-Y6) depending on the display pattern and the distance between the respective scanning electrode and said at least one driving end of the signal electrode group (X1-X6).

4. The liquid crystal display device according to claim 2 or 3, wherein a selective voltage is successively and periodically applied to each scanning electrode (Y1-Y6), the correcting voltage being superimposed on said selective voltage and the voltage times time area of the correcting voltage being individually controlled for each scanning electrode depending on the lighting or non-lighting status of the pixels on a respective scanning electrode and the distance between each of said pixels and said at least one driving end of the scanning electrode group.

Patentansprüche

1. Flüssigkristallanzeigevorrichtung, umfassend:

eine Flüssigkristalltafel (201; 801), die mit zwei zwischen sich eine Flüssigkristallschicht einschließenden Substraten (202, 203) versehen ist,

eine Abtastelektrodengruppe (Y1-Y6) auf einem der Substrate,

eine Signalelektrodengruppe (X1-X6) auf dem anderen der Substrate, wobei an jedem Kreuzungspunkt zwischen einer Abtastelektrode und einer Signalelektrode ein Pixel gebildet wird, und

eine Einrichtung (205, 213; 905, 213) zum Anlegen einer Abtastspannungswelle an wenigstens ein Ende der Abtastelektrodengruppe und zum Anlegen einer Signalspannungswelle an wenigstens ein Ende der Signalelektrodengruppe zwecks Anzeige eines Anzeigemusters und zur Überlagerung einer Korrekturspannung zu der Abtastspannungswelle und/oder der Signalspannungswelle nach Maßgabe des Anzeigemusters,

gekennzeichnet durch

eine Einrichtung (104; 804) zum Verändern des Werts und/oder der Zeit des Anlegens der Korrekturspannung nach Maßgabe der Pixelpositionen von dem wenigstens einen Ende der Abtastelektrodengruppe und/oder nach Maßgabe der Pixelpositionen von dem wenigstens einen Ende der Signalelektrodengruppe.

2. Flüssigkristallanzeigevorrichtung nach Anspruch 1, bei der der Wert und/oder die Anlegezeit der Korrekturspannung selektiv für jede Elektrode der Abtastelektrodengruppe und/oder für jede Elektrode der Signalelektrodengruppe variiert wird.

3. Flüssigkristallanzeigevorrichtung nach Anspruch 2, bei der eine Wählspannung nacheinander periodisch

an jede Elektrode der Abtastelektrodengruppe (Y1-Y6) angelegt wird, während eine Nicht-Wählspannung an die anderen Elektroden der Abtastelektrodengruppe angelegt wird, und bei der die Korrekturspannung der Nicht-Wählspannung überlagert wird, wobei die Spannungszeitfläche der Korrekturspannung separat für jede Abtastelektrode (Y1-Y6) abhängig von dem Anzeigemuster und der Entfernung zwischen der jeweiligen Abtastelektrode und dem wenigstens einen Ansteuerende der Signalelektrodengruppe (X1-X6) gesteuert wird.

4. Flüssigkristallanzeigevorrichtung nach Anspruch 2 oder 3, bei der eine Wählspannung nacheinander und periodisch an jede Abtastelektrode (Y1-Y6) angelegt wird, wobei die Korrekturspannung der Wählspannung überlagert wird und die Spannungszeitfläche der Korrekturspannung einzeln für jede Abtastelektrode abhängig vom Leucht- oder Nichtleuchtzustand der Pixel auf einer jeweiligen Abtastelektrode und dem Abstand zwischen jedem der Pixel und dem wenigstens einen Ansteuerende der Abtastelektrodengruppe gesteuert wird.

Revendications

1. Un dispositif de visualisation à cristal liquide, comprenant :
un panneau à cristal liquide (201; 801) comportant une paire de substrats (202, 203) entre lesquels est intercalée une couche de cristal liquide,
un groupe d'électrodes de balayage (Y1-Y6) sur l'un des substrats,
un groupe d'électrodes de signal (X1-X6) sur l'autre substrat, un pixel étant formé à chaque point d'intersection entre une électrode de balayage et une électrode de signal, et
des moyens (205, 213; 905, 213) pour appliquer une onde de tension de balayage à au moins une extrémité du groupe d'électrodes de balayage, et pour appliquer une onde de tension de signal à au moins une extrémité du groupe d'électrodes de signal, pour visualiser une confiration de visualisation, et pour superposer une tension de correction sur l'onde de tension de balayage et/ou l'onde de tension de signal, conformément à la configuration de visualisation,
caractérisé par
des moyens (104; 804) pour faire varier la valeur et/ou la durée d'application de la tension de correction, conformément aux positions de pixels à partir de ladite au moins une extrémité du groupe d'électrodes de balayage, et/ou conformément à la position des pixels à partir de ladite au moins une extrémité du groupe d'électrodes de signal.

2. Le dispositif de visualisation à cristal liquide selon la revendication 1, dans lequel on fait varier sélectivement la valeur et/ou la durée d'application de la tension de correction pour chaque électrode du groupe d'électrodes de balayage, et/ou pour chaque électrode du groupe d'électrodes de signal.

3. Le dispositif de visualisation à cristal liquide selon la revendication 2, dans lequel une tension sélective est appliquée successivement et périodiquement à chaque électrode du groupe d'électrodes de balayage (Y1-Y6), une tension non sélective étant appliquée aux autres électrodes du groupe d'électrodes de balayage, et dans lequel la tension de correction est superposée sur la tension non sélective, l'aire correspondant au produit de la tension par le temps pour la tension de correction, étant commandée séparément pour chaque électrode de balayage (Y1-Y6), sous la dépendance de la configuration de visualisation et de la distance entre l'électrode de balayage respective et ladite au moins une extrémité d'attaque précitées du groupe d'électrodes de signal (X1-X6).

4. Le dispositif de visualisation à cristal liquide selon la revendication 2 ou 3, dans lequel une tension sélective est appliquée successivement et périodiquement à chaque électrode de balayage (Y1-Y6), la tension de correction étant superposée sur la tension sélective, et l'aire correspondant au produit de la tension par le temps pour la tension de correction, étant commandée individuellement pour chaque électrode de balayage sous la dépendance de l'état éclairé ou non éclairé des pixels sur une électrode de balayage respective, et de la distance entre chacun des pixels et ladite au moins une extrémité d'attaque du groupe d'électrodes de balayage.

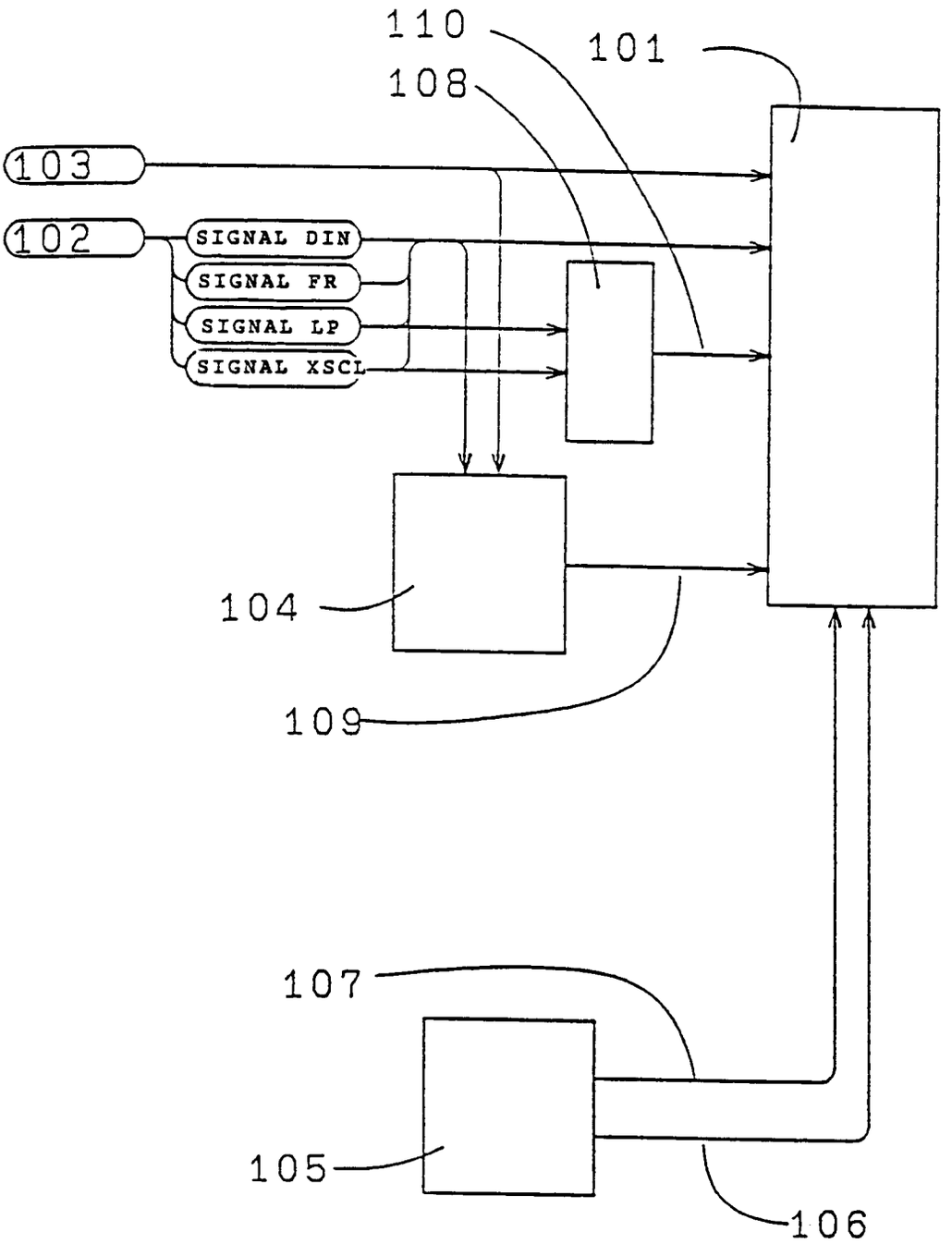

110
101
108
103
102
SIGNAL DIN
SIGNAL FR
SIGNAL LP
SIGNAL XSCL
104
109
107
105
106

Fig. 1

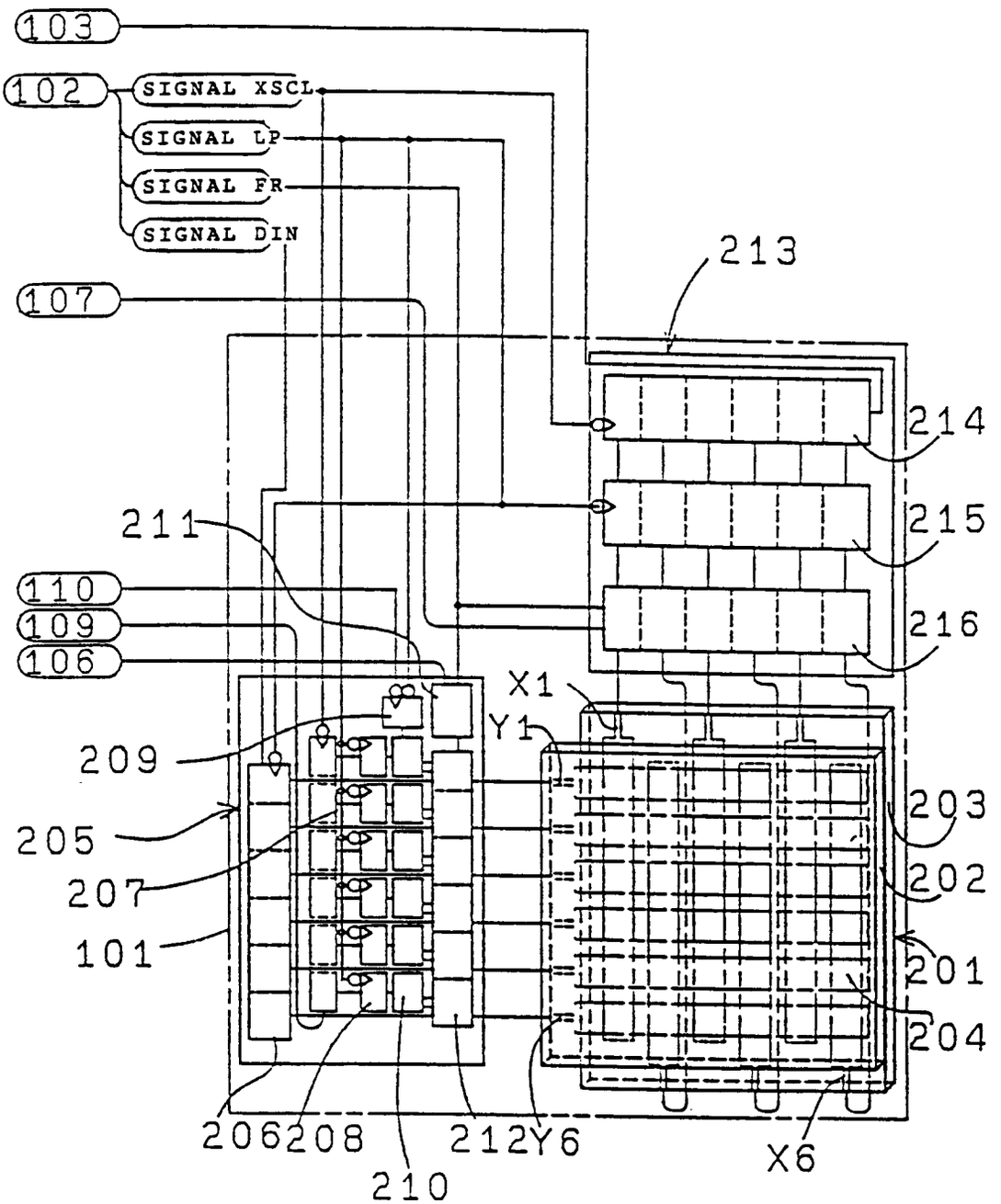

103
102
SIGNAL XSCL
SIGNAL LP
SIGNAL FR
SIGNAL DIN
107
213
214
215
216
211
110
109
106
X1
Y1
209
205
207
101
203
202
201
204
206
208
210
212
Y6
X6

Fig. 2

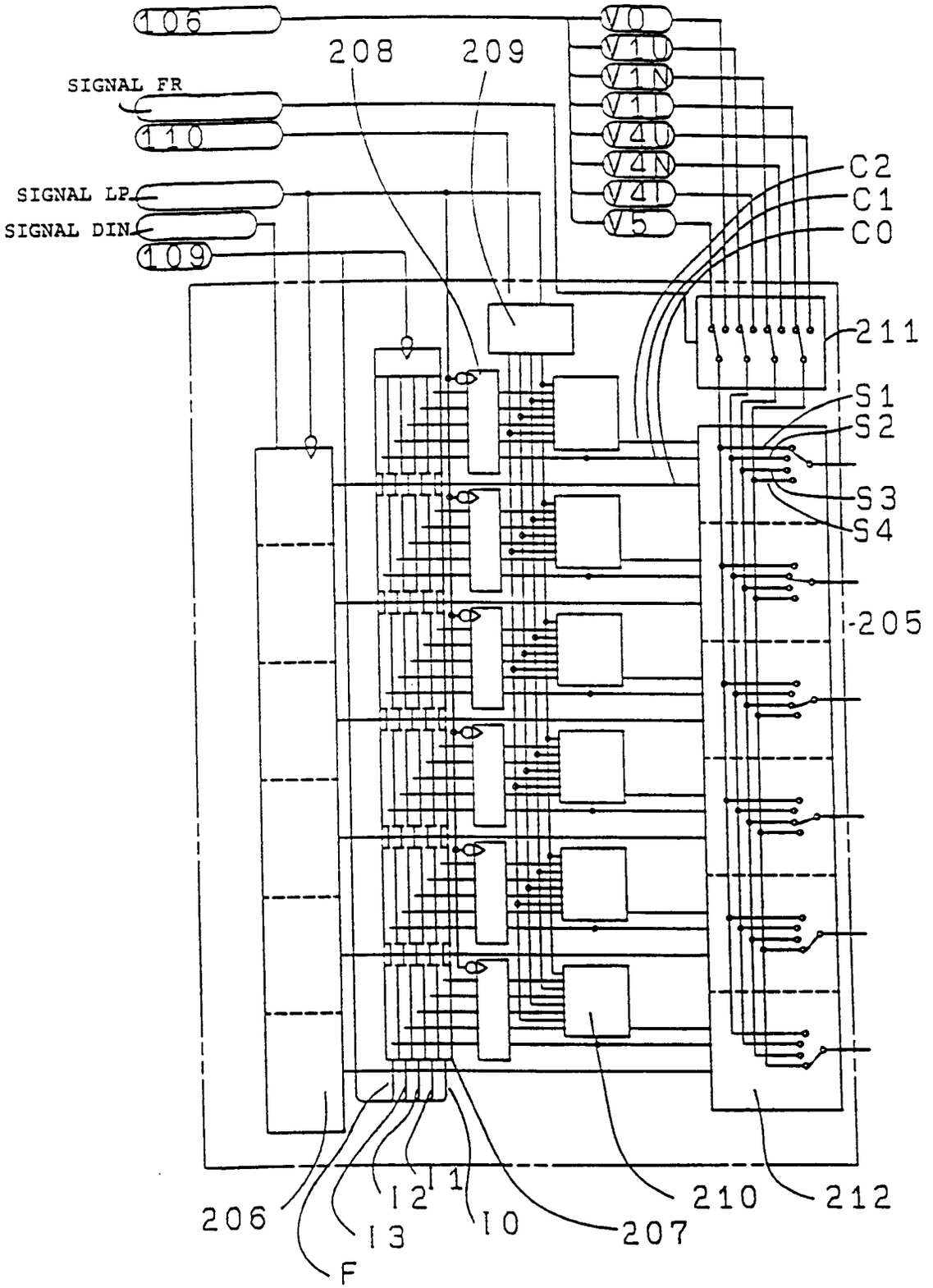

106
SIGNAL FR
110
SIGNAL LP
SIGNAL DIN
109
208
209
V0
V10
V1N
V1
V40
V4N
V41
V5
C2
C1
C0
211
S1
S2
S3
S4
205
206
F
13
12
11
10
207
210
212

Fig. 3

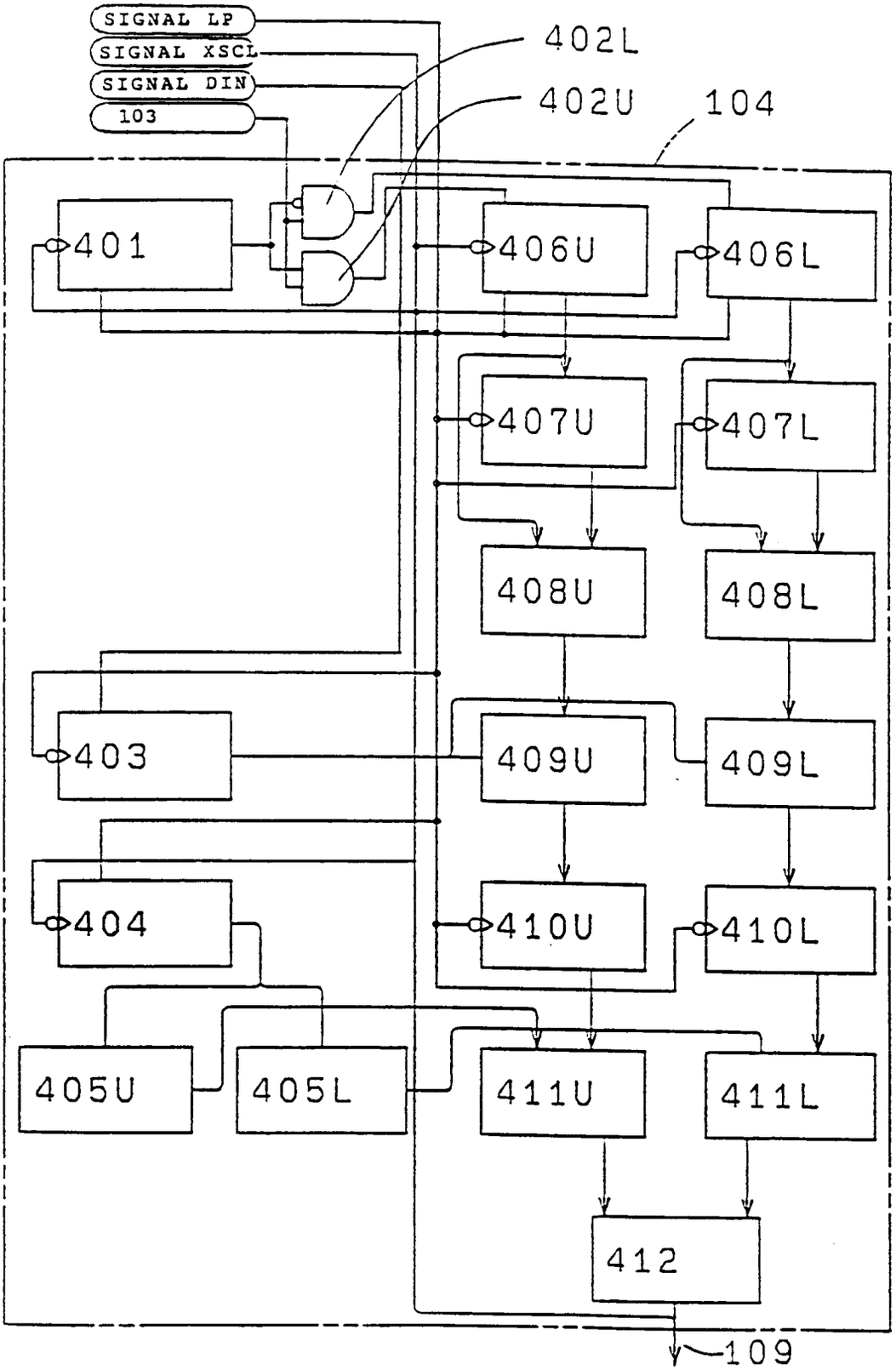

SIGNAL LP
SIGNAL XSCL
SIGNAL DIN
103
402L
402U
104
401
406U
406L
407U
407L
408U
408L
403
409U
409L
404
410U
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405L
411U
411L
412
109

Fig. 4

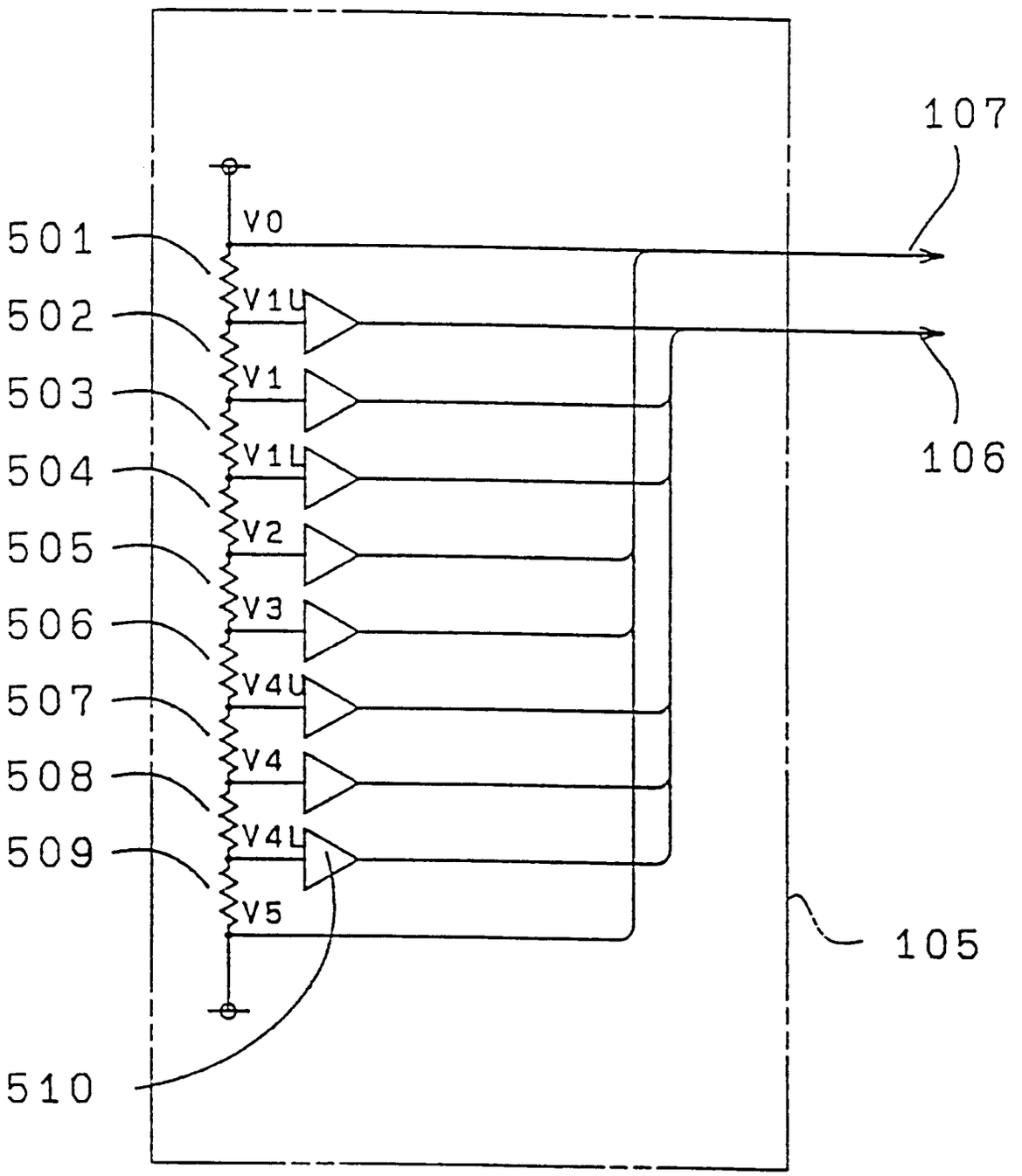

107
V0
501
V1U
502
V1
503
V1L
504
V2
505
V3
506
V4U
507
V4
508
V4L
509
V5
106
105
510

Fig. 5

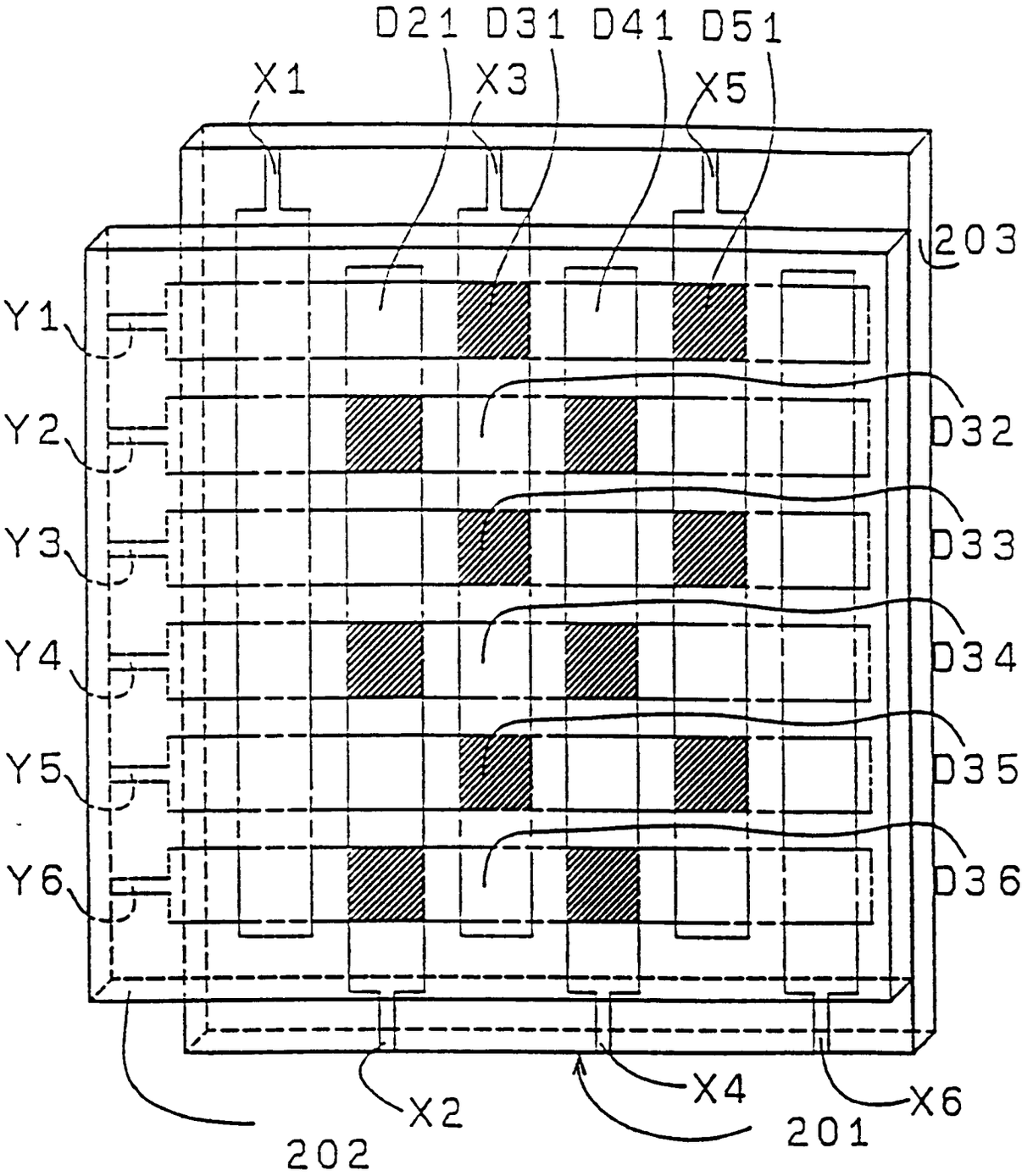

D21 D31 D41 D51
X1
X3
X5
203
Y1
Y2
Y3
Y4
Y5
Y6
D32
D33
D34
D35
D36
X2
X4
X6
202
201

Fig. 6

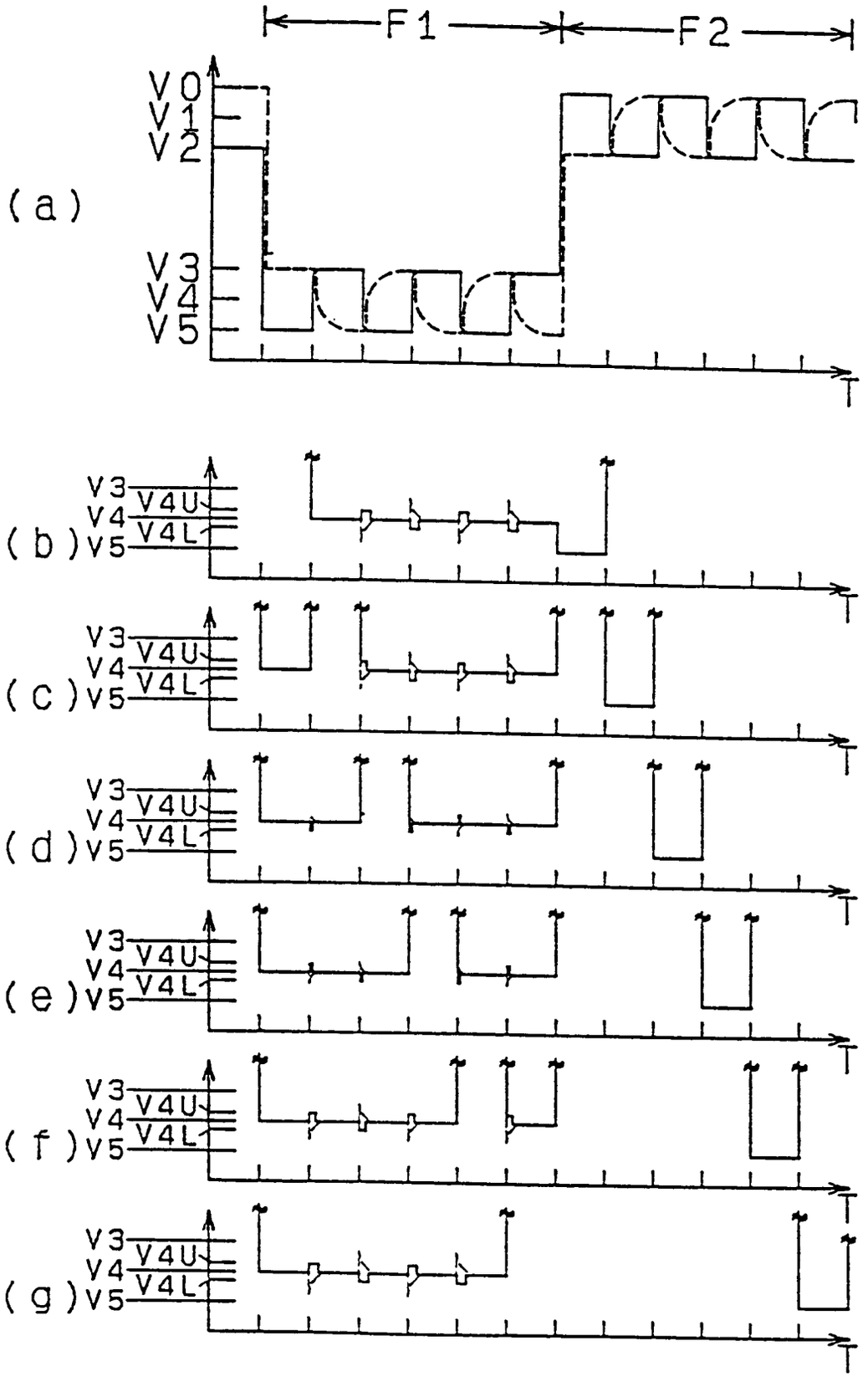


Fig. 7

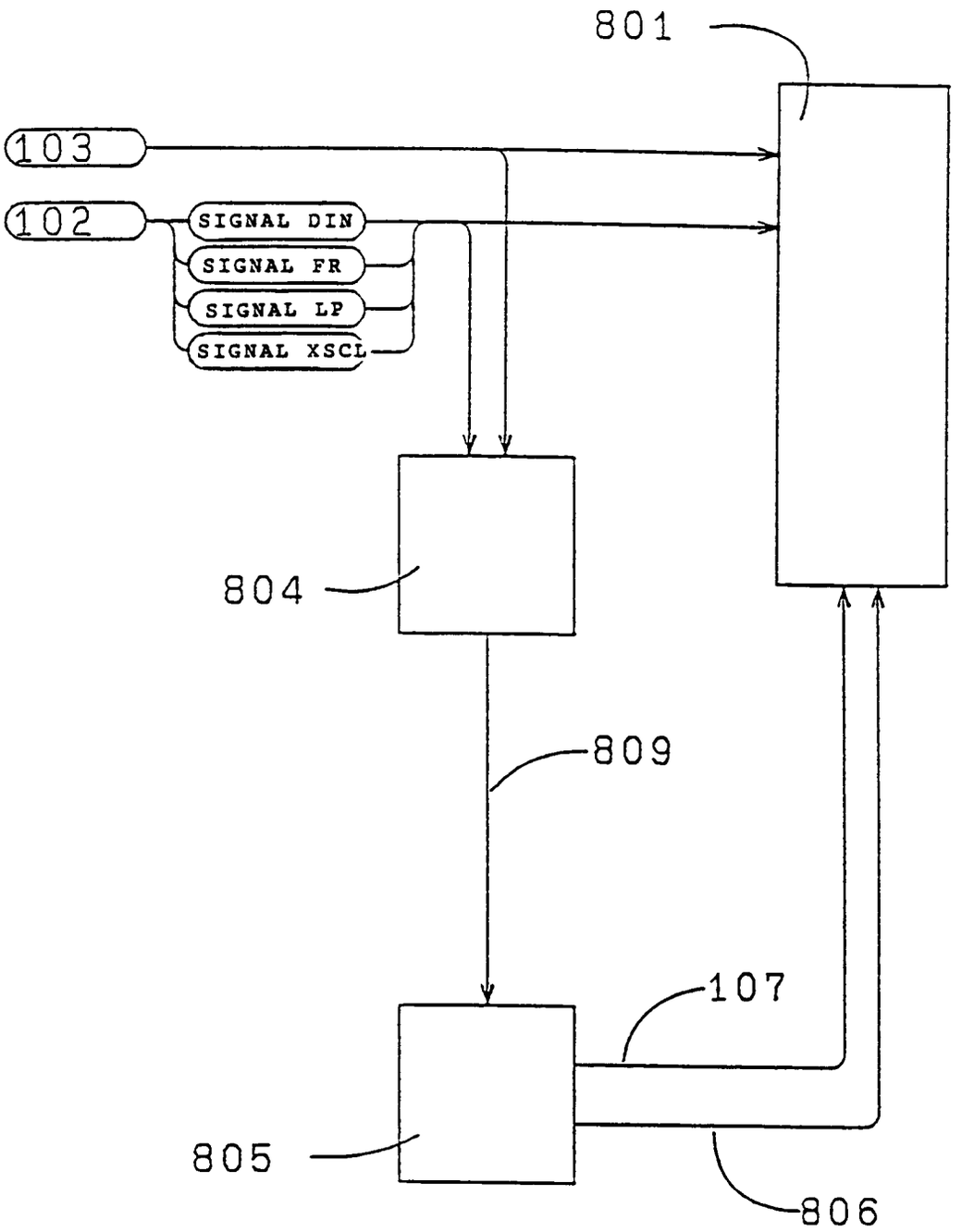

801
103
102
SIGNAL DIN
SIGNAL FR
SIGNAL LP
SIGNAL XSCL
804
809
107
805
806

Fig. 8

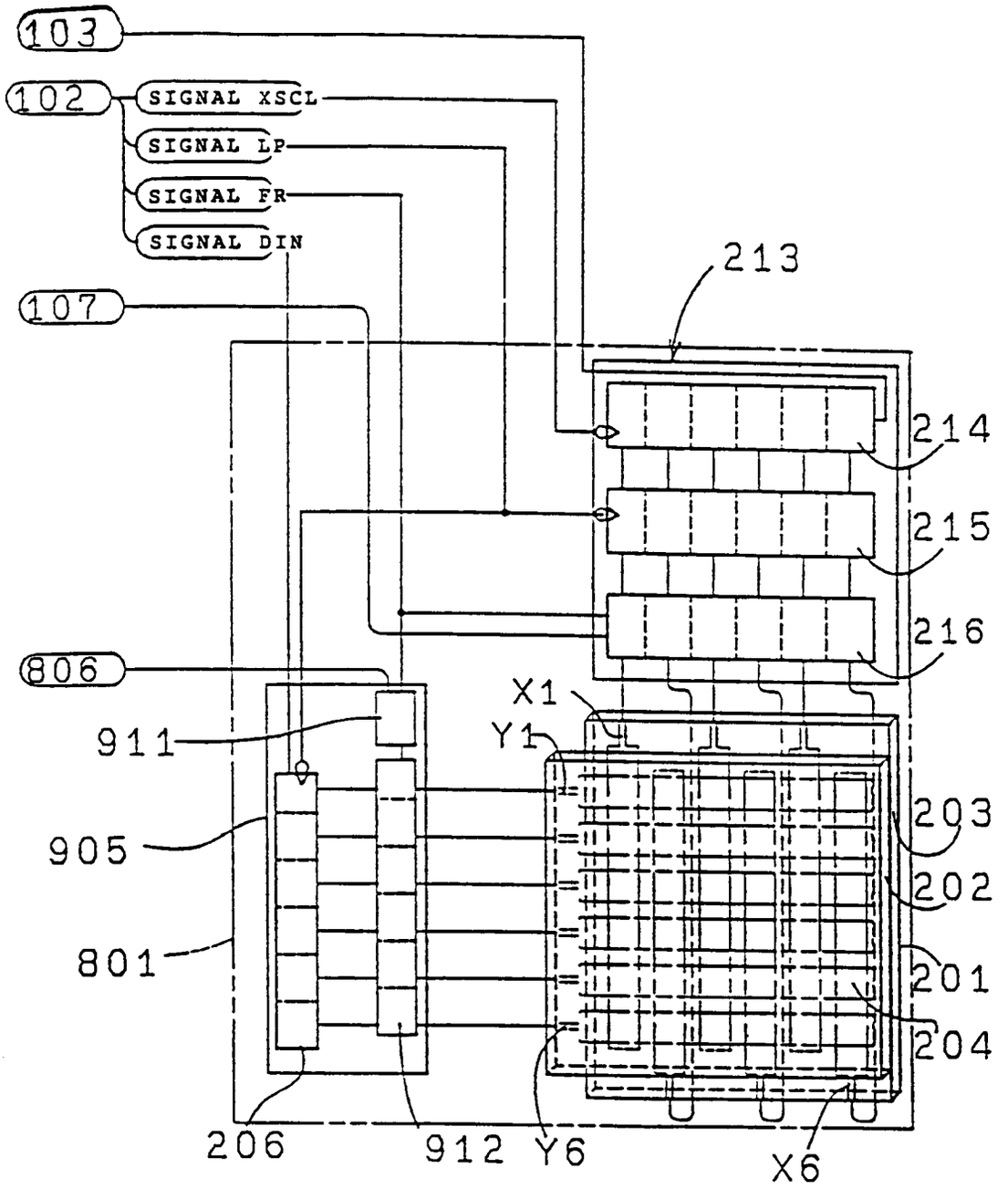

103
102
SIGNAL XSCL
SIGNAL LP
SIGNAL FR
SIGNAL DIN
107
213
214
215
216
806
911
905
801
X1
Y1
203
202
201
204
206
912
Y6
X6

Fig. 9

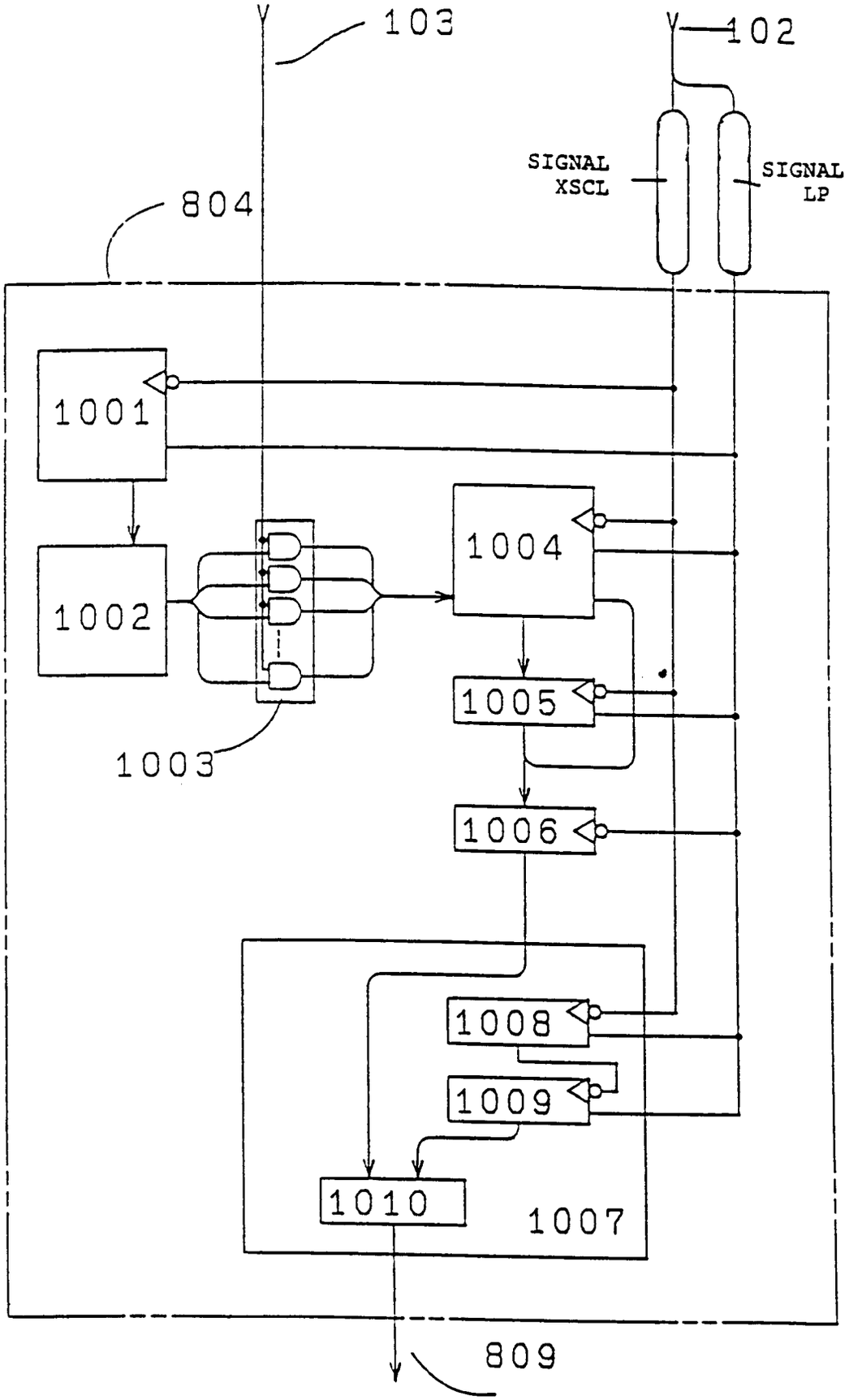

103
102
SIGNAL XSCL
SIGNAL LP
804
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
809

Fig. 10

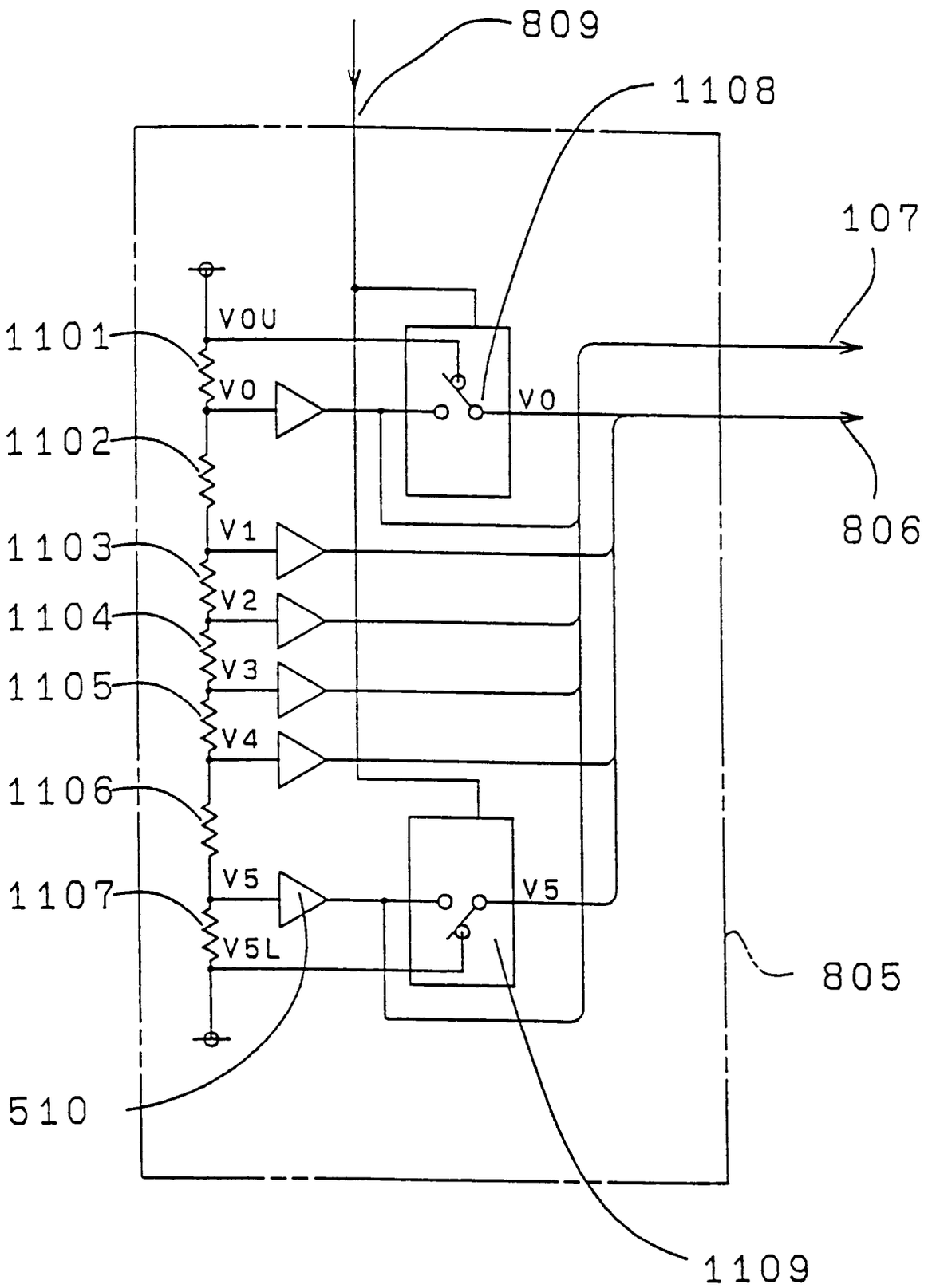

809
1108
107
VOU
1101
V0
V0
1102
806
V1
1103
V2
1104
V3
1105
V4
1106
V5
V5
1107
V5L
805
510
1109

Fig. 11

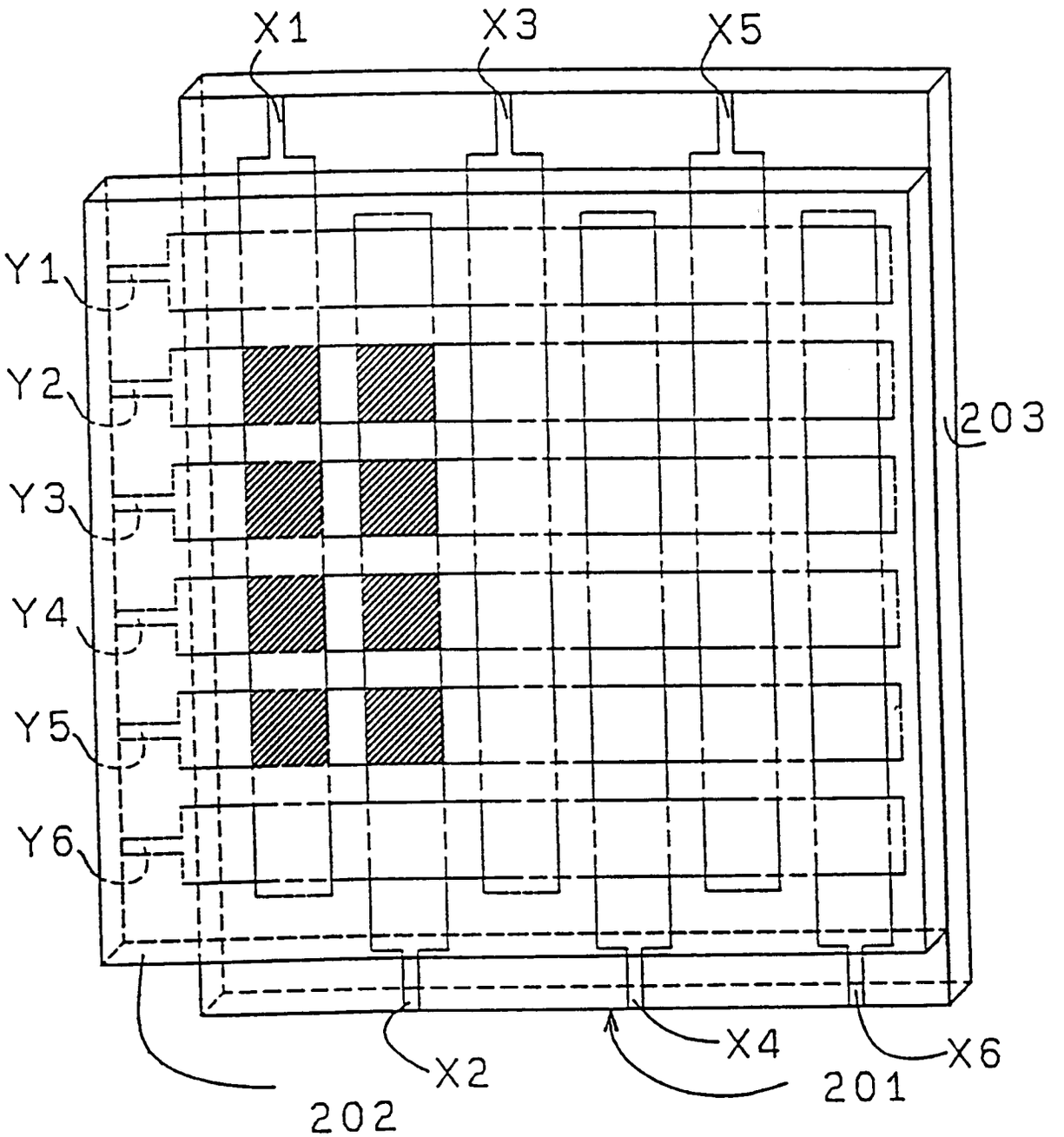


Fig. 12

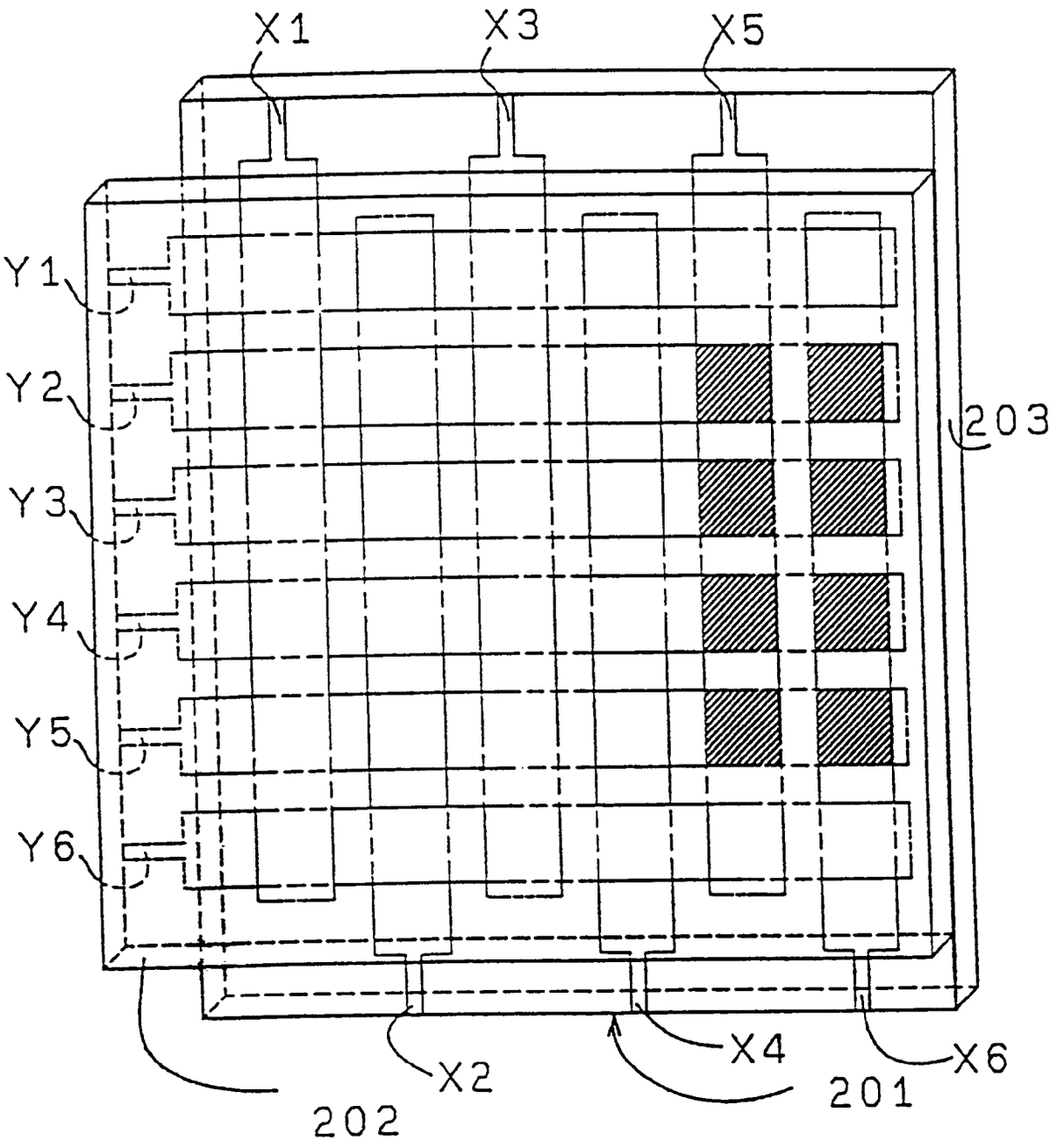


Fig. 13

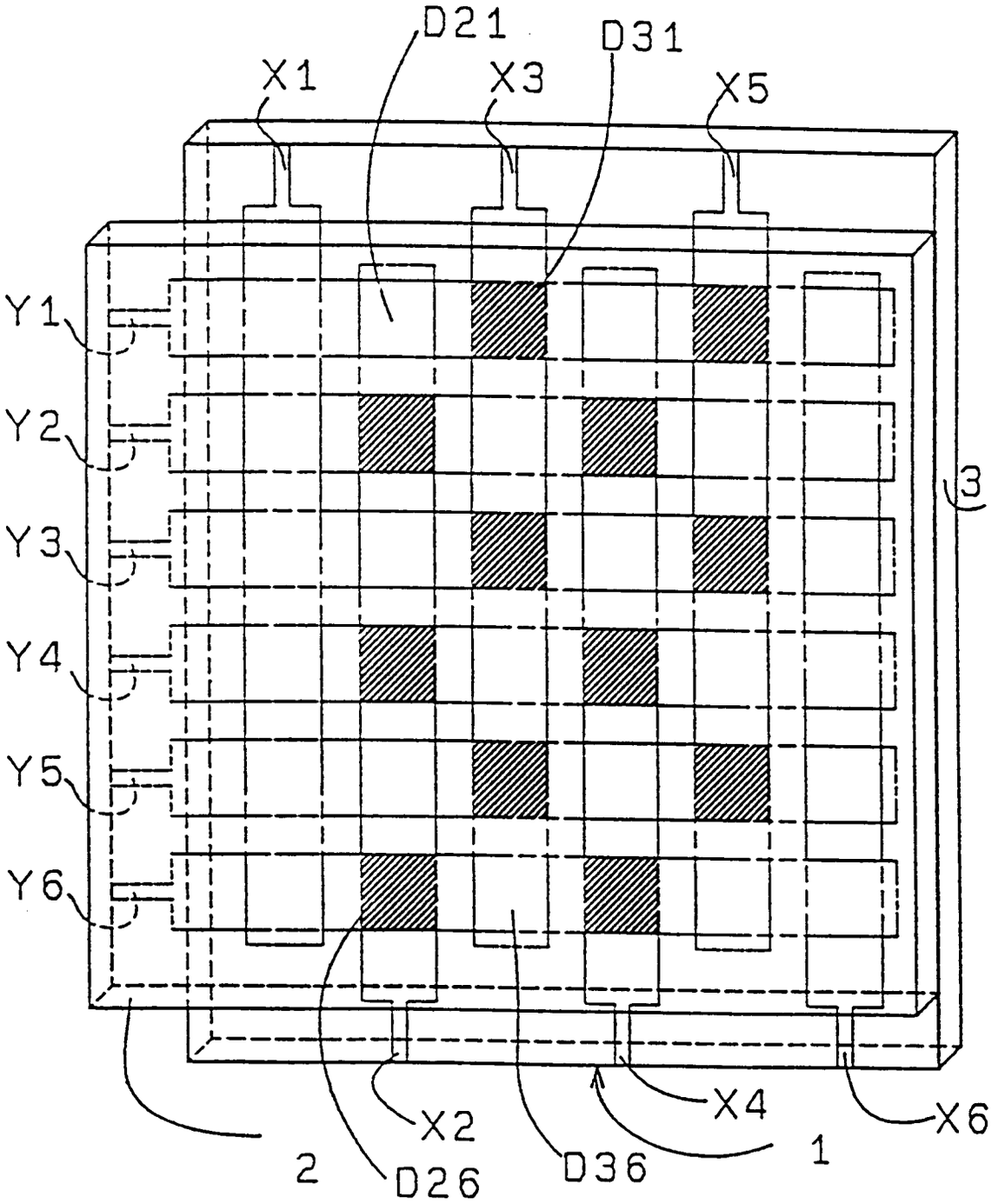


Fig. 14

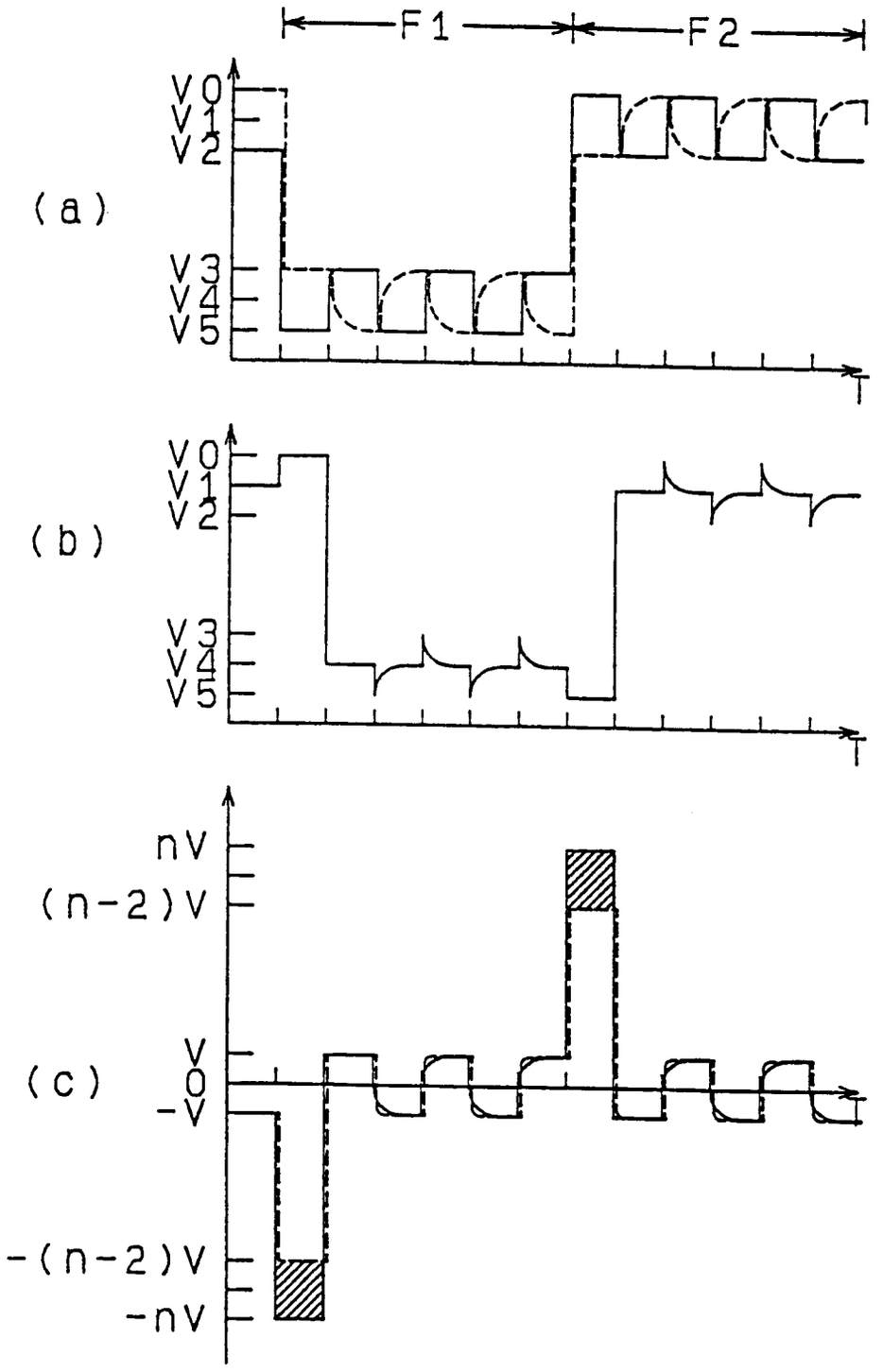


Fig. 15

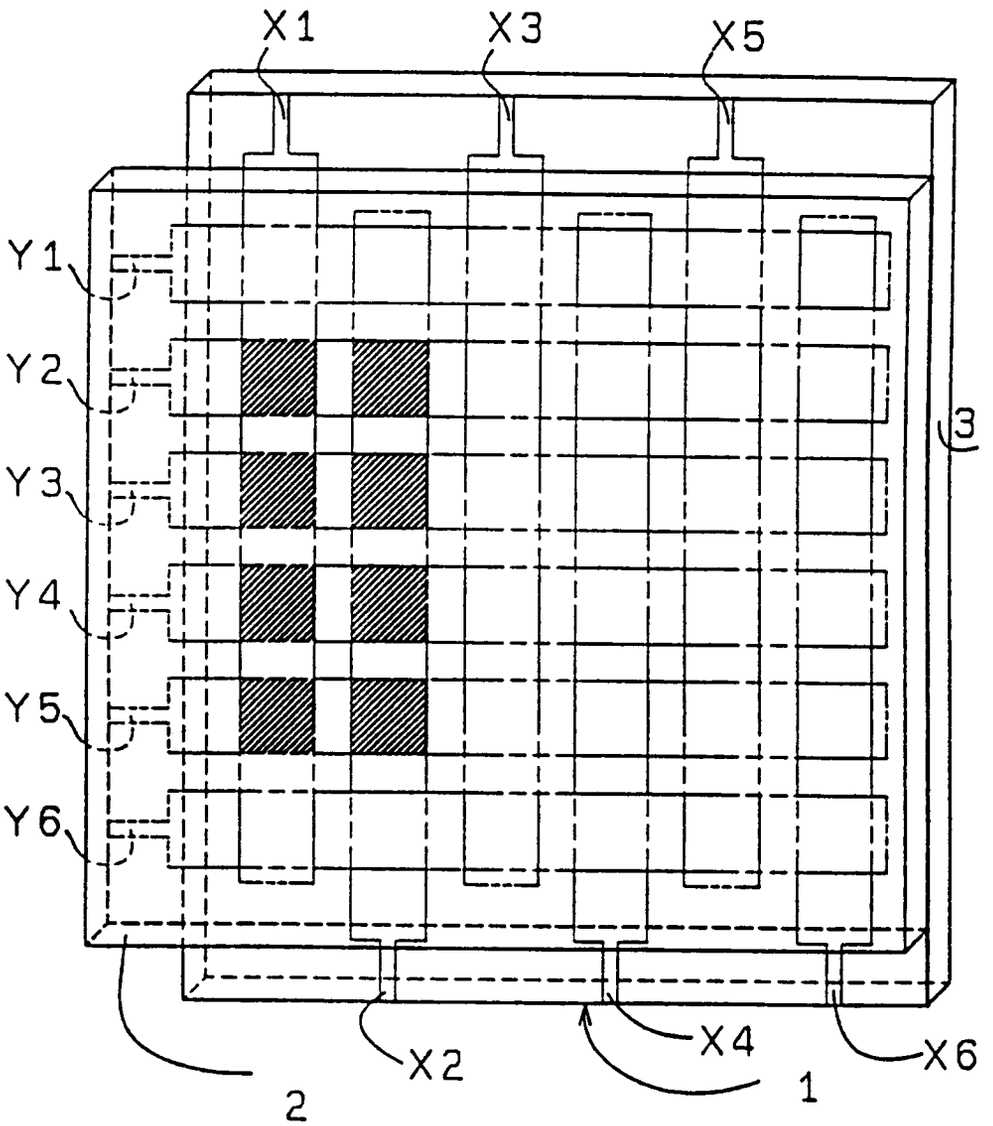


Fig. 16

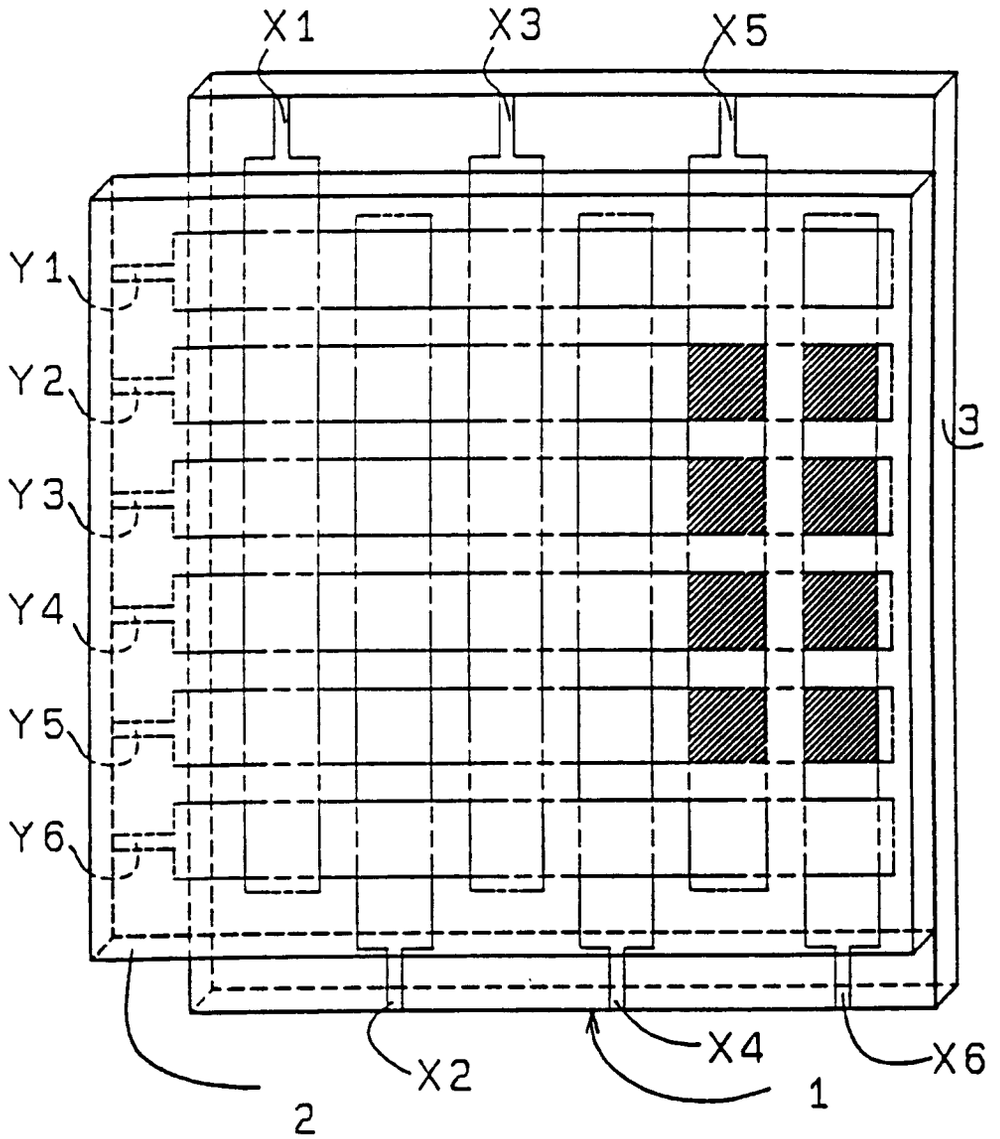


Fig. 17