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(54) **Semiconductor device including a lateral bipolar transistor and corresponding manufacturing methods**

Halbleitervorrichtung mit einem lateralen Bipolartransistor und entsprechende Herstellungsverfahren

Dispositif semi-conducteur comprenant un transistor bipolaire latéral et méthodes de fabrication correspondantes

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device including a lateral bipolar junction transistor and a method of fabricating the same.

Description of the Prior Art

A known very-high-speed bipolar junction transistor has a base contact electrode and an emitter contact electrode formed of a polycrystalline silicon film, and a base region and an emitter region formed by the diffusion of the impurity from the polycrystalline silicon film forming the emitter contact electrode in a self-alignment mode. Figs. 14A, 14B, 14C and 14D show the very-high-speed bipolar junction transistor in different steps of the fabricating process. As shown in Fig. 14A, an n-type epitaxial layer 4 is formed after forming an embedded collector region 2 of a second conductivity type, for example, n-type, and a p-type channel stop region 3 in one of the major surfaces of a silicon substrate 1 of a first conductivity type, for example, p-type, a heavily doped n-type collector contact region 5 is formed so as to reach the embedded collector region 2, and then a field insulating film 6 is formed by local oxidation over the entire surface excluding the collector electrode region, and a region 4A in which a base region and an emitter region are to be formed afterward. Subsequently, a thin insulating film 7, such as a thin SiO_2 film, is formed over the entire surface, a portion of the thin insulating film 7 corresponding to the region 4A is removed, a first polycrystalline silicon film 8, which serves as a base contact electrode, is formed by a CVD process (chemical vapor deposition process), and then the polycrystalline silicon film 8 is doped with a p-type impurity, i.e., boron. Then, the p^+-type polycrystalline silicon film 8 is patterned by using a first resist mask 9 having the pattern of the-base contact electrode.

Then, as shown in Fig. 14B, a SiO_2 film 10 is formed over the entire surface including the patterned p^+-type polycrystalline silicon film 8 by a CVD process, and then a second resist mask 11 is formed. Portions of the SiO_2 film 10 and the p^+-type polycrystalline silicon film 8 corresponding to an active region, in which an intrinsic base region and an emitter region are to be formed, are removed by selective etching using the resist mask 11 to form a window 13 and a base contact electrode 12 formed of the p^+-type polycrystalline silicon film 8.

Then, as shown in Fig. 14C, the region 4A is doped through the window 13 with a p-type impurity, i.e., boron, by ion implantation to form a link base region 14 for connecting an external base region and an intrinsic base region to be formed on the region 4A afterward. Then, a SiO_2 film is formed by a CVD process, and then the SiO_2 film formed by the CVD process is densified through a heat treatment in which the SiO_2 film is heated at a temperature on the order of 900°C. During the heat treatment of the SiO_2 film, boron contained in the base contact electrode 12 formed of the p^+-type polycrystalline silicon film is caused to diffuse into the region 4A to form part of an external base region 16. Then, a SiO_2 side wall 15 is formed over the inner surface of the base electrode 12 facing the window 13.

Then, as shown in Fig. 14D, a second polycrystalline silicon film 18 for an emitter contact electrode is deposited by a CVD process in a window 17 defined by the side wall 15. Then, the polycrystalline silicon film 18 is doped by ion implantation with a p-type impurity, such as B or BF_2, and annealed to form a p-type intrinsic base region 19 in the active region, and then, the p-type base region 19 is doped by ion implantation with an n-type impurity, such as As, and annealed to form an n-type emitter region 20. In another method, the polycrystalline silicon film 18 is doped by ion implantation with p-type and n-type impurities and annealed to form the p-type intrinsic base region 19 and the n-type emitter region 20. During the annealing process for forming the base region 19 and the emitter region 20, boron contained in the base contact electrode 12 formed of p^+ -type polycrystalline silicon is caused to diffuse to complete the external base region 16.The impurity concentration of the intrinsic base region 19 is higher than that of the link base region 14. Then, contact holes are formed, and then a base electrode 21, a collector electrode 22 and an emitter electrode 23 of a metal, such as aluminum, are formed to complete a very-high-speed bipolar transistor 24.

Fig. 10 shows the structure of a lateral pnp bipolar junction transistor 40. The lateral pnp bipolar junction transistor 40 is constructed by forming an n-type epitaxial layer 4 over an n-type embedded base region 26 formed on a p-type silicon substrate 1, forming a field insulating film 6 by selective oxidation, forming an n-type plug-in region 27 reaching the n-type embedded base region 26, and an n-type contact base region 28, forming a p-type collector region 32 and a p-type emitter region 33 respectively having heavily doped p-type regions 30 and 21, and forming an aluminum collector electrode 34, an aluminum base-electrode 35 and an aluminum emitter electrode 36. In Fig. 10, indicated at 37 is a p-type isolating region, at 38 is a layer insulating film and at 39 is a thin SiO_2 film. In most cases, the p-type collector region 32 and the p-type emitter region are formed at the same time with the p-type intrinsic base region 19 of the npn bipolar junction transistor 24 shown in Fig. 14D, and the heavily doped p-type regions 30 and 31 are formed at the same time with the external base region 16 of the npn bipolar junction transistor 24. The base width W_B is determined by the p-type collector region 32 and the p-type emitter region 33. Fig. 11 shows the impurity concentration profile of a section along an alternate long and short dash line 41. The impurity con-

centration profile has a peak at a position corresponding to a portion near the surface of the substrate as shown in Fig. 11, because the surface is doped by ion implantation with boron and boron is caused to diffuse in forming the p-type collector region 32 and the p-type emitter region 33. Accordingly, the collector region 32 and the emitter region are nearest in the vicinity of the surface.

Fig. 12 shows the structure of another lateral pnp bipolar junction transistor 42, in which portions corresponding to those of the lateral pnp bipolar junction transistor shown in Fig. 10 are denoted by the same reference characters and the description thereof will be omitted to avoid duplication. In fabricating the lateral pnp bipolar junction transistor 42, a contact base region 28 is formed simultaneously with the contact collector region 5 of the npn bipolar junction transistor 24 shown in Fig. 14D, and a p-type emitter region 33 and a p-type collector region 32 are formed simultaneously with the external base region 16 of the npn bipolar junction transistor 24 through the diffusion of boron from a contact electrodes 44 and 43 formed of p^+-type polycrystalline silicon. Indicated at 3 is a p-type channel stop region.

The current amplification factor h_{FE} of the lateral pnp trans istor 40 shown in Fig. 10 is reduced due to surface recombination because the current flows mainly along the surface, i.e., the vicinity of the interface of the SiO_2 film 39, and the current amplification factor h_{FE} is liable to be unstable due to the variation of the surface recombination electrode depending on the condition of the interface of the SiO_2 film 39.

As shown in Fig. 13, the base width W_B of the lateral pnp transistor 42 shown in Fig. 12 is not dependent on the minimum line width achieved by lithography, but is dependent on several factors as expressed by:

$$W_B = a + 2b - 2c$$

where a is the minimum line width achieved by lithography, b is the width of overlaps in which the SiO_2 film 19 and the p^+-type polycrystalline silicon films 43 and 44-overlap each other, and c is the width of areas of side diffusion of the p^+-type diffused regions of the emitter 32 and the collector 33.

For example, when the minimum line width a = 1.2 μm, a stepping projection aligner of ± 0.3 μm aligning-accuracy is employed, and the the junction depth X_j of the p^+-type diffused regions 32 and 33 is 0.2 μm,

$$W_B =$$

$$1.2\ \mu m + 2 \times 0.8\ \mu m - 2 \times 0.8 \times 0.2\ \mu m \simeq 2.48\ \mu m$$

The base width W_B is approximately twice as large as the minimum line width a, and hence it is impossible to provide the lateral pnp transistor 42 with a high f_T.

Patent Abstracts of Japan, vol.5, no.125 (E-69) (797), August 12, 1981 & JP-A-56-62361 discloses a lateral pnp transistor in which the current flows mainly along the surface of the device.

SUMMARY OF THE INVENTION

The present invention is intended to prevent surface recombination in a semiconductor device including a lateral bipolar junction transistor having a collector region, a base region and an emitter region formed in a lateral arrangement on a semiconductor substrate and to improve and stabilize the current amplification factor of the lateral bipolar junction transistor by forming the respective portions having peak impurity concentrations of the collector region and the emitter region within the base region.

A semiconductor device in accordance with the present invention is set out in claim 1.

A method of fabricating a semiconductor device in accordance with the present invention is furthermore set out in any one of claims 3 and 4. The present invention reduces the base width W_B to provide a high f_T and a high h_{FE}.

Accordingly, it is an object of the present invention to provide a method of fabricating a lateral bipolar junction transistor, capable of reducing the base width W_B to the minimum line width to provide the lateral bipolar junction transistor with a high f_T and a high h_{FE}.

A semiconductor device in accordance with the present invention comprises a semiconductor substrate 1 provided with a collector region 62, a base region 60 and an emitter region 61 in a lateral arrangement, wherein respective portions having peak impurity concentrations of the collector region and the emitter region are formed within the base region 60 and not near the surface.

A method of fabricating a semiconductor device in accordance with the present invention comprises a step of forming a collector region 132 of a second conductivity type and an emitter region 133 of the second conductivity type in a lateral arrangement in a semiconductor substrate 1 of a first conductivity type by using a first mask 123 provided with a pair of openings 121 and 122; and a step of forming heavily doped regions 130 and 131 of the second conductivity type so as to be connected respectively to the collector region 132 and the emitter region 133 by using a second mask 127 provided with a pair of openings separated from each other by a distance d_2 greater than the distance d_1 between the openings of the first mask 123.

In the semiconductor device in the first aspect of the present invention, the collector region 62 and emitter region 61 of the lateral transistor are formed so that portions thereof having the maximum impurity concentration are formed within the base region 60 to form a main current path within the base region 60 instead of near the surface of the same, which prevents the reduction of h_{FE} due to surface recombination. The small variation

of the surface recombination current due to the condition of the surface of the oxide film stabilizes the h_{FE}. Thus, the lateral transistor has a stable, high h_{FE}.

In the method of fabricating a lateral transistor in the second aspect of the present invention, the collector region 132 and the emitter region 133 are formed by using the first mask 123, and the heavily doped regions 130 and 131 of the collector region and the emitter region are formed by using a second mask 127. Accordingly, the pair of openings 121 and 122 of the first mask 123 can be separated from each other by the distance d_1 corresponding to the minimum line width which can be achieved by lithography. Accordingly, the collector region 132 and the emitter region 133 can be formed so that the base width W_E corresponds to the minimum line width to achieve a high f_T. Since the collector electrodes 43 and 134 and the emitter electrodes 44 and 136 are formed by using the second mask provided with the openings 125 and 126, the collector electrodes 43 and 134 and the emitter electrodes 44 and 136 can easily be isolated from each other.

Since the emitter region 133 has a heavily doped region 131, the emitter injection efficiency is high and the h_{FE} is improved.

Thus, a lateral transistor having a high f_T and a high h_{FE} can be fabricated.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following description taken in connection with the accompanying drawings, in which:

Figure 1 is a sectional view of a lateral bipolar transistor in a preferred embodiment according to the present invention;

Figures 2 and 3 are graphs showing impurity concentration profiles respectively along the lines A_1-A_1 and B_1-B_1 in Fig. 1;

Figures 4A to 4D are sectional views of assistance in explaining steps of a method of fabricating the lateral bipolar transistor of Fig. 1 and a low emitter concentration (LEC) transistor ;

Figure 5 is a sectional view of a semiconductor device comprising a lateral bipolar transistor and a LEC transistor according to the present invention;

Figures 6 and 7 are graphs showing impurity concentration profiles respectively along the lines A_2-A_2 and B_2-B_2 in Fig. 5;

Figure 8 is a sectional view of a lateral bipolar transistor in a further embodiment according to the present invention;

Figures 9A to 9C are sectional views of assistance in explaining steps of a method of fabricating the lateral bipolar transistor of Fig. 8;

Figure 10 is a sectional view of a conventional lateral bipolar transistor;

Figure 11 is a graph showing an impurity concentration profile in the lateral bipolar transistor of Fig. 16;

Figure 12 is a sectional view of another conventional lateral bipolar transistor;

Figure 13 is an enlarged sectional view of an essential portion of the lateral bipolar transistor of Fig. 18; and

Figures 14A to 14D are sectional views of assistance in explaining steps of a conventional method of fabricating a very-high-speed bipolar transistor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a lateral pnp transistor in a first embodiment according to the present invention.

According to the present invention, an embedded n-type base region 26 and an n-type epitaxial layer 4 are formed on a p-type silicon substrate 1, a p-type isolation region 37, and a selectively oxidized (LOCOS) field insulating layer 6 are formed and n-type plug-in region 27 reaching the embedded n-type base region 26, and an n-type base contact region 28 are formed.

A p-type emitter region 61 and a p-type collector region 62 are formed in a lateral arrangement so that portions thereof respectively having maximum impurity concentrations are within the n-type epitaxial layer 4, which serves as a base region 60, with a distance corresponding to a base width W_B therebetween, and then heavily doped p-type regions 63 and 64 are formed so as to be joined respectively to the emitter region 61 and the collector region 62. Subsequently, a layer insulating film 38 is formed, and then a collector electrode 34, a base electrode 35 and an emitter electrode 36, such as aluminum electrodes, are formed in contact holes to complete a lateral pnp bipolar transistor 65.

Fig. 2 shows the variation of impurity concentration with depth along the line A_1-A_1 in Fig. 1, and Fig. 3 shows the variation of impurity concentration with depth along the line B_1-B_1 in Fig. 1.

Figs. 4A, 4B, 4C and 4D are sectional views showing the lateral pnp bipolar transistor 65 in different steps of a fabricating process. In this case, the lateral pnp bipolar transistor 65 is fabricated together with a low emitter concentration transistor (LEC) featured by its high V_{EBO}, low C_{BE} and low noise.

As shown in Fig. 4A, an embedded n-type base region 26 and an embedded n-type collector region 68 are formed respectively in a lateral pnp transistor forming section 66 and a LEC transistor forming section 67 of a p-type silicon substrate 1, an n-type epitaxial layer 4 is formed, and then p-type isolation regions 37 and a field insulating layer 6 are formed. When necessary, an n-type plug-in region 27 reaching the embedded n-type base region 26, and an n-type plug-in region 69 reaching the embedded n-type collector region 68 are formed respectively in the sections 66 and 67. Indicated at 80 is

a thin SiO_2 film.

Then, as shown in Fig. 4B, a p-type emitter region 61 and a p-type collector regions 62 are formed in the section 66 so that portions thereof having maximum impurity concentrations are formed within the epitaxial layer 4, which serves as a base region, and, simultaneously, a p-type base region 83 for the LEC transistor is formed in the section 67 by ion implantation using a p-type impurity 82, such as boron, a resist mask 81 and energy of 180 keV or higher.

Then, as shown in Fig. 4C, heavily doped p-type regions 64 and 63, i.e., a p-type collector contact region and a p-type emitter contact region, are formed in the section 66 and, at the same time, a p-type base contact region 84 for the LEC transistor is formed in the section 67. An n-type emitter region 85 for the LEC transistor is formed in the section 67. An n-type collector contact region 86 for the LEC transistor is formed and an n-type base contact region 28 for the lateral pnp transistor is formed in the section 66 simultaneously with the formation of the n-type emitter region.

Then, as shown in Fig. 4D, contact holes are formed after forming a layer insulating film 38, and then collector electrode 34 and a base electrode 35 and an emitter electrode 36, such as aluminum electrodes, are formed in the section 66 to complete the lateral pnp bipolar transistor 65 and a collector electrode 87, a base electrode 88 and an emitter electrode 89, such as aluminum electrodes, are formed in the section 67 to complete the LEC npn transistor 90.

In the lateral pnp bipolar transistor 65 thus fabricated, portions of the collector region 62 and the emitter region 61 respectively having maximum impurity concentrations are formed within the bulk and portions of the collector region 62 and the emitter region 61 nearest to each other are formed within the bulk to form a principal current passage within the bulk instead of near the surface. Consequently, reduction in current amplification factor h_{FE} due to surface recombination is prevented to provide a lateral bipolar transistor having a high h_{FE}. Instability in the h_{FE} due to the condition of the interface of the oxide film (SiO_2 film) is removed, namely, change in the surface recombination current due to the condition of the interface of the oxide film is reduced to stabilize the h_{FE}.

Fig. 5 shows a lateral pnp bipolar transistor 91 in a second embodiment according to the present invention, in which parts corresponding to those shown in Figs. 4A to 4D are denoted by the same reference characters and the description thereof will be omitted to avoid duplication. The collector region 62 and the emitter region 61 of the lateral pnp bipolar transistor 91 are formed by doping the corresponding regions with a p-type impurity by ion implantation using high energy in the range of 100 to 150 keV, and then the collector region 62 and the emitter region 63 are subjected to a heat treatment to make the impurity diffuse into the surface epitaxial layer 4 so that portions respectively having maximum impurity concentrations of the collector region 62 and the emitter region 63 are formed within the bulk as shown in Fig. 6.

Fig. 6 shows the profile of impurity concentration along the line A_2-A_2 in Fig. 5, and Fig. 7 shows the profile of impurity concentration along the line B_2-B_2 in Fig. 5.

The collector region 62 and the emitter region 61, similarly to those shown in Fig. 1, are formed so that the impurity concentration in the vicinity of the surface is 1/3 the maximum impurity concentration in the bulk or below, namely, $b/a \leqq 1/3$ as shown in Fig. 6. On the other hand, the base region 83, which is formed simultaneously with the collector region 62 and the emitter region 61, of the LEC transistor 90 is formed, similarly to the collector region 62 and the emitter region 61 of the pnp bipolar transistor 91, so that a portion having a maximum impurity concentration is formed within the bulk, and the impurity concentration in the vicinity of the surface is lower than the maximum impurity concentration.

In the lateral pnp bipolar transistor 91, portions having the maximum impurity concentrations of the collector region 62 and the emitter region 61 are formed within the bulk to form a principal current passage within the bulk instead of near the surface. Consequently, reduction in current amplification factor h_{FE} due to surface recombination is prevented, instability in the h_{FE} due to the condition of the interface of the oxide film is removed to provide the lateral pnp bipolar transistor 91 with a stable, high h_{FE}.

Incidentally, a high-speed device requires a high-performance lateral pnp transistor. The performance of the lateral pnp transistor 65 of Fig. 1 can be improved by diminishing the base width W_B. However, the epitaxial concentration, in general, is in the range of 5×10^{14} to $5 \times 10^{16}/cm^3$. When the lateral pnp transistor is incorporated into a LSI provided with a npn bipolar transistor provided with a base electrode and an emitter electrode formed of polycrystalline silicon as shown in Fig. 14, the epitaxial concentration is not higher than $10^{15}/cm^3$ when the epitaxial layer 4 has a high resistance to reduce the collector junction capacity C_{JC} so that the operating speed of the npn bipolar transistor is enhanced. Accordingly, when the base width W_B of the lateral pnp transistor is diminished to a width not greater than 1.0 μm, the total quantity Q_B of the impurity in the base becomes a value on the order of $10^{11}/cm^2$ and punch through occurs between the emitter and the collector. Thus, it is difficult to improve the performance of the lateral pnp transistor by reducing the base width W_B.

Fig. 8 shows a high-performance, stable lateral pnp bipolar transistor 93 embodying the present invention developed by solving the foregoing problems.

In Fig. 8, parts corresponding to those shown in Fig. 1 are denoted by the same reference characters. The pnp transistor 93 is fabricated by a process similar to that for fabricating the lateral pnp bipolar transistor shown in Fig. 1. In-fabricating the pnp transistor 93, an embedded n-type base layer 26 is formed on a p-type silicon substrate 1, an n-type epitaxial layer 4 is formed

over the embedded n-type layer 26, p-type isolation regions 37 and a field insulating layer 6 are formed, and then an n-type plug-in region 27 reaching the embedded n-type base region 27, and an n-type base contact region 28 are formed. A p-type collector region 62 and a p-type emitter region 61 are formed in the epitaxial layer 4 in a lateral arrangement with a spacing corresponding to the base width W_B so that portions of the p-type collector region 62 and the p-type emitter region 61 respectively having maximum impurity concentrations are formed within the bulk. In this embodiment, in particular, a heavily doped n-type region 94 having an impurity concentration higher than that of the epitaxial layer 4 and having a portion having a maximum impurity concentration is formed in an intrinsic region between the p-type collector region 62 and the p-type emitter region 61 on the same level as that on which the portions having the maximum impurity concentrations of the p-type collector region 62 and the p-type emitter region 61 are formed. The n-type region 94 must be formed so that the same does not overlap the collector region 62 and a p^+-type emitter region 61.

The heavily doped n-type region 94 having an impurity concentration higher than that of the epitaxial layer 4 and formed between the collector region 62 and the emitter region 61 prevents punch through attributable to the reduction in the base width W_B. The n-type region 94 not overlapping the collector region 62 and the emitter region 61 prevents increase in junction capacity. Thus, a stable, high-performance pnp transistor can easily fabricated.

A method of fabricating the lateral pnp transistor 93 simultaneously with the npn bipolar transistor 24 shown in Fig. 14 will be described hereinafter with reference to Figs. 9A, 9B and 9C, in which only the lateral pnp transistor 93 is shown. As shown in Fig. 9A, an n-type epitaxial layer 4 having an impurity concentration of $10^{15}/cm^3$ or below is formed over an embedded n-type base layer 26 and p-type channel stop regions 3 formed on a p-type silicon substrate 1, a field insulating layer 6 for element isolation is formed by selective oxidation, a thin SiO_2 film 7 is formed, and then an n-type base contact region 27 reaching the embedded base layer 26 is formed. Subsequently, collector openings 96 and an emitter opening 97 are formed in the thin SiO_2 film 7, and then p-type collector regions 62 and a p-type emitter region 61 are formed with a spacing corresponding to the base width W_B therebetween so that portions respectively having maximum impurity concentrations are formed within the epitaxial layer 4 through the ion implantation of a p-type impurity, such as boron, by using a resist mask 100 having openings 98 and 99 of a size greater than that of the openings 96 and 97, namely, openings 98 and 99 spaced apart by a distance smaller than that between the openings 96 and 97. The openings 96 and 97 in the thin SiO2 film 7 are formed simultaneously with an opening corresponding to a region including the base contact region, intrinsic base region and an active region in which an emitter region is to be formed of the npn bipolar transistor 24 (Fig. 14A).

Then, as shown in Fig. 9B, the resist mask 100 is removed, a polycrystalline silicon film 8 is deposited by a CVD process over the entire surface including the openings 96 and 97, the polycrystalline silicon film 8 is doped with a p-type impurity, such as boron, by ion implantation, and then the polycrystalline silicon film 8 is patterned by using a resist mask 111 to form collector contact electrodes 112 and an emitter contact electrode 113 of a p^+-type polycrystalline silicon film. The interval ℓ between the electrodes 112 and 113 corresponds to the base width W_B, namely, the interval between the collector region 62 and the emitter region 61. A portion of the p^+-type polycrystalline silicon film in the npn bipolar transistor 24 is patterned so that the shape of the remaining portion of the p^+-type polycrystalline silicon film corresponds to the external shape of the base contact electrode (Fig. 14B). Then, the epitaxial layer 4 is doped with an n-type impurity, such as arsenic, by ion implantation by using the same resist mask 111 to form a n-type region 94 having an impurity concentration on the order of $10^{17}/cm^3$ (a dose on the order of $10^{12}/cm^2$) in the intrinsic base regions between the collector regions 62 and the emitter region 61 so that portions respectively having maximum impurity concentrations of the doped regions are on a level the same as that on which the portions having the maximum impurity concentrations of the collector regions and the emitter region are formed.

Then, as shown in Fig. 9C, the entire surface is coated with a SiO_2 film 10. Thereafter, in the section for the npn bipolar transistor, the SiO_2 film 10 and the p^+-type polycrystalline silicon film 8 are patterned simultaneously to form a base contact electrode 12 of p^+-type polycrystalline silicon and an opening is formed to expose the active region. Subsequently, side walls are formed and boron is caused to diffuse from the collector contact electrodes 112 and the emitter contact electrode 113 formed of the p^+-type polycrystalline silicon film to form heavily doped collector regions 64 and a heavily doped emitter contact region 63. In the section for the npn transistor, a p^+-type external base region is formed. Subsequently, in the section for the npn transistor, a second polycrystalline silicon film is formed, the second polycrystalline silicon film is doped with a p-type impurity, such as boron, by ion implantation, the doped second polycrystalline silicon film is subjected to a heat treatment to form a p-type base region, and the second polycrystalline silicon film is doped with an n-type impurity, such as arsenic, by ion implantation to form an n-type emitter region. A portion of the n^+-type second polycrycrystalline silicon film forms an emitter contact electrode. Then, contact holes are formed in the insulating film consisting of the SiO_2 film 10 and the thin SiO_2 film 7, and then a collector electrode 34, base electrode 35 and an emitter electrode 36 are formed of an Al-Si alloy through a Ti/TiN film 114 in the contact holes to complete

the lateral pnp bipolar transistor 93 and the npn bipolar transistor 24, not shown.

Thus, the stable, high-performance lateral pnp transistor 93 having a reduced base width W_B and the very-high-speed npn bipolar transistor 24 can be simultaneously fabricated.

A lateral bipolar transistor in accordance with the first aspect of the present invention comprises collector regions and an emitter region each having a portion having a maximum impurity concentration formed within the substrate instead of the surface of the substrate, so that the influence of surface recombination is suppressed, a high h_{FE} is achieved, change in surface recombination current is reduced, the h_{FE} is uniform and stable.

A method of fabricating a lateral bipolar transistor, in accordance with the second aspect of the present invention forms collector regions, and an emitter region in a lateral arrangement on a semiconductor substrate serving as a base region by using a first mask provided with a pair of openings, and then forms heavily doped regions connected respectively to the collector regions and the emitter regions by using a second mask provided with openings formed at an interval smaller than that between the openings of the first mask to form the base region in a base width as small as the minimum line width which can be achieved by lithography. Thus, a lateral bipolar transistor thus fabricated has a high f_T and a high h_{FE}.

Although the invention has been described in its preferred forms with a certain degree of particularity, obviously many changes and variations are possible therein. It is therefore to be understood that the present invention may be practiced otherwise than as specifically described herein without departing from its scope as defined by the appended claims.

Claims

1. A semiconductor device comprising a semiconductor substrate (1) and a major surface opposite said substrate (1), said semiconductor device including a lateral bipolar transistor, said transistor comprising:

   a base region (26; 60) of a first conductivity type;
   an emitter region (61) and a collector region (62) both of a second, opposite conductivity type located in a lateral arrangement in said base region (60);
   an emitter contact region (63) and a collector contact region (64) both of the second conductivity type and having higher impurity concentrations than said emitter (61) and said collector (62) regions located in said base region (60), exposed at said major surface, and contacting said emitter region (61) and said collector region (62), respectively;

   characterized in that
   said emitter region (61) and said collector region (62) are buried within said base region (60),
   portions of said emitter region (61) and said collector region (62) nearest to each other each having a peak impurity concentration, the respective adjacent impurity concentrations of said emitter (61) and collector (62) regions closer to said major surface being lower than said peak impurity concentration, whereby a principal current passage is formed within said base region (60) instead of near said major surface.

2. The semiconductor device of claim 1, further comprising a heavily doped region (94) of said first conductivity type formed in a portion of said base region (60) between and at the same depth as that of said portions of the emitter region (61) and the collector region (62) nearest to each other, having an impurity concentration higher than that of said base region (60) and not overlapping said emitter (61) and collector (62) regions, whereby punch-through is prevented.

3. A method of fabricating the semiconductor device including a lateral bipolar transistor of claim 1, said method comprising the steps of:

   forming a first region (26) of a first conductivity type on a semiconductor substrate (1) of a second conductivity type;
   forming an epitaxial layer (4) of the first conductivity type having a major surface opposite to said substrate (1) on said first region and on said substrate, whereby said first region forms an embedded base region of said lateral bipolar transistor and said epitaxial layer (4) forms a base region (60) of said lateral bipolar transistor;
   forming an emitter region (61) and a collector region (62) of said lateral bipolar transistor, both of the second conductivity type, by ion implantation using a first mask (81) provided with a pair of openings separated from each other by a first distance, so that said emitter (61) and collector (62) regions have portions having a peak impurity concentration and are buried within said epitaxial layer (4), the respective adjacent impurity concentrations of said emitter (61) and collector (62) regions closer to said major surface being lower than said peak impurity concentration of said emitter (61) and collector (62) regions;
   forming an emitter contact region (63) and a collector contact region (64) of said lateral bipolar transistor, both of the second conductivity

type, having higher impurity concentrations than said emitter (61) and
said collector (62) regions in said epitaxial layer (4), and connected respectively to said emitter region (61) and said collector region (62), by using a second mask provided with a pair of openings separated from each other by a second distance greater than said first distance.

4. A method of fabricating a semiconductor device including the semiconductor device including a lateral bipolar transistor of claim 1 as well as a low emitter concentration transistor, said method comprising the steps of:

forming a first region (26), and a second region (68), both of a first conductivity type in a lateral bipolar transistor forming section (66), and a low emitter concentration transistor forming section (67) on a semiconductor substrate (1) of a second, opposite conductivity type, respectively;
forming an epitaxial layer (4) of the first conductivity type, having a major surface opposite to said substrate (1) on said first and second regions (26; 68) and on said substrate (1), whereby said first region (26) forms an embedded base region of said lateral bipolar transistor, said second region (68) forms an embedded collector region of said low emitter concentration transistor, and said epitaxial layer (4) forms a base region (60) of said lateral bipolar transistor and a collector region of said low emitter concentration transistor;
forming isolation regions (37) of the second conductivity type and a field insulating layer (6);
forming an emitter region (61) and a collector region (62) of said lateral bipolar transistor in said lateral bipolar transistor forming section (66), both of the second conductivity type so that said emitter (61) and collector (62) regions have portions having a peak impurity concentration and are buried within said epitaxial layer (4). the respective adjacent impurity concentrations of said emitter (61) and collector (62) regions closer to said major surface being lower than said peak impurity concentration of said emitter (61) and collector (62) regions,
and, simultaneously, a base region (83) of the second conductivity type for the low emitter concentration transistor in said low emitter concentration transistor forming section (67), by ion implantation in said epitaxial layer (4), using a first mask (81) provided with a pair of openings separated from each other by a first distance in said lateral bipolar transistor forming section (66);
forming an emitter contact region (63) and a collector contact region (64) of said lateral bipolar transistor in said lateral bipolar transistor forming section (66) and, at the same time, a base contact region (84) for the low emitter concentration transistor in said low emitter concentration transistor forming section (67), all three of the second conductivity type and having higher impurity concentrations than said emitter (61) and said collector (62) regions of said lateral bipolar transistor and said base (83) region of said low emitter concentration transistor in said epitaxial layer (4) and connected respectively to said emitter region (61) and said collector region (62) of said lateral bipolar transistor and said base region (83) of said low emitter concentration transistor, by using a second mask provided with a pair of openings in said lateral bipolar transistor forming section (66) separated from each other by a second distance greater than said first distance;
forming simultaneously in said epitaxial layer (4) an emitter region (85) and a collector contact region (86) for said low emitter concentration transistor in said low emitter concentration transistor forming section (67) as well as a base contact region (28) for said lateral bipolar transistor in said lateral bipolar transistor forming section (68), all three of the first conductivity type.

Patentansprüche

1. Halbleiterbauteil mit einem Halbleitersubstrat (1) und einer vom Substrat (1) abgewandten Hauptfläche, wobei das Halbleiterbauteil einen lateralen Bipolartransistor mit folgendem enthält:

- einem Basisbereich (26; 60) von erstem Leitungstyp;
- einem Emitterbereich (61) und einem Kollektorbereich (62), die beide von einem zweiten, entgegengesetzten Leitungstyp sind und in einer Lateralanordnung im Basisbereich (60) liegen;
- einem Emitterkontaktbereich (63) und einem Kollektorkontaktbereich (64), die beide vom zweiten Leitungstyp sind und höhere Verunreinigungskonzentration als der Emitterbereich (61) und der Kollektorbereich (62) aufweisen, die im Basisbereich (60) liegen, wobei sie an der Hauptfläche freiliegen und den Emitterbereich 61 bzw. den Kollektorbereich (62) kontaktieren;

dadurch gekennzeichnet, dass

- der Emitterbereich (61) und der Kollektorbereich (62) innerhalb des Basisbereichs (60) ver-

graben sind;

- Abschnitte des Emitterbereichs (61) und des Kollektorbereichs (62), die am nächsten beieinander liegen, jeweils einen Spitzenwert der Fremdstoffkonzentration aufweisen, wobei jeweils benachbarte Fremdstoffkonzentrationen des Emitterbereichs (61) und des Kollektorbereichs (62), die näher an der Hauptfläche liegen, niedriger als der Spitzenwert der Fremdstoffkonzentration sind, wodurch ein Hauptstromkanal innerhalb des Basisbereichs (60) anstatt nahe an der Hauptfläche ausgebildet ist.

2. Halbleiterbauteil nach Anspruch 1, ferner mit einem stark dotierten Bereich (94) vom ersten Leitungstyp, der in einem Abschnitt des Basisbereichs (60) zwischen den Abschnitten des Emitterbereichs (61) und des Kollektorbereichs (62), die am nächsten beieinander liegen, und in derselben Tiefe wie diese ausgebildet ist, mit einer Fremdstoffkonzentration, die über der des Basisbereichs (60) liegt, ohne Überlappung mit dem Emitterbereich (61) und dem Kollektorbereich (62), wodurch Durchschläge verhindert sind.

3. Verfahren zum Herstellen des Halbleiterbauteils mit einem lateralen Bipolartransistor gemäß Anspruch 1, das folgende Schritte umfasst:

- Herstellen eines ersten Bereichs (26) von erstem Leitungstyp auf einem Halbleitersubstrat (1) von zweitem Leitungstyp;
- Herstellen einer Epitaxieschicht (4) vom ersten Leitungstyp mit einer vom Substrat (1) abgewandten Hauptfläche auf dem ersten Bereich und auf dem Substrat, wodurch der erste Bereich einen vergrabenen Basisbereich des lateralen Bipolartransistors bildet und die Epitaxieschicht (4) einen Basisbereich (60) des lateralen Bipolartransistors bildet;
- Herstellen eines Emitterbereichs (61) und eines Kollektorbereichs (62) des lateralen Bipolartransistors, die beide vom zweiten Leitungstyp sind, durch Ionenimplantation unter Verwendung einer ersten Maske (81), die mit einem Paar Öffnungen versehen ist, die voneinander um einen ersten Abstand beabstandet sind, so dass der Emitterbereich (61) und der Kollektorbereich (62) Abschnitte mit einem Spitzenwert der Fremdstoffkonzentration aufweisen, und sie innerhalb der Epitaxieschicht (4) vergraben sind, wobei jeweils benachbarte Fremdstoffkonzentrationen des Emitterbereichs (61) und des Kollektorbereichs (62), die näher an der Hauptfläche liegen, niedriger sind als der Spitzenwert der Fremdstoffkonzentration des Emitterbereichs (61) und des Kollektorbereichs (62);
- Herstellen eines Emitterkontaktbereichs (63) und eines Kollektorkontaktbereichs (64) des lateralen Bipolartransistors, die beide vom zweiten Leitungstyp sind, die höhere Fremdstoffkonzentration als der Emitterbereich (61) und der Kollektorbereich (62) in der Epitaxieschicht (4) aufweisen, und die mit dem Emitterbereich (61) bzw. dem Kollektorbereich (62) verbunden werden, wozu eine zweite Maske verwendet wird, die mit einem Paar Öffnungen versehen ist, die voneinander um einen zweiten Abstand beabstandet sind, der größer als der erste Abstand ist.

4. Verfahren zum Herstellen eines Halbleiterbauteils mit dem Halbleiterbauteil mit einem lateralen Bipolartransistor nach Anspruch 1, und mit einem Transistor mit niedriger Emitterkonzentration, wobei das Verfahren folgende Schritte umfasst:

- Herstellen eines ersten Bereichs (26) und eines zweiten Bereichs (68), beide von einem ersten Leitungstyp, in einem Abschnitt (66) zum Herstellen eines lateralen Bipolartransistors bzw. einem Abschnitt (67) zum Herstellen eines Transistors mit niedriger Emitterkonzentration auf einem Halbleitersubstrat (1) von zweitem, entgegengesetztem Leitungstyp;
- Herstellen einer Epitaxieschicht (4) vom ersten Leitungstyp, mit einer Hauptfläche, die vom Substrat (1) abgewandt ist, auf dem ersten und zweiten Bereich (26; 68) und auf dem Substrat (1), wodurch der erste Bereich (26) einen vergrabenen Basisbereich des lateralen Bipolartransistors bildet, wobei der zweite Bereich (68) einen vergrabenen Kollektorbereich des Transistors mit niedriger Emitterkonzentration bildet, und die Epitaxieschicht (4) den Basisbereich (60) des lateralen Bipolartransistors und den Kollektorbereich des Transistors mit niedriger Emitterkonzentration bildet;
- Herstellen von Isolierbereichen (37) vom zweiten Leitungstyp sowie einer Feldisolierschicht (6);
- Herstellen eines Emitterbereichs (61) und eines Kollektorbereichs (62) des lateralen Bipolartransistors im Abschnitt (66) zum Herstellen des lateralen Bipolartransistors, die beide vom zweiten Leitungstyp sind, so dass der Emitterbereich (61) und der Kollektorbereich (62) Abschnitte mit einem Spitzenwert der Fremdstoffkonzentration aufweisen, und sie innerhalb der Epitaxieschicht (4) vergraben sind, wobei jeweils benachbarte Fremdstoffkonzentrationen des Emitterbereichs (61) und des Kollektorbereichs (62), die näher an der Hauptoberfläche liegen, niedriger als der Spitzenwert der

Fremdstoffkonzentration im Emitterbereich (61) und im Kollektorbereich (62) sind, und gleichzeitiges Herstellen eines Basisbereichs (83) vom zweiten Leitungstyp für den Transistor mit niedriger Emitterkonzentration im Abschnitt (67) zum Herstellen des Emitters mit niedriger Emitterkonzentration durch Ionenimplantation in der Epitaxieschicht (4) unter Verwendung einer ersten Maske (81), die mit einem Paar Öffnungen versehen ist, die voneinander um einen ersten Abstand beabstandet sind, was im Abschnitt (66) zum Herstellen des lateralen Bipolartransistors erfolgt;

- Herstellen eines Emitterkontaktbereichs (63) und eines Kollektorkontaktbereichs (64) des lateralen Bipolartransistors im Abschnitt (66) zum Herstellen des lateralen Bipolartransistors, mit gleichzeitigem Herstellen eines Basiskontaktbereichs (64) für den Transistor mit niedriger Emitterkonzentration im Abschnitt (67) zum Herstellen des Transistors mit niedriger Emitterkonzentration, die alle drei vom selben Leitungstyp sind und eine höhere Fremdstoffkonzentration als der Emitterbereich (61) und der Kollektorbereich (62) des lateralen Bipolartransistors sowie der Basisbereich (83) des Transistors mit niedriger Emitterkonzentration in der Epitaxieschicht (4) aufweisen und sie mit dem Emitterbereich (61) und dem Kollektorbereich (62) des lateralen Bipolartransistors bzw. dem Basisbereich (83) des Transistors mit niedriger Emitterkonzentration verbunden werden, wozu eine zweite Maske verwendet wird, die mit einem Paar Öffnungen versehen ist, was im Abschnitt (66) zum Herstellen des lateralen Bipolartransistors erfolgt, die voneinander um einen zweiten Abstand beabstandet sind, der größer als der erste Abstand ist;
- gleichzeitiges Herstellen eines Emitterbereichs (85) und eines Kollektorkontaktbereichs (66) für den Transistor mit niedriger Emitterkonzentration in der Epitaxieschicht (4) im Abschnitt (67) zum Herstellen des Transistors mit niedriger Emitterkonzentration, wie auch eines Basiskontaktbereichs (28) für den lateralen Bipolartransistor im Abschnitt (68) zum Herstellen des lateralen Bipolartransistors, wobei alle drei vom ersten Leitungstyp sind.

Revendications

1. Dispositif semi-conducteur comprenant un substrat semi-conducteur (1) et une surface principale opposée audit substrat (1), ledit dispositif semi-conducteur comprenant un transistor bipolaire latéral, ledit transistor comprenant :

une zone de base (26 ; 60) d'un premier type de conductivité ;
une zone d'émetteur (61) et une zone de collecteur (62) les deux d'un second type de conductivité opposée situées dans une disposition latérale dans ladite zone de base (60) ;
une zone de contact d'émetteur (63) et une zone de contact de collecteur (64) les deux du second type de conductivité et ayant des concentrations d'impureté pius élevées que lesdites zones d'émetteur (61) et de collecteur (62) situées dans ladite zone de base (60) exposées sur ladite surface principale, et respectivement en contact avec ladite zone d'émetteur (61) et ladite zone de collecteur (62) :

caractérisé en ce que

ladite zone d'émetteur (61) et ladite zone de collecteur (62) sont enterrées dans ladite zone de base (60),
des parties de ladite zone d'émetteur (61) et de ladite zone de collecteur (62) plus proches l'une de l'autre, ayant chacune une crête de concentration d'impureté, les concentrations d'impureté voisines respectives desdites zones d'émetteur (61) et de collecteur (62) plus proches de ladite surface principale étant plus petite que ladite concentration d'impureté de crête, de sorte qu'un passage de courant principal est formé dans ladite zone de base (60) au lieu de près de ladite surface principale.

2. Dispositif semi-conducteur selon la revendication 1, comprenant en outre une zone fortement dopée (94) dudit premier type de conductivité formée dans une partie de ladite zone de base (60) entre et à la même profondeur que celle desdites parties de ladite zone d'émetteur (61) et de ladite zone de collecteur (62) plus proches l'une de l'autre, ayant une concentration d'impureté plus élevée que celle de ladite zone de base (60) et ne recouvrant pas lesdites zones d'émetteur (61) et de collecteur (62), de sorte qu'un claquage est empêché.

3. Procédé de fabrication d'un dispositif semi-conducteur comprenant un transistor bipolaire latéral dudit transistor bipolaire latéral, ledit procédé comprenant les étapes de :

formation d'une première zone (26) d'un premier type de conductivité sur un substrat semi-conducteur (1) d'un second type de conductivité ;
formation d'une couche épitaxiale (4) du premier type de conductivité ayant une surface principale opposée audit substrat (1) sur ladite première zone et sur ledit substrat, de sorte que

ladite première zone forme une zone de base enterrée dudit transistor bipolaire latéral et ladite couche épitaxiale (4) forme une zone de base (60) dudit transistor bipolaire latéral ;
formation d'une zone d'émetteur (61) et d'une zone de collecteur (62) les deux du second type de conductivité, par implantation ionique en utilisant un premier masque (81) pourvu d'une paire d'ouvertures séparées l'une de l'autre d'une première distance, de sorte que lesdites zones d'émetteur (61) et de collecteur (62) ont des parties ayant une concentration d'impureté de crête et sont enterrées dans ladite couche épitaxiale (4), lès concentrations d'impureté adjacentes respectives desdites zones d'émetteur (61) et de collecteur (62) plus proches de ladite surface principale étant plus petite que ladite concentration d'impureté desdites zone d'émetteur (61) et de collecteur (62) ;
formation d'une zone de contact d'émetteur (63) et d'une zone de contact de collecteur (64) dudit transistor bipolaire latéral, les deux du second type de conductivité, ayant des concentrations d'impureté plus élevées que lesdites zones d'émetteur (61) et de collecteur (62) dans ladite couche épitaxiale (4), et raccordées respectivement auxdites zones d'émetteur (61) et de collecteur (62), en utilisant un second masque pourvu d'une paire d'ouvertures séparées l'une de l'autre d'une seconde distance plus grande que ladite première distance.

4. Procédé de fabrication d'un dispositif semi-conducteur comprenant le dispositif semi-conducteur comprenant un transistor bipolaire latéral selon la revendication 1 ainsi qu'un transistor de faible concentration d'émetteur, ledit procédé comprenant les étapes de :

formation d'une première zone (26) et d'une seconde zone (68) les deux d'un premier type de conductivité dans une section de formation de transistor bipolaire latéral (66), et respectivement une section de formation de transistor de faible concentration d'émetteur (67) sur un substrat semi-conducteur (1) d'un second type de conductivité opposée ;
formation d'une couche épitaxiale (4) d'un premier type de conductivité, ayant une surface principale opposée audit substrat (1) sur lesdites première et seconde zones (26, 68) sur ledit substrat (1), de sorte que ladite première zone (26) forme une zone de base enterrée dudit transistor bipolaire latéral, ladite seconde zone (68) forme une zone de collecteur enterrée dudit transistor de faible concentration d'émetteur, et ladite couche épitaxiale (4) forme une zone de base (60) dudit transistor bipolaire latéral et une zone de collecteur dudit transistor à faible concentration d'émetteur ;
formation d'une zone isolante (37) d'un second type de conductivité et d'une couche isolante épaisse (6) ;
formation d'une zone de contact d'émetteur (61) et d'une zone de contact de collecteur (62) dudit transistor bipolaire latéral dans ladite section de formation de transistor bipolaire latéral (66), les deux du second type de conductivité de sorte que lesdites zones d'émetteur (61) et de collecteur (62) ont des parties ayant une concentration d'impureté de crête et sont enterrées dans ladite couche épitaxiale (4), les concentrations d'impureté adjacentes respectives desdites zones d'émetteur (61) et de collecteur (62) plus proches de ladite surface principale étant plus petite que ladite concentration d'impureté de crête desdites zones d'émetteur (61) et de collecteur (62), et, simultanément, une zone de base (83) du second type de conductivité pour le transistor à faible concentration d'émetteur dans ladite section de formation de transistor à faible concentration d'émetteur (67), par implantation ionique dans ladite couche épitaxiale (4), utilisant un premier masque (81) pourvu d'une paire d'ouvertures séparées l'une de l'autre d'une première distance dans ladite section de formation de transistor bipolaire latéral (66) ;
formation d'une zone de contact d'émetteur (63) et d'une zone de contact de collecteur (64) dudit transistor bipolaire latéral dans ladite section de formation de transistor bipolaire latéral (66) et, en même temps, une zone de contact de base (84) pour le transistor à faible concentration d'émetteur dans ladite section de formation de transistor à faible concentration d'émetteur (67), toutes les trois du second type de conductivité et ayant une concentration d'impureté plus élevée que lesdites zones d'émetteur (61) et de collecteur (62) dudit transistor bipolaire latéral et ladite zone de base (83) dudit transistor à faible concentration d'émetteur dans ladite couche épitaxiale (4) et respectivement raccordées à ladite zone d'émetteur (61) et à ladite zone de collecteur (62) dudit transistor bipolaire latéral et ladite zone de base (83) dudit transistor à faible concentration d'émetteur, en utilisant un second masque pourvu d'une paire d'ouvertures dans ladite section de formation de transistor bipolaire latéral (66) séparées l'une de l'autre d'une seconde distance plus grande que ladite première distance ;
formation simultanément dans ladite couche d'alliage d'aluminium (4) d'une zone d'émetteur (85) et d'une zone de contact de collecteur (86) pour ledit transistor à faible concentration

d'émetteur dans ladite section de formation de transistor à faible concentration d'émetteur (67) ainsi qu'une zone de contact de base (28) pour ledit transistor bipolaire latéral dans ladite section de formation de transistor bipolaire latéral (68), toutes les trois du premier type de conductivité.

FIG. 1

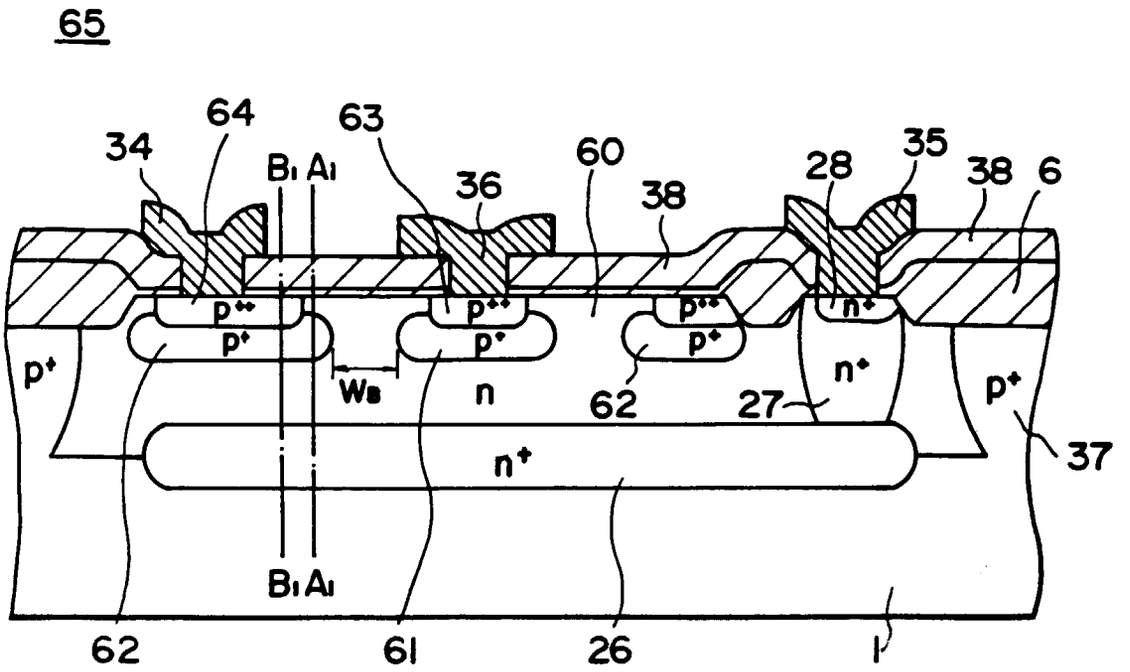

FIG. 2

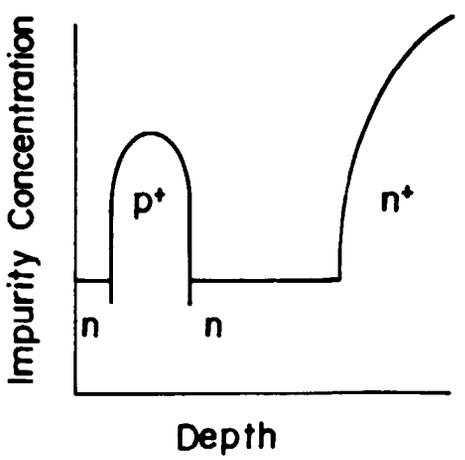

FIG. 3

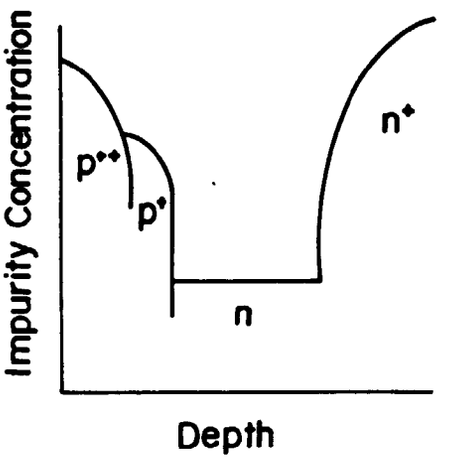

FIG. 4A

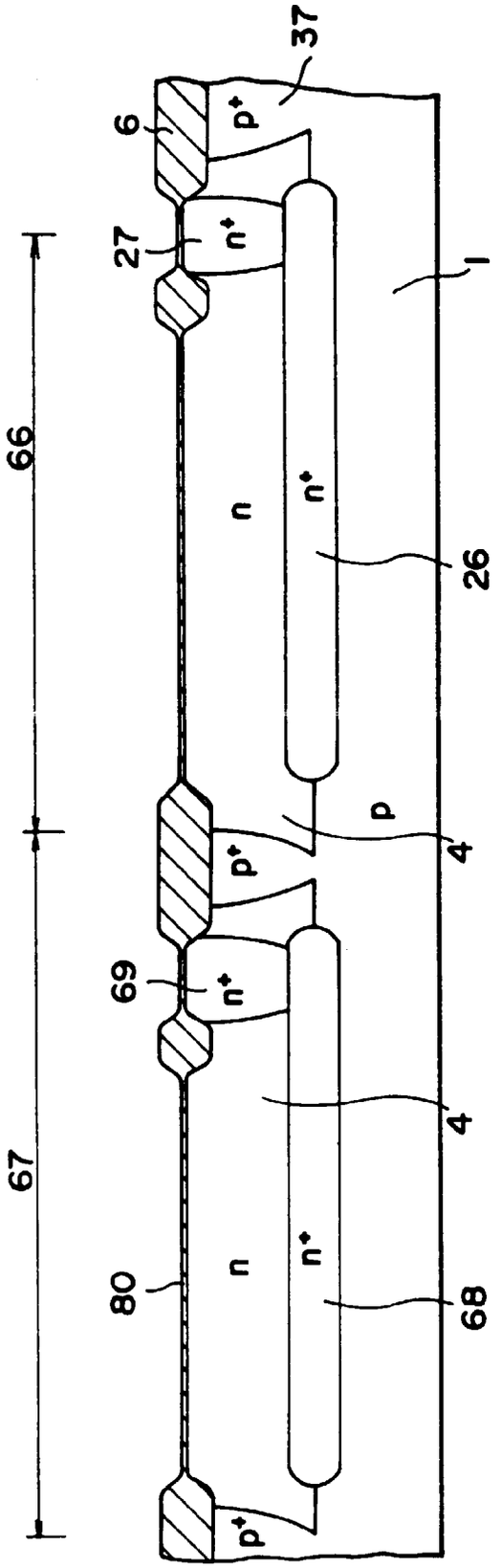
37
6
p+
27
n+
1
66
n
n+
26
p
4
p+
69
n+
4
67
80
n
n+
68
p+

FIG. 4B

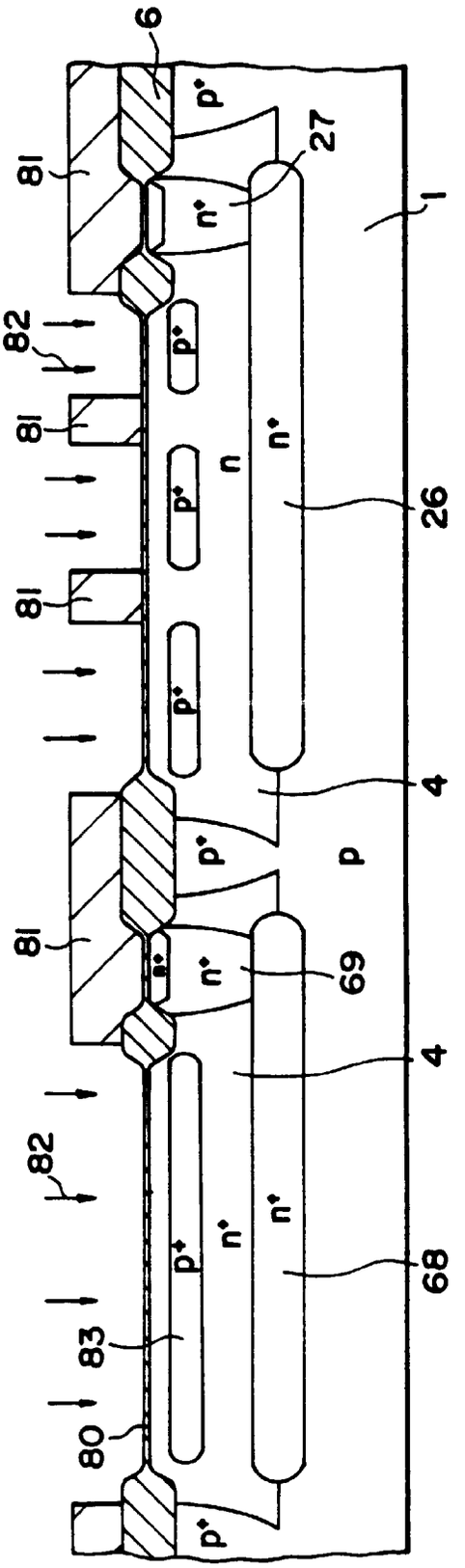
6
p+
81
27
n+
1
82
p+
81
n
n+
26
p+
81
p+
4
p+
81
p
n+
69
4
82
p+
n+
n+
68
83
80
p+

FIG. 4C

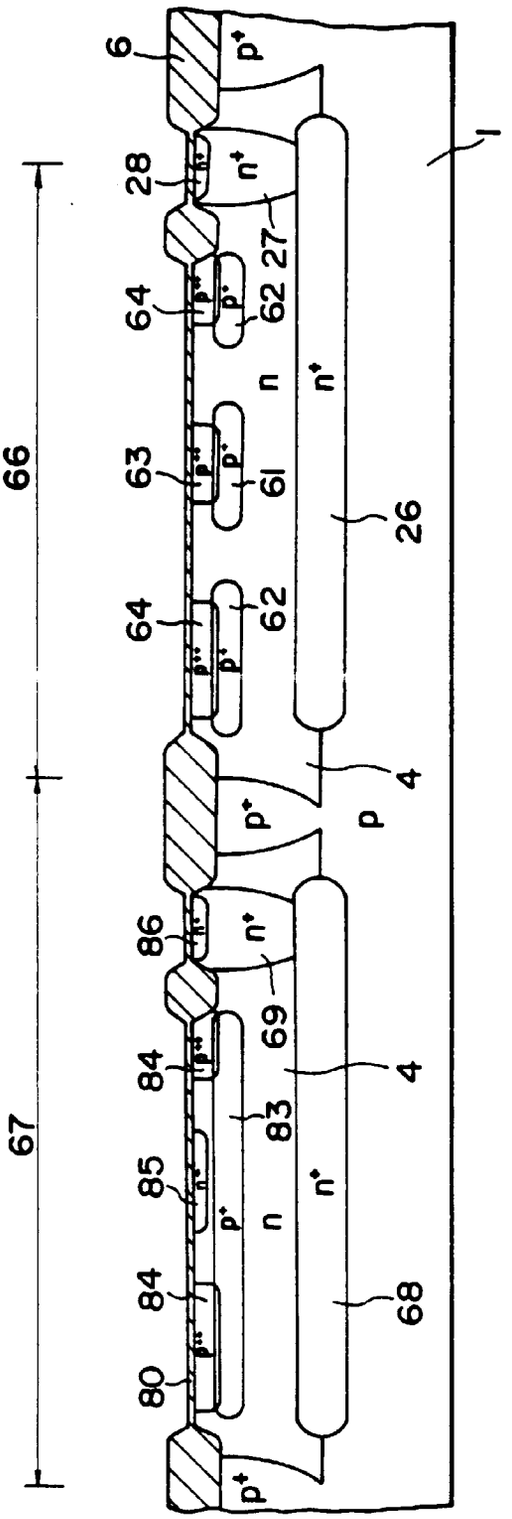
6
28
64
63
64
86
84
85
84
80
66
67
p+
n+
p'
p''
n
p
1
4
26
27
62
61
69
83
68

FIG. 4D

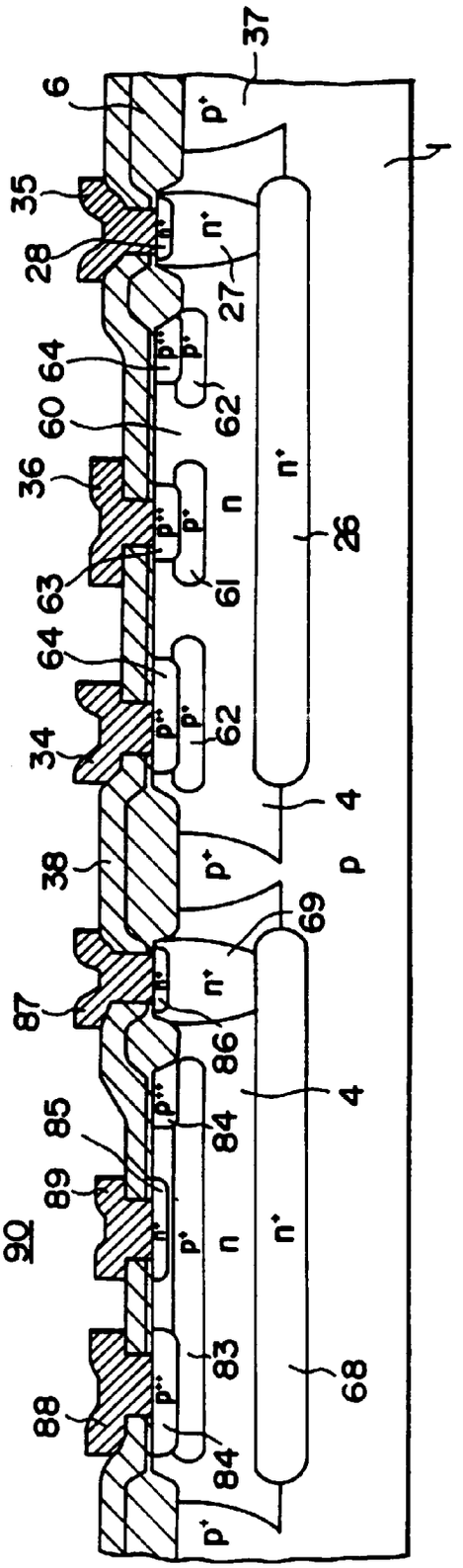
37
6
35
28
64
60
36
63
64
34
38
87
85
89
90
88
p+
n+
p'
p''
n
p
1
4
26
27
62
61
69
86
84
83
68

FIG. 5

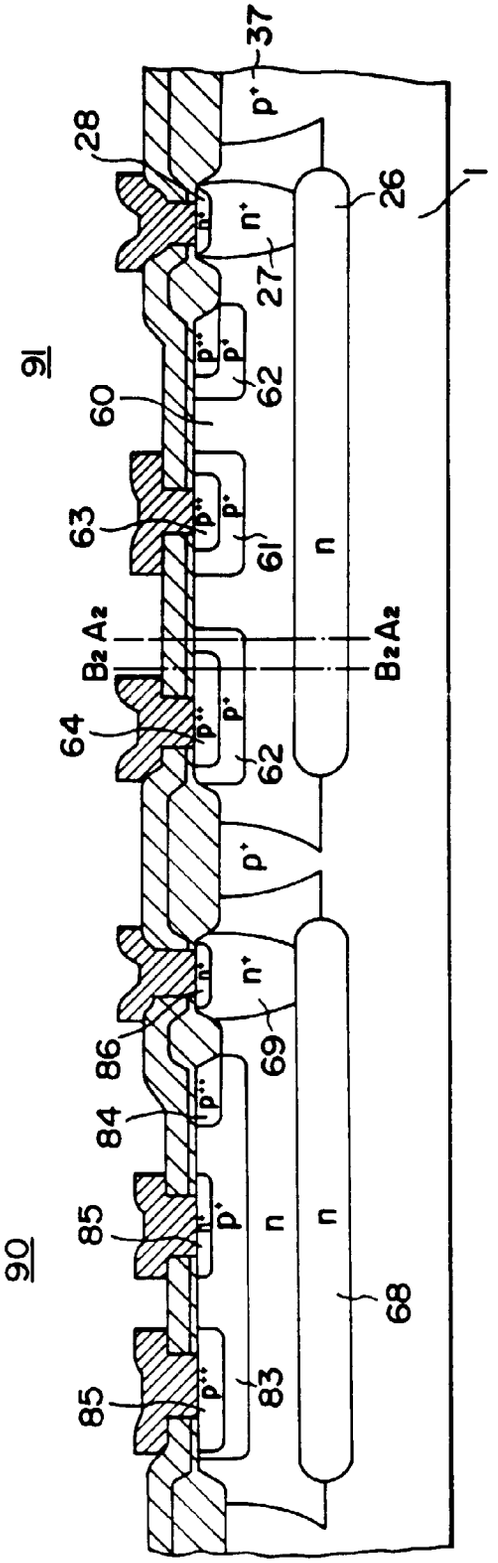

FIG. 7

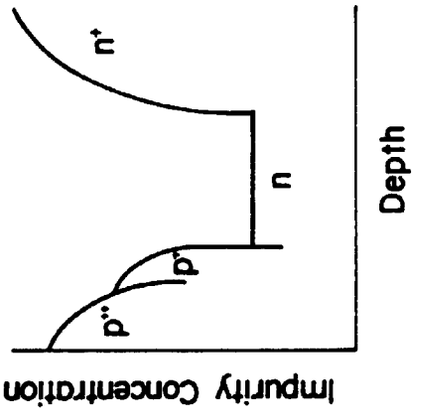

FIG. 6

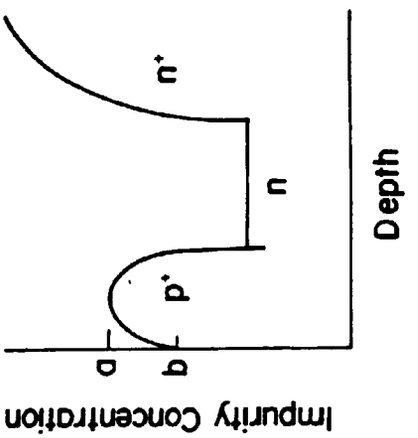

FIG. 8

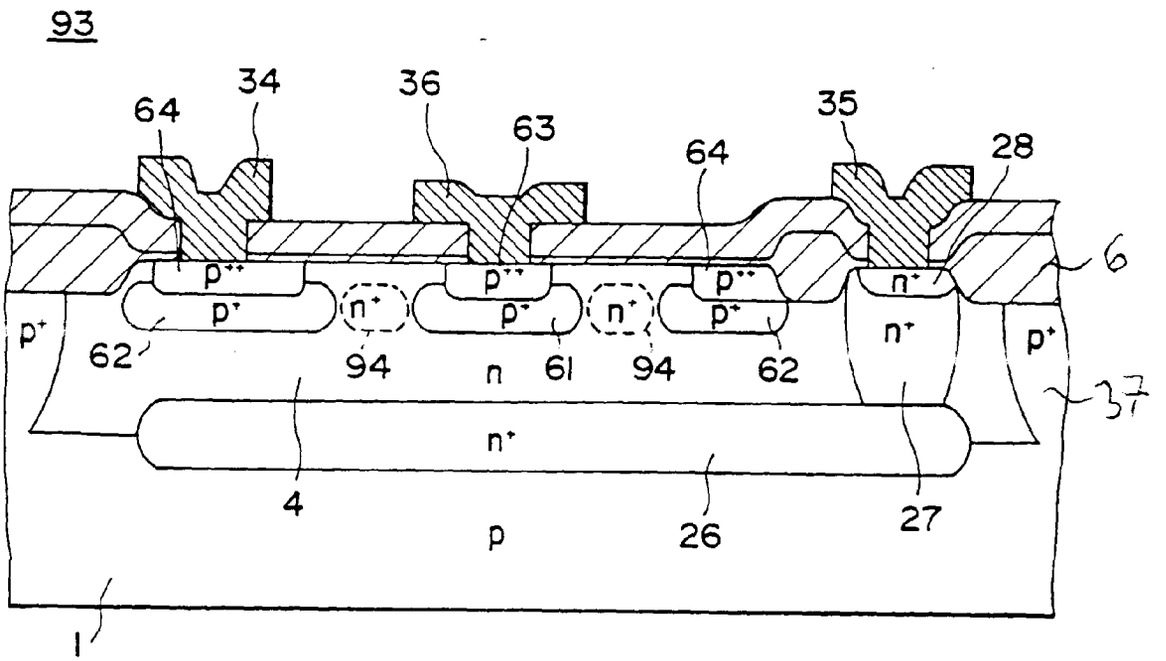

FIG. 9A

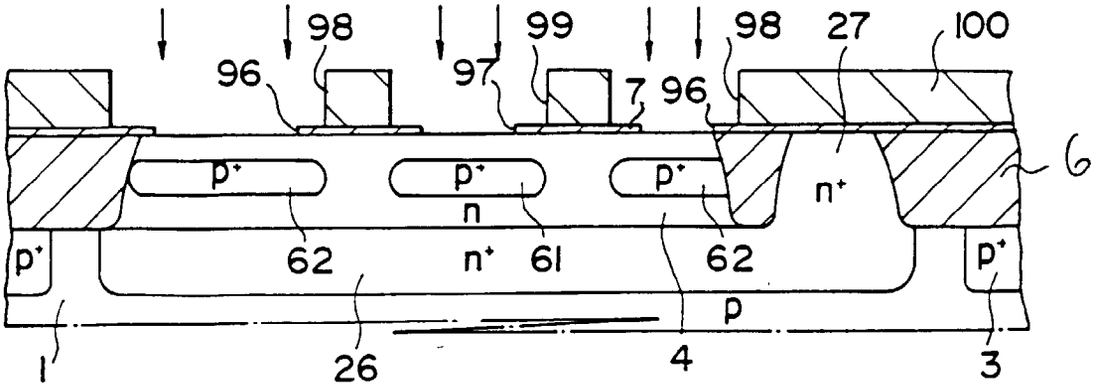

FIG. 9B

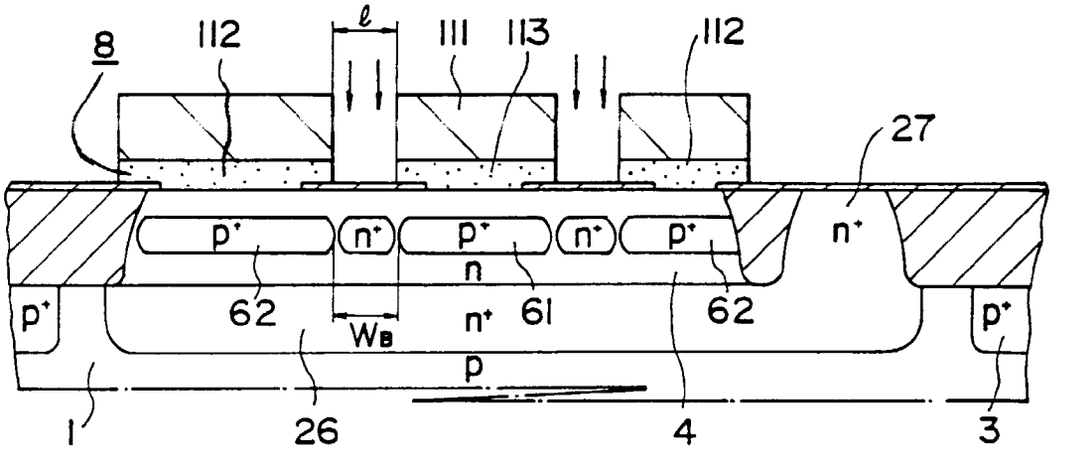

FIG. 9C

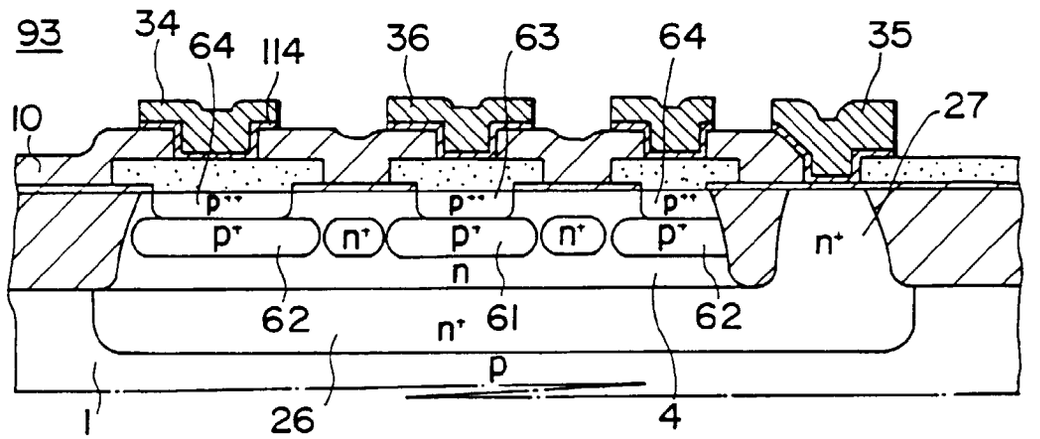

FIG. 10

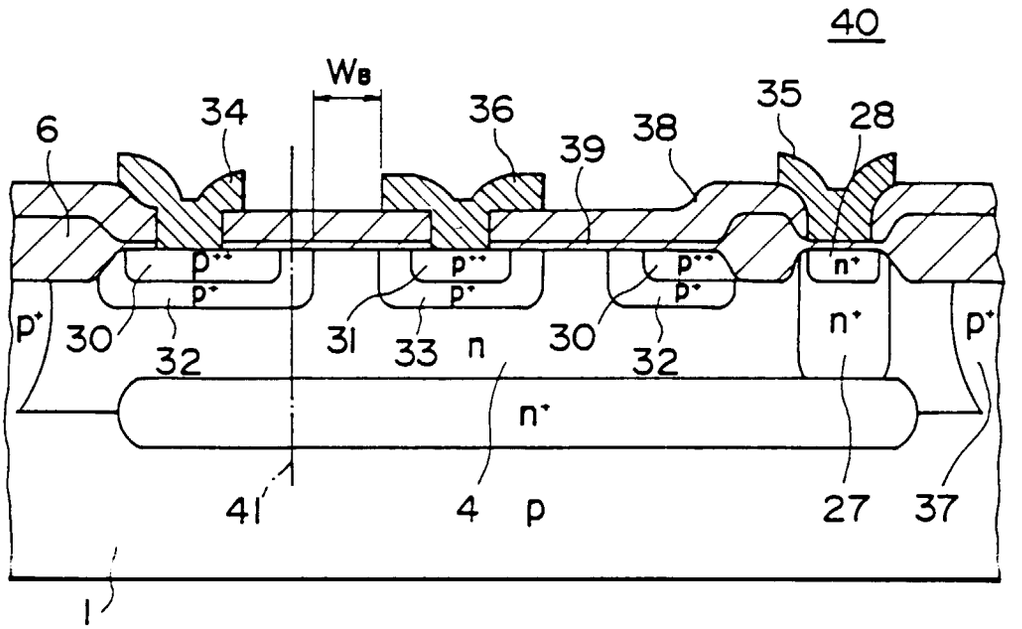
40
W_B
6
34
36
39
38
35
28
p^{++}
p^+
n^+
p^+
30
32
31
33
n
30
32
n^+
p^+
n^+
41
4
p
27
37
1

FIG. 11

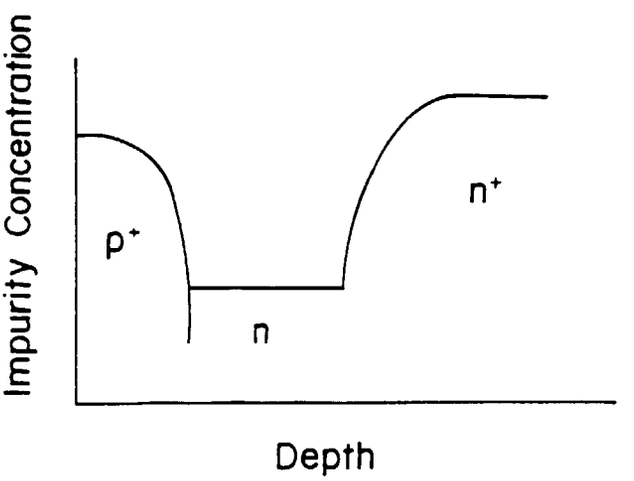
Impurity Concentration
p^+
n
n^+
Depth

FIG. 12

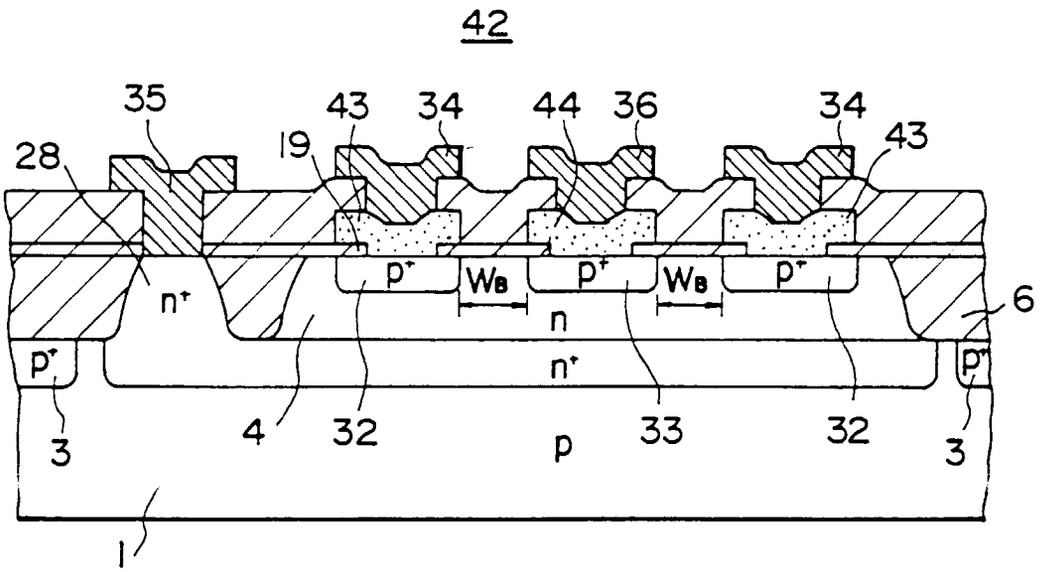
42
35
43
34
44
36
34
43
28
19
p+
WB
p+
WB
p+
6
n+
n
p+
n+
p+
3
4
32
33
32
3
p
1

FIG. 13

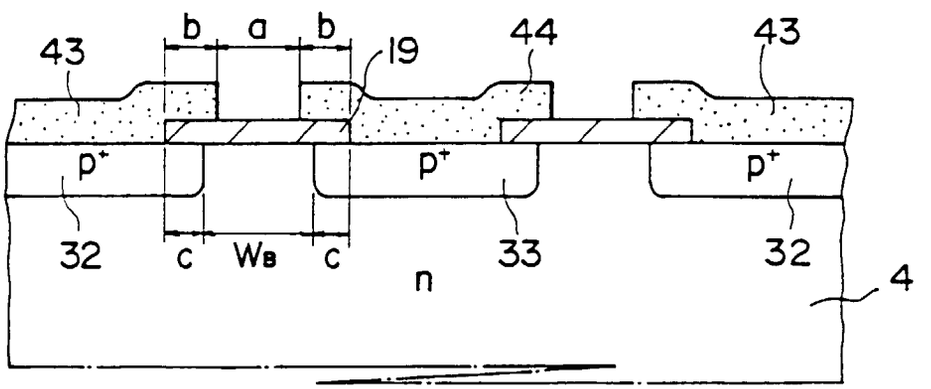
b
a
b
43
19
44
43
p+
p+
p+
32
c
WB
c
33
32
n
4

FIG. 14A

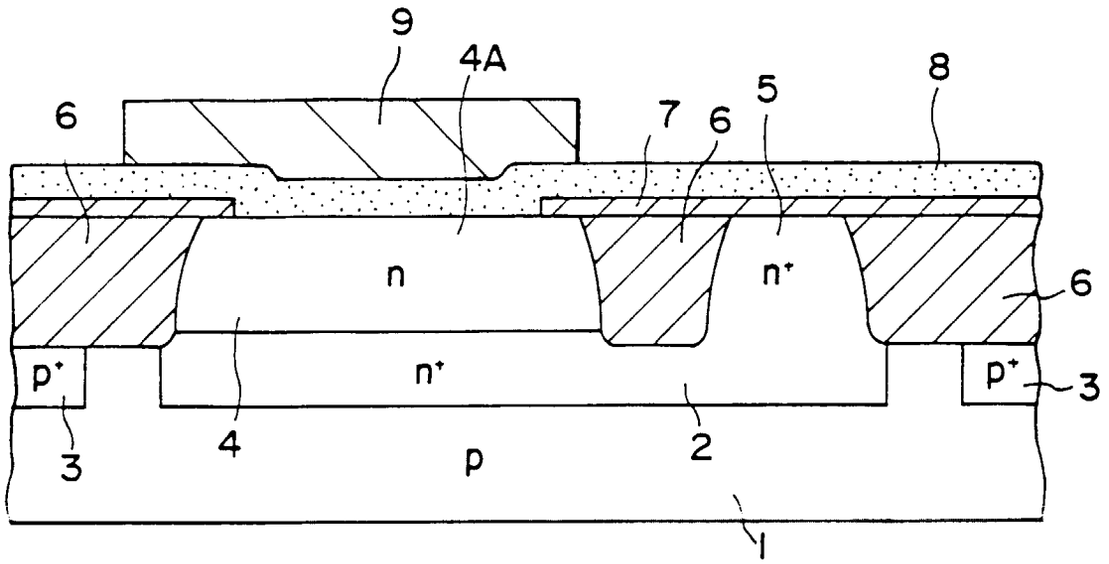

FIG. 14B

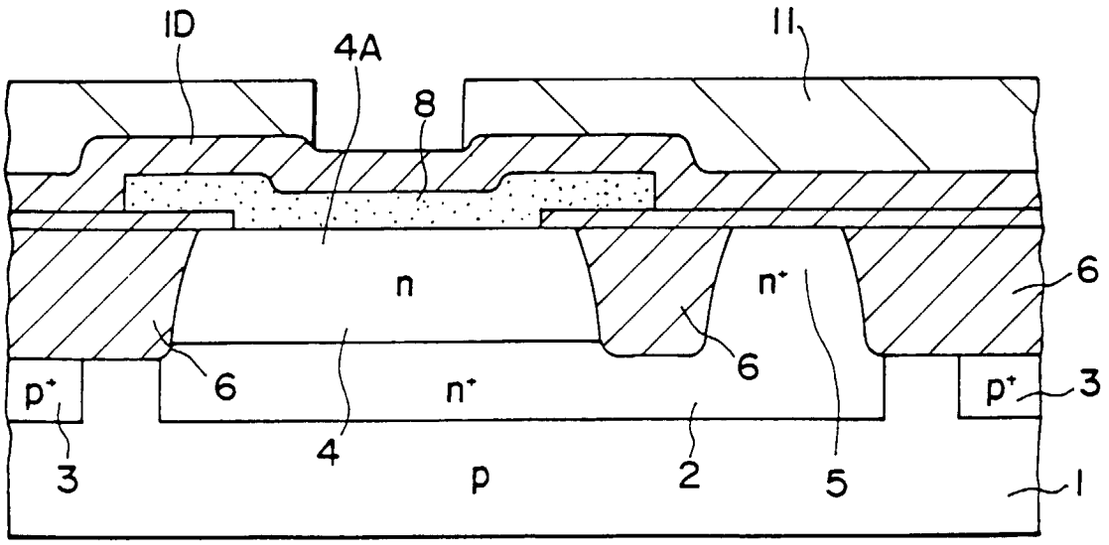

FIG. 14C

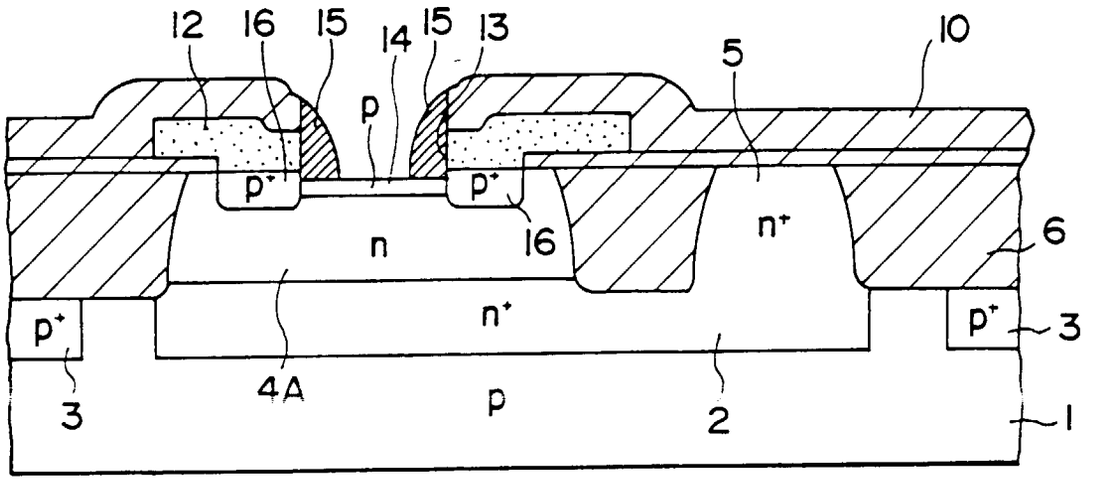

FIG. 14D