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(54) Method of driving a liquid crystal panel.

(57) In a method of driving a liquid crystal panel comprising scanning electrodes on a substrate and signal electrodes on another substrate, between which substrates a liquid crystal layer is sandwiched, scanning electrode driving waveforms (a) consisting of selective and non-selective voltages are applied to the scanning electrodes of the liquid crystal panel. Lighting or non-lighting voltages (b and c) are applied to the signal electrodes. Polarities of the lighting and non-lighting voltages are inverted with respect to the non-selective voltages to thereby drive the liquid crystal panel. During a period (TC, tc) the selective voltage is not applied to any of the scanning electrodes and a compensating voltage is applied to each signal electrode in accordance with the number of variations in the polarities of the voltages applied to the respective signal electrode with respect to the non-selective voltages applied to the scanning electrodes during a constant period.

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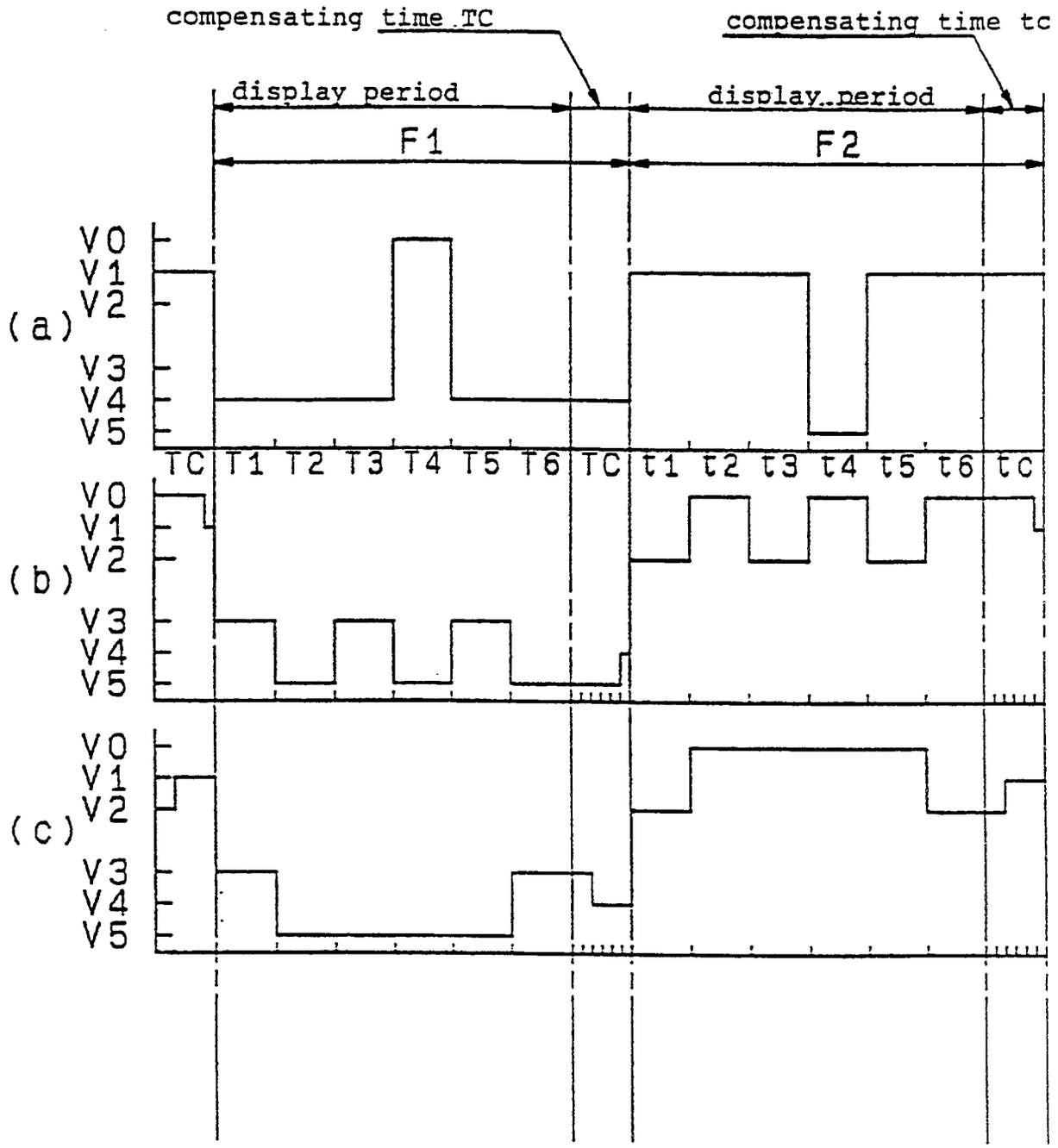

compensating time TC
compensating time tc
display period
display period
F1
F2
(a)
(b)
(c)
V0
V1
V2
V3
V4
V5
TC T1 T2 T3 T4 T5 T6 TC t1 t2 t3 t4 t5 t6 tc

FIG. 1

METHOD OF DRIVING A LIQUID CRYSTAL PANEL

The present invention relates to methods of driving liquid crystal panels.

The operation of driving a simple matrix liquid crystal panel has hitherto involved the use of a driving method generally known as a voltage averaging method.

Based on this driving method, selection voltages are sequentially impressed on scanning electrodes, and in synchronization with this process lighting or non-lighting voltages are applied to signal electrodes.

In practice, a liquid crystal panel is constructed of scanning and signal electrodes, each having a non-zero resistance, and a liquid crystal layer which functions as a dielectric substance. For this reason, when driving the liquid crystal panel by the conventional voltage averaging method, effective voltages impressed on display dots composed of intersecting scanning and signal electrodes vary in many ways depending on a character or graphic pattern displayed on the liquid crystal panel. This results in non-uniform display.

The problem is a classical one. A countermeasure against this problem may be, for instance, a method (hereinafter referred to as a line inversion driving method) of inverting a polarity of the voltage applied to the liquid crystal panel several times during one frame. This method is disclosed in Japanese Patent Laid-Open Publication Nos. 31825/1987, 19195/1985 and 19196/1985.

The line inversion driving method resulted in some improvement in an otherwise non-uniform display. In this case, the non-uniform display appeared when optical characteristics of the liquid crystal sandwiched in between the liquid crystal panels changed depending on a frequency component of the voltage applied. This method could not completely eliminate the unevenness of display. As a result of research by the inventor of the present invention and others in the applicant company, it was found that the display unevenness was caused by some remaining factors, explained hereinafter by reference to Figures 11 to 14. In a liquid crystal panel 1 (Figure 11) a liquid crystal layer (not shown) is sandwiched between substrates 2 and 3. Formed on the substrate 2 is a plurality of scanning electrodes Y1 to Y6. A plurality of signal electrodes X1 to X6 is formed on the substrate 3. It will be appreciated that only six scanning electrodes and six signal electrodes are shown for the sake of simplicity, but that many more of both could be used in practice. Display dots may be lit up at the intersections of the scanning electrodes Y1 to Y6 and the signal electrodes X1 to X6. In Figure 11, those display dots which are lit up are indicated as hatched. This liquid crystal panel is driven so that the selective voltages are applied to the scanning electrodes Y1 to Y6 sequentially, and repeatedly so that the selective voltage is applied again to Y1 subsequent to being applied to Y6. At this time, lighting voltages are impressed on the respective signal electrodes X1 to X6, if the display dots at the intersections of the signal and scanning electrodes are to be lit up while the selective voltages are applied to the scanning electrodes. If the display dots are not to be lit up, non-lighting voltages are applied to the respective signal electrodes. When the effective voltages applied to the display dot intersections increase, so-called positive display is effected, wherein the display appears to be dense. In order to prevent a direct current from being applied to the liquid crystal panel 1, all the selective voltages are applied to the scanning electrodes Y1 to Y6 during a single frame F1 (Figures 13 and 14). Thereafter, during the next frame F2, the scanning electrodes are driven by a group of selective voltages which have undergone a polarity inversion.

Even if resistances of the scanning electrodes Y1 to Y6 are set ideally to zero, the resistances of the signal electrodes X1 to X6 and capacitances of the capacitors consisting of the display dot intersections in which the liquid crystal serves as a dielectric substance form a low-pass filter (Figure 12) the symbol R representing the resistance of each of the signal electrodes X1 to X6 and the symbol C representing the capacitance of each of the capacitors formed at the display dot intersections. The ground symbol represents each of the scanning electrodes having zero resistance. Attenuation takes place when a change of applied voltage E from positive to negative and vice versa with respect to the scanning electrodes (ground) takes place. Hence, the effective voltages between the signal electrodes and the scanning electrodes are reduced as more frequent changes take place. The display dots formed at the intersections of the signal electrode X2 (Figure 11) and the scanning electrodes Y1 to Y6 frequently change in state from above (Y1, X2) as follows : non-lighting, lighting, non-lighting, lighting, non-lighting and lighting. In this case, there is caused a larger attenuation than in the case where the display dots formed at the intersections of the signal electrode X4 and the scanning electrodes Y1 to Y6 change less frequently from above (Y1, X4) as follows : non-lighting, lighting, lighting, lighting, lighting and non-lighting. This is explained with reference to Figures 13(a)-13(c) and Figures 14(a)-14(c) which depict voltage waveforms during two successive frame periods F1 and F2. During the frame period F1, the voltages V0, V4, V5 and V3 are selective, non-selective, lighting and non-lighting voltages. During the period F2, the voltages V5, V1, V0 and V2 are selective, non-selective, lighting and non-lighting voltages. Figure 13(a) shows the voltage

waveform applied to the signal electrode X2 intersecting the scanning electrode Y4. Figure 13(b) shows the voltage waveform applied to the scanning electrode Y4. Figure 13(c) shows the differences between the voltage waveforms applied to the scanning electrode Y4 and the signal electrode X2 and thus across the display dot intersection of the electrodes Y4 and X2.

Similarly, Figure 14(a) shows the voltage waveform applied to the signal electrode X4 intersecting the scanning electrode Y4. Figure 14(b) shows the voltage waveform applied to the scanning electrode Y4. Figure 9(c) shows the differences between the voltage waveforms applied to the scanning electrode Y4 and the signal electrode X4 and thus across the display dot intersection of the electrodes Y4 and X4.

The hatched portions imply deficiencies to ideal voltage waveforms in Figures 13(c) and 14(c), and it can be seen that Figure 13(c) shows more deficiencies than Figure 14(c). Therefore, the display dot at the intersection of the signal electrode X2 and scanning electrode Y4 becomes very pale, whilst the display dot at the intersection of the signal electrode X4 and scanning electrode Y4 is only slightly pale.

The number of variations in the voltages between the respective signal and scanning electrodes can be made more or less uniform by the line inversion driving method discussed above, but sufficient uniformity cannot be achieved depending on the display content of the liquid crystal panel, which leads to unevenness of display.

It is an object of the present invention to provide a method of driving a high-definition liquid crystal display device without producing unevenness of display by compensating for attenuation caused when voltages change.

This invention is based on the discovery that display unevenness in a character or graphic pattern displayed on a liquid crystal panel, appears to be produced in conformity with the variations produced along the signal electrodes. Accordingly, there is provided a time during which selective voltage is not applied to any scanning electrode, and unevenness of display is eliminated by applying, to each of the signal electrodes, a compensating voltage having a magnitude based on these variations along the respective signal electrode.

According to one aspect of the invention, a method of driving a liquid crystal panel comprising a plurality of scanning electrodes on a substrate and a plurality of signal electrodes on another substrate, between which substrates a liquid crystal layer is sandwiched, comprises applying scanning electrode driving waveforms consisting of selective and non-selective voltages to the scanning electrodes of the liquid crystal panel ; applying lighting or non-lighting voltages to the plurality of signal electrodes ; and periodically inverting polarities of the lighting and non-lighting voltages with respect to the non-selective voltages thereby to drive the liquid crystal panel, characterised by providing a compensating period for which the selective voltage is not applied to any one of the plurality of scanning electrodes ; and, during the compensating period, applying a compensating voltage to each of the signal electrodes of the liquid crystal panel, each compensating voltage being in accordance with the number of variations in the polarities of the voltages applied to the respective signal electrode with respect to the non-selective voltages applied to the scanning electrodes during a constant period.

Impressed on the signal electrode is the compensating voltage having a combined magnitude and duration corresponding to the number of variations in the polarity of the voltage applied to the signal electrode with respect to the non-selective voltages applied to the scanning electrodes during the compensating time for which the selective voltage is not applied to any one of the plurality of scanning electrodes. This compensates for any difference between the effective voltages applied to the display dots on the signal electrodes.

It is therefore possible to provide a high definition display device.

How the present invention may be carried into effect will hereinafter be particularly described with reference to the accompanying drawings, in which :-

Figures 1(a) to 1(c) are voltage waveform diagrams illustrating a first example of a driving method according to the invention ;

Figure 2 is a diagram showing display contents and a configuration of a liquid crystal panel ;

Figures 3(a) to 3(c) are diagrams of voltage waveforms applied to a particular signal electrode and a particular scanning electrode in the first example.

Figures 4(a) to 4(c) are diagrams of voltage waveforms applied to another particular signal electrode and the particular scanning electrode in the first example ;

Figure 5 is a circuit diagram of an X electrode driver for the first example of driving method according to the invention ;

Figures 6 (a), 6 (b), 6 (c) and 6 (d) if placed together as indicated in Figure 6 show a timing chart of the operation of the circuit of Figure 5 ;

Figure 7 is a circuit diagram of a power regulator circuit for use with the driver of Figure 5 ;

Figure 8 is a circuit diagram of a Y electrode driver for use in conjunction with the driver of Figure 5 ;

Figure 9 is a circuit diagram of a D/$\overline{C}$ signal generator circuit for use with the driver of Figure 5 ;

Figures 10(a) to 10(c) are voltage waveform diagrams illustrating a second example of a driving

method according to the invention ;

Figure 11 is a diagram showing display contents and a configuration of a prior art liquid crystal panel ;

Figure 12 is a circuit diagram depicting an electric equivalent circuit of the liquid crystal panel ;

Figures 13(a) to 13(c) are diagrams of voltage waveforms applied to a particular signal electrode and a particular scanning electrode of the liquid crystal panel in a prior art driving method ; and

Figures 14(a) to 14(c) are diagrams of voltage waveforms applied to another particular signal electrode and the particular scanning electrode of the liquid crystal panel in the prior art driving method.

Examples of driving methods according to the invention will be described in relation to a liquid crystal panel 1 depicted in Figure 2. The liquid crystal panel 1 is constructed of a pair of substrates 2 and 3 between which a liquid crystal layer is sandwiched. Scanning electrodes Y1 to Y6 are formed on the substrate 2 in the lateral direction. Signal electrodes X1 to X6 are formed on the substrate 3 in the vertical direction. Display dots are intersections of the scanning electrodes Y1 to Y6 and the signal electrodes X1 to X6. The hatched display dots are to be lit up, while the other display dots are not to be so lit up. The liquid crystal panel 1 adopts a positive display mode in which the display dots are darkened with higher effective voltages impressed thereon. As shown, there are six scanning and six signal electrodes to simplify the explanation. In practice, a much larger number of electrodes would be provided on the liquid crystal panel. The configuration of this liquid crystal panel is the same as that of the prior art liquid crystal panel shown in Figure 6.

A first example of a driving method according to the invention is hereinafter described with reference to Figures 1 and 2. During a frame period F1, voltages V0, V5, V4 and V3 are selective, lighting, non-selective and non-lighting voltages of a first group. During a second frame period F2, voltages V5, V0, V1 and V2 are selective, lighting, non-selective and non-lighting voltages of a second group. The application of the first and second voltage groups is periodically changed over at arbitrarily chosen intervals. In this example, the period is set as the sum of a display period and a compensating time TC. The symbols T1 to T6 represent times during which the selective voltages of the first voltage group are applied to the respective scanning electrodes Y1 to Y6. The symbols t1 to t6 represent times during which the selective voltages of the second voltage group are applied to the respective scanning electrodes Y1 to Y6. The relationship between voltages is expressed as V = V0 - V1 = V1 - V2 = V3 - V4 = V4 - V5. Then (V0 - V5)/V is in the range 4 to 50.

Figure 1(a) shows a voltage waveform applied to the scanning electrode Y4. In the waveforms of the voltages impressed on the scanning electrodes Y1 to Y6, the selective voltage V0(V5) is applied to the scanning electrode Y1 during the time T1 (t1), while the non-selective voltage V4 (V1) is applied to other scanning electrodes Y2 to Y6. (The scanning electrode to which the selective voltage is applied is said to be selected. The scanning electrode to which the non-selective voltage is applied is said to be non-selected). During the subsequent times T2 (t2) to T6 (t6), the selection of the scanning electrode is also shifted from Y1 to Y2 to Y3 to Y4 to Y5 to Y6. During these times, the scanning electrodes other than that which is selected are non-selected. The times T1 to T6 represent the display period. During the subsequent compensating time TC (tc) none of the scanning electrodes Y1 to Y6 is selected and all are non-selected. After the compensating time TC (tc), a display period starting with time t1 (T1) occurs, during which a similar shifting is repeated. The times T1 (t1) to T6 (t6) are referred to as the display period and the time TC (tc) is referred to as the compensating time.

Figures 1(b) and 1(c) show voltage waveforms of signals applied to the signal electrodes X2 and X4, respectively, to achieve the display shown in Figure 2. The signal voltage waveforms become lighting voltages during lighting of the display dots at the intersections of the signal electrodes X1 to X6 and the selected scanning electrodes Y1 to Y6 for a certain time. The signal voltage waveforms then change to non-lighting voltages. Within the compensating time TC (tc), the lighting or non-lighting voltages are applied to the signal electrodes X1 to X6 for a time corresponding to the number of variations in the polarities of the voltages on the signal electrodes X1 to X6 with respect to the non-selective voltages for a constant period. The voltage (lighting or non-lighting voltage in this example) applied to the signal electrodes X1 to X6 is different from the non-selective voltages applied to the scanning electrodes Y1 to Y6 during the compensating time TC (tc). The time during which this different voltage is impressed is referred to as the application time. A compensating voltage is the product of the different voltage and the application time. The compensating time is divided into a number of equal time periods, the number being not less than the maximum number of variations of polarity. The application time is then equal to the product of the number of variations and the duration of one of the equal time periods. The constant period for which the number of variations is counted, may be an integral multiple of the sum of the compensating time and the pair of display times. In this example, the constant period is a frame period F1 to F2. However, no account is taken of changeovers from the lighting or non-lighting voltage to the non-lighting voltage or vice versa within and at the end of the compensating time TC (tc). More specifically, in the case of the signal electrode X2, the

number of variations in the polarity of the voltage on X2 with respect to the non-selective voltage is five. Hence, the lighting or non-lighting voltage is applied for a large part of the compensation time. In the case of the signal electrode X4, the number of variations in the polarity of the voltage on X4 with respect to the non-selective voltage is two. Hence, the lighting or non-lighting voltage is impressed for a small part of the compensation time. Note that in this embodiment, the application time is exactly proportional to the number of inversions in the polarity. The application time is not so limited but may be obtained by experiment in accordance with the number of variations.

The liquid crystal panel 1 is driven by the driving waveforms described above.

Figures 3(a) to 3(c) and 4(a) to 4(c) illustrate waveforms of the voltages actually impressed on the display dot intersections on the liquid crystal panel 1 of Figure 2.

Figure 3(a) depicts the voltage waveform on the signal electrode X2 at its intersection with the scanning electrode Y4 when applying the signal voltage waveform of Figure 1(b) to the signal electrode X2 of Figure 2.

Figure 3(b) shows the voltage waveform on the scanning electrode Y4 at its position of intersection with the signal electrode X2 when applying the scanning voltage waveform of Figure 1(a) to the scanning electrode Y4 of Figure 2. To simplify the explanation, it is assumed that there is no attenuation of the voltage waveform due to zero electric resistance of the scanning electrodes Y1 to Y6.

Figure 3(c) shows the differences between the waveforms of Figures 3(a) and 3(b). This is the waveform of voltage impressed on the display dot intersection X2/Y4.

Similarly, Figure 4(a) shows the voltage waveform on the signal electrode X4 at its intersection with the scanning electrode Y4 when applying the signal voltage waveform of Figure 1(c) to the signal electrode X4 of Figure 2.

Figure 4(b) illustrates the voltage waveform on the scanning electrode Y4 at its intersection with the signal electrode X4 when applying the scanning voltage waveform of Figure 1(a) to the scanning electrode Y4 of Figure 2. For descriptive simplicity, it is assumed that there is no attenuation of the voltage waveforms due to the zero electric resistance of the scanning electrodes Y1 to Y6.

Figure 4(c) shows the differences between the waveforms of Figures 4(a) and 4(b). This is the waveform of voltage impressed on the display dot intersection X4/Y4.

It will be seen from Figure 3(a) that the voltage on the signal electrode X2 often changes from the lighting voltage to the non-lighting voltage and vice versa during the display period and the attenuation increases. During compensating time TC, however, the lighting voltage is applied for five sixths of that time, giving a compensation voltage corresponding to the attenuation quantity. It is therefore possible substantially to compensate for the reduction in the effective voltages impressed on the display dots, caused by the attenuation of the voltages applied during the display period.

Similarly, as seen from Figure 4(a) there are less frequent changeovers of the voltage on the signal electrode X2 from the lighting voltage to the non-lighting voltage and vice versa during the display period. Less attenuation takes place. In this case, during the compensating time TC (tc), the lighting voltage is applied only for one third of the compensation time. This substantially compensates for the reduction in effective voltages impressed on the display dots, caused by the attenuation of the voltages applied during the display period.

As described above, unevenness of display can be substantially eliminated by increasing or decreasing the compensation voltage applied during the compensating time in accordance with the number of variations in the polarities of the voltages of the respective signal electrodes with respect to the non-selective voltages applied to the scanning electrodes during the display period.

An embodiment of X driver circuit for carrying out the method of the invention with six signal electrodes X1 to X6 is shown in Figure 5. An XSCL signal line is connected to operate shift registers S1-1 to S1-6 upon a fall of signal on the XSCL line. Data signals are fed to the shift register S1-1 and are shifted from shift register S1-1 to register S1-2 and so on, at each fall of XSCL signal. The output of each of the shift registers S1-1 to S1-6 is taken to the input of a corresponding latch of a first group of latches L1-1 to L1-6 and to one input of a corresponding one of six Exclusive OR circuits EX-1 to EX-6. An LP signal line is connected to operate the latches of the first group upon a fall of signal on the LP line. The XSCL signal comprises a set of six pulses during each of the individual display time periods T1 to T6, respectively. The LP signal comprises a similar pulse at the start of each such display time period and a set of seven pulses during the compensating time TC. Thus the XSCL and LP signals combined comprise a continuous series of pulses.

The output of each of the latches L1-1 to L1-6 of the first group is to the other input of the respective one of the Exclusive OR circuits EX-1 to EX-6. The latch circuits of the first group receive the output data from their corresponding shift registers upon the fall of the LP signal. Each Exclusive OR circuit compares the data output from its shift register and from its latch of the first group and provides a "1" output when they do not agree. The LP signal line is also connected to operate latches L2-1 to L2-6 of a second group so as to latch the output of their corresponding Exclusive OR circuits EX-1 to EX-6 upon a rise of the LP signal.

The latch circuits L2-1 to L2-6 of the second group also have a pre-set function provided by an input from a D/$\overline{C}$ signal line which carries a "1" signal during the display period and not during the compensating time. This pre-set function ensures that the latch circuits of the second group output a "1" signal unconditionally whenever the D/$\overline{C}$ signal is "0", that is during the compensating time. The output of each of the latches L2-1 to L2-6 of the second group is taken to an enable input of a corresponding one of six counter circuits CNT-1 to CNT-6. The D/$\overline{C}$ signal line is connected to an up/not down (U/$\overline{D}$) input of each of the counters CNT-1 to CNT-6. When the U/$\overline{D}$ input is "1" during the display period, and the latch circuit of the second group provides a "1" signal to the E input at the rise of the LP signal, the counter circuit acts as an incremental counter and adds +1. During the compensating time the D/$\overline{C}$ signal is down and the U/$\overline{D}$ input is "0", so that the counter circuit acts as a decremental counter and adds -1 upon the fall of the LP signal. When the input E to the counter circuit is "0", there is no change in the counter circuit. Control of this timing is achieved by connecting the LP signal line to the counter circuits CNT-1 to CNT-6 through an AND circuit AN whose other input is the inverse of the DOUT signal line. The DOUT signal is up during the last part of the display period before compensating time, corresponding to the display time T6. This masks the LP signal from the counter circuits CNT-1 to CNT-6 just before compensating time.

The data in each counter is output to a corresponding one of six OR circuits OR-1 to OR-6 which pass on the data to one input of a corresponding one of six selector circuits SEL-1 to SEL-6. The other input of each selector circuit is taken from the output of the corresponding latch of the first group L1-1 to L1-6. The D/$\overline{C}$ signal line is connected to each selector circuit so that each of the latter gives an output which is that of the latch of the first group when D/$\overline{C}$ signal is "1" (display period) and which is that of the contents of the counter circuit through the OR circuit when D/$\overline{C}$ signal is "0" (compensating time). The output of each of the selector circuits SEL-1 to SEL-6 is taken to a corresponding one of six analog switches SW1 to SW6. These receive "1" and "0" inputs of lighting voltage V0 or V5 and non-lighting voltage V2 or V3, respectively. According to the output of the corresponding selector circuit, the lighting or non-lighting voltage is passed on to the corresponding X electrode.

Selection of lighting and non-lighting voltages is by means of a frame signal FR applied to two analog switches SW7 and SW8. These two switches receive as inputs, the lighting voltages V0 and V5, and the non-lighting voltages V2 and V3, respectively. When the FR signal is "0", the lighting voltage V5 and the non-lighting voltage V3 are chosen for connection to the switches SW1 to SW6. When the FR signal is "1", the voltages are V0 and V2.

The timing chart of Figure 6 illustrates the operation of the driver circuits. When the D/$\overline{C}$ signal is "1" during the display period, shift registers S1-1 to S1-6 receive data concerning the following selected dot on the scanning electrode at the trailing edge of the XSCL signal. The Exclusive OR circuits analyse whether the data in the shift registers and latches of the first group correspond and transmit resultant data to the latches of the second group at the leading edge of the LP signal. The latches of the first group receive data from the corresponding shift registers at the trailing edge of the LP signal. At the same time, the counter circuits count up +1 if their corresponding latches of the second group output "1". This is repeated throughout the display period when the D/$\overline{C}$ signal is "1". Thus, each counter circuit counts how frequently the voltage applied to the corresponding X electrode changes from lighting to non-lighting.

When the D/$\overline{C}$ signal is "0" during the compensating time, each counter circuit acts as a decremental counter and adds -1 at the trailing edge of the LP signal. The OR circuits repeatedly output "1" until the corresponding count is "0" in the counter. Thus, the higher the number of counts in a counter cirucuit (arising from the number of changes between lighting and non-lighting voltages) the longer the OR circuit outputs "1", thus controlling the duration of the compensating voltage during the compensation time. The compensation voltage is either V0 or V5 depending upon the level of the frame signal FR. When the output data from the OR circuit is "0", the voltage applied to the X electrode is either V2 or V3, but these are modified during the compensating-time by means of the circuit shown in Figure 7.

The input voltages V2 and V3 in Figure 5 are derived from switches SW9 and SW10, respectively. The switch SW9 is controlled by the D/$\overline{C}$ signal to connect a V1 supply to the V2 terminal when D/$\overline{C}$ is "0" (compensating time) and a V2 supply to the V2 terminal when D/$\overline{C}$ is "1" (display period). In similar manner, the switch SW10 connects a V4 supply to the V3 terminal when D/$\overline{C}$ is "0" and a V3 supply when the D/$\overline{C}$ is "1".

The X driver circuit outputs the same voltage waveform as the conventional one during the display period. During compensating time, the lighting voltage is applied for a longer time to the signal electrode which has more frequently changed from lighting to non-lighting voltage during the display period then to a signal electrode which has not changed so frequently.

The AND circuit AN corrects the term of the compensating time. Without it, the last LP signal before the compensating time would reduce the count in each of the counters by one and shorten the compensating voltage duration.

An embodiment of Y driver circuit for use with the

X driver circuit of Figure 5 is shown in Figure 8. The LP signal line is connected to operate shift registers S2-1 to S2-6 upon a fall of signal on the LP line. A DIN signal which defines the start of each frame is input to the shift register S2-1 and shifted to the next register upon the fall of each LP signal. The output of the last shift register S2-6 is the DOUT signal. Each of the shift registers S2-1 to S2-6 is connected to a corresponding one of six analog switches SW11 to SW16 and thus selects either selective voltage V5 or V0 or non-selective voltage V1 or V4 for application to the corresponding Y electrode. The frame signal FR is used to control analog switches SW17 and SW18 so that the selection of voltages V5 and V1 or V0 and V4 may be made

The D/$\overline{C}$ signal is derived from a circuit shown in Figure 9. The signal DIN is applied to a flip flop circuit F to set the flip flop to "1". The signal DOUT re-sets the flip flop to "0". The flip flop output D/C-1 is applied to a D flip flop circuit DF which is controlled by the trailing edge of the LP signal. The DIN signal at the start of a frame sets the flip flop F to provide a D/C-1 signal of "1". An LP signal for the first part T1 of the display period falls and the D flip flop circuit DF outputs a D/$\overline{C}$ signal of "1" which continues until both the D/C-1 signal and the LP signal have fallen. The D/C-1 signal falls when the flip flop F is re-set by the DOUT signal at the start of the last part T6 of the display period starts. The LP signal falls again at the start of the compensating time. Thus D/$\overline{C}$ signal from the D flip flop circuit DF falls at the start of the compensating time.

The voltages impressed on the signal electrodes X1 to X6 during the compensating time TC (tc) are the lighting or non-lighting voltages. This is intended to restrict the number of voltages supplied to the liquid crystal panel 1. If necessary, however, these may be replaced by an arbitrary voltage giving the same compensation voltage, being the product of the arbitrary voltage and the application time. The voltage waveform is rectangular in this example but may assume other arbitrary shapes. The compensating time TC may also be increased or decreased as the necessity arises.

The present invention is also applicable to a driving method which uses the line inversion driving method by which the polarities are inverted more often than once per frame period. The line inversion driving method in the second example (Figure 10) is such that the first and second voltage groups are changed over thrice per frame period, that is every time two of the scanning electrodes have been selected. Figure 10(a) illustrates the waveform of a signal voltage applied to the signal electrode X2 of Figure 2. Figure 10(b) depicts the waveform of a voltage applied to the scanning electrode Y4 of Figure 2. Figure 10(c) shows the differences between the waveforms of Figures 10(a) and 10(b) with dotted lines showing attenuation, and the actual waveform of voltage applied to the display dot intersection X2/Y4 by solid lines.

As will be seen in Figure 10(a), the voltage applied to signal electrode X2 during time T2 is V5, the lighting voltage of the first group. On passsing into time t/3, the voltage changes to V2, the non-lighting voltage of the second group. Simultaneously, the non-selective voltage V4 applied to scanning electrode Y4 (Figure 10(b)) changes to the non-selective voltage V1 of the second group. Thus there is no variation in the polarity of the voltage on the signal electrode with respect to the non-selective voltage on the scanning electrode. On passing from time t4, during which lighting voltage VO of the second group is applied, to time T5, the voltage applied changes to V3, the non-lighting voltage of the first group. Simultaneously the non-selective voltage changes from V1 of the second group to V4 of the first group. Thus, again there is no such variation. In similar fashion, passing from time t2 to T3 and from T4 to t5 produces no variation. Thus, as seen in Figure 10(c), there are only three polarity changes during the frame period under such line inversion driving conditions. This is to be compared with the position illustrated in Figure 3, where there are five such polarity changes. Thus the requirement for compensation is reduced and the different voltage is applied during the application time of one half of compensation time Tc or tc. As indicated by the solid line of Figure 10(c), the voltages actually applied to the display dots undergo attenuation three times within the display period during the constant period F1 or F2. The compensating voltage corresponding to the attenuation is applied during the compensating times Tc and tc, thereby substantially compensating for the reduction in the effective voltage of the display dot. Thus, unevenness of display can be removed even when employing the line inversion driving method.

For the inverse driving method, it is necessary to change the voltages more frequently than once per frame. Accordingly a new FR signal is derived which changes switches SW7, SW8, SW17 and SW18 more frequently than once per frame, in the disclosed method, three times during the six part display period. The changes of voltage are synchronised with the LP signal, but not during the compensating time. A circuit detects the change of FR signal and indicates this by means of a signal DET. One of an additional six Exclusive OR circuits then receives the output of each Exclusive OR circuit EX-1 to EX-6 and compares this with the signal DET, sending on the result to the latch of the second group. Thus a correct count of voltage changes to be compensated is made.

Although the illustrative embodiments of the present invention have been described in detail with reference to the accompanying drawings, it is to be understood that the present invention is not limited to those embodiments. Various changes or modifications may be effected therein by one skilled in the

art without departing from the scope of the invention claimed.

Claims

1. A method of driving a liquid crystal panel (1), comprising a plurality of scanning electrodes (Y) on a substrate (2) and a plurality of signal electrodes (X) on another substrate (3) between which substrates a liquid crystal layer is sandwiched, the method comprising applying scanning electrode driving waveforms consisting of selective (VO, V5) and non-selective voltages (V4, V1) to the scanning electrodes (Y) of the liquid crystal panel (1), applying lighting (V5,VO) or non-lighting voltages (V3,V2) to the plurality of signal electrodes (X) ; and periodically inverting polarities of the lighting and non-lighting voltages with respect to the non-selective voltages thereby to drive the liquid crystal panel, characterised by providing a compensating period (TC) during which the selective voltage is not applied to any one of the plurality of scanning electrodes (Y) and, during the compensating period, applying a compensating voltage to each of the signal electrodes (X) of the liquid crystal panel 1, each compensating voltage being in accordance with the number of variations in the polarities of voltages applied to a respective signal electrode (X) with respect to the non-selective voltages applied to the scanning electrodes (Y) during a constant period.

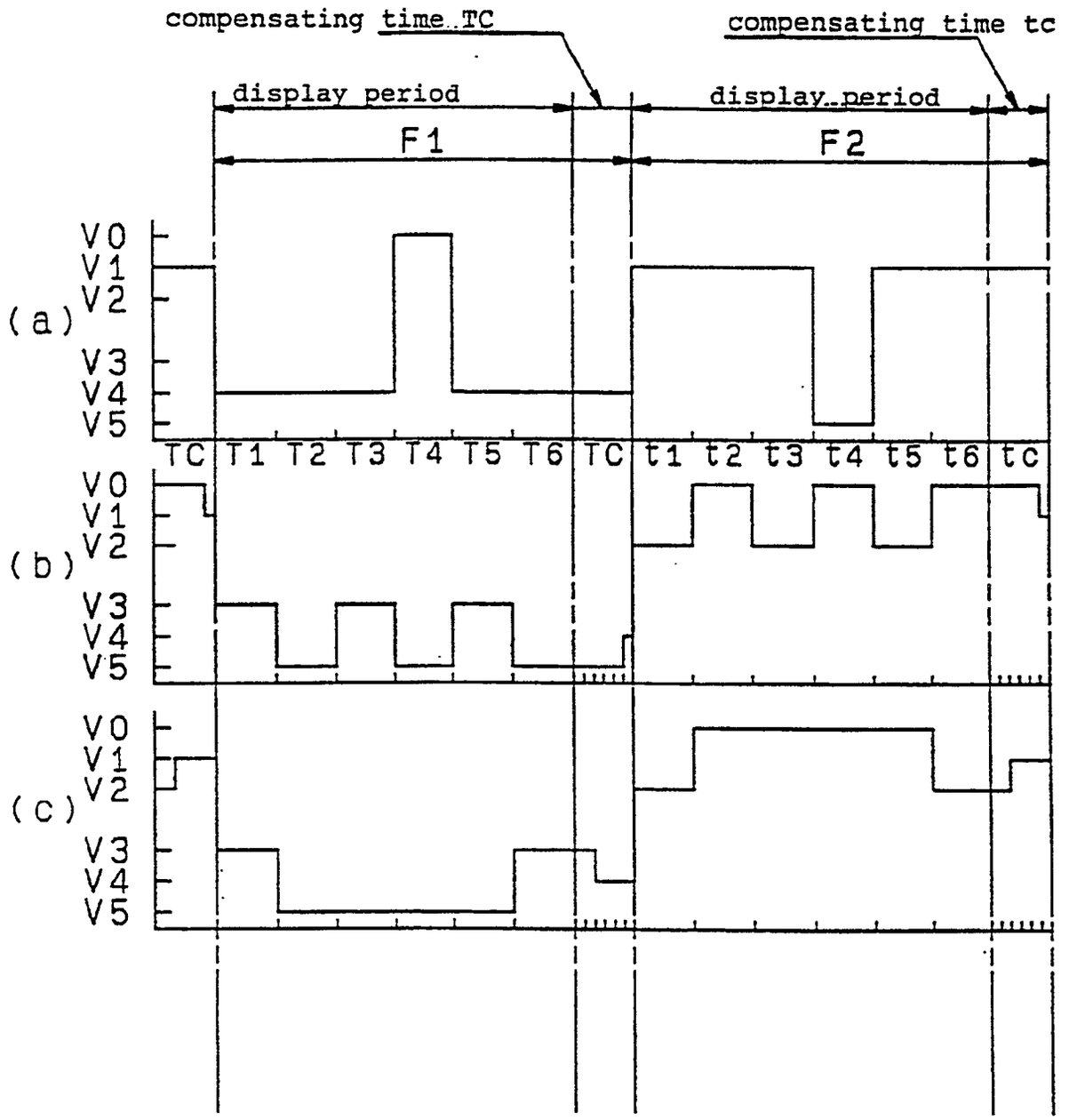
2. A method as claimed in claim 1, characterised in that the constant period is a display period forming part of a frame period (F1, F2) which also includes compensating time (TC, tc).

3. A method as claimed in claim 1 or 2, characterised in that periodic inversion occurs at the beginning of each display period.

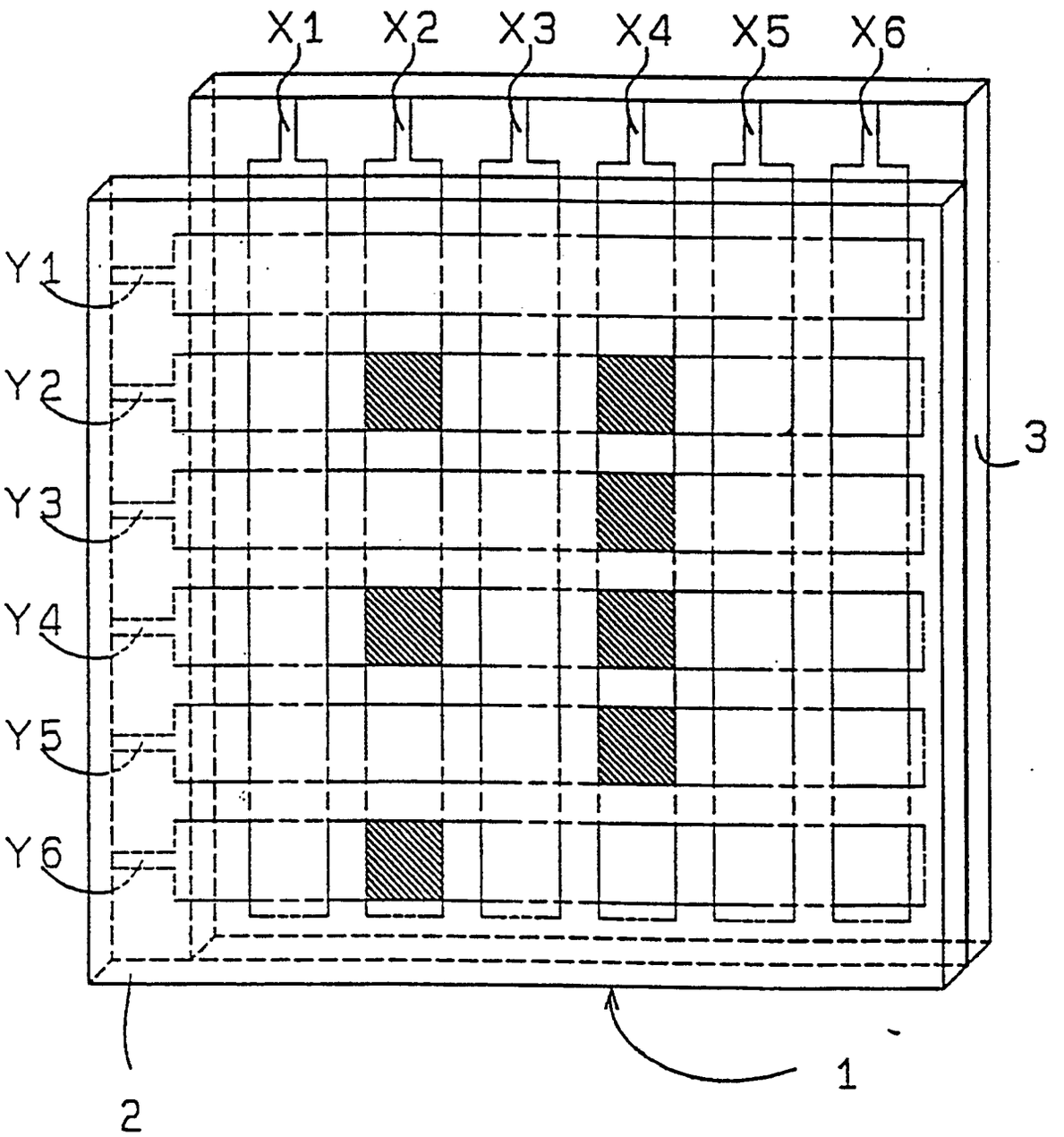
4. A method as claimed in claim 1 or 2, characterised in that periodic inversion occurs a plurality of times during each display period (Figure 5).

5. A method as claimed in any preceding claim, characterised in that the lighting or non-lighting voltage being applied to the signal electrode (X) at the end of the display period continues to be applied during compensating time for a time proportional to the number of said variations.

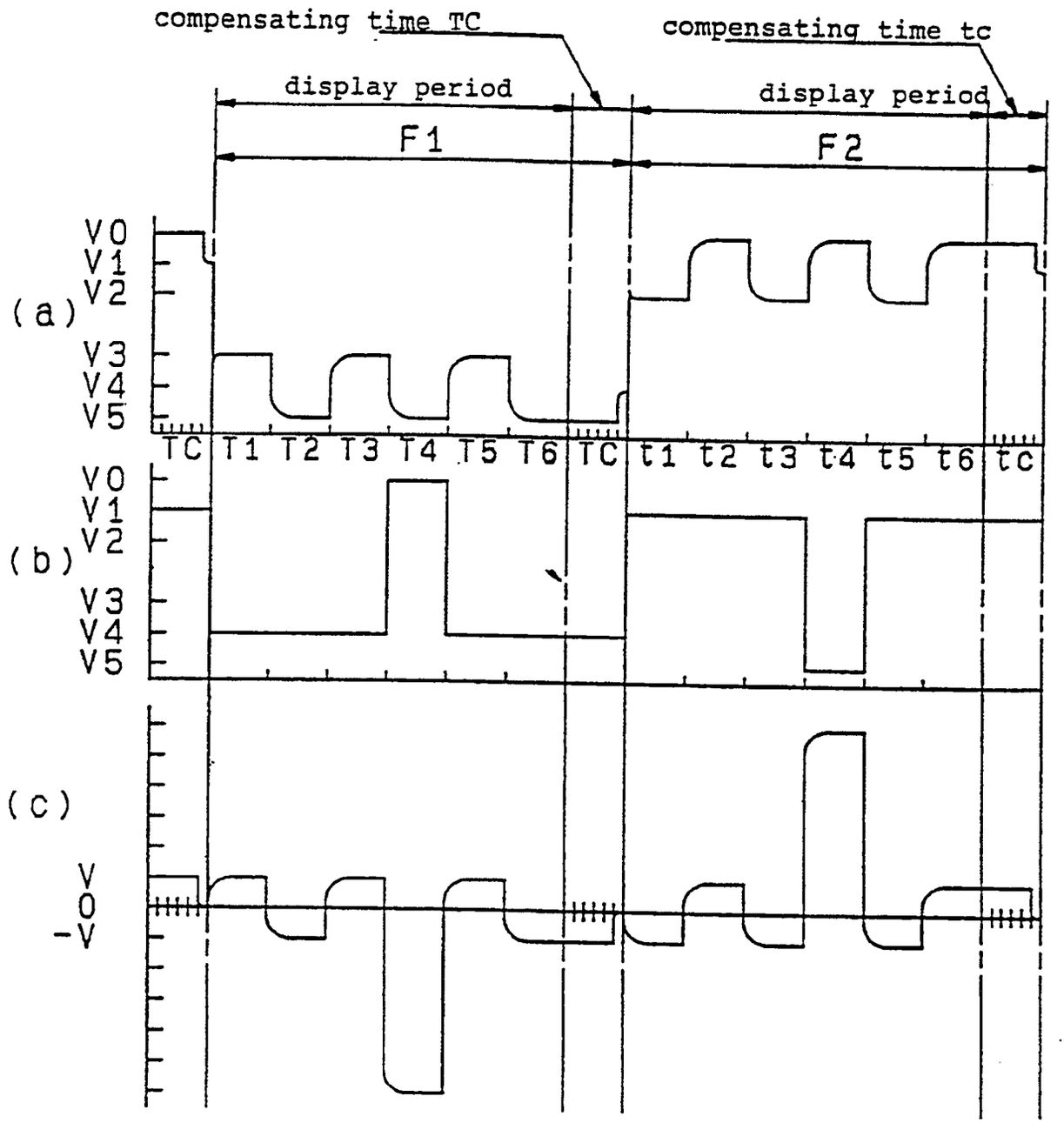
6. Means for carrying into effect the method according to any of the preceding claims.


compensating time TC
compensating time tc
display period
display period
F1
F2
(a)
(b)
(c)
V0
V1
V2
V3
V4
V5
TC T1 T2 T3 T4 T5 T6 TC t1 t2 t3 t4 t5 t6 tc

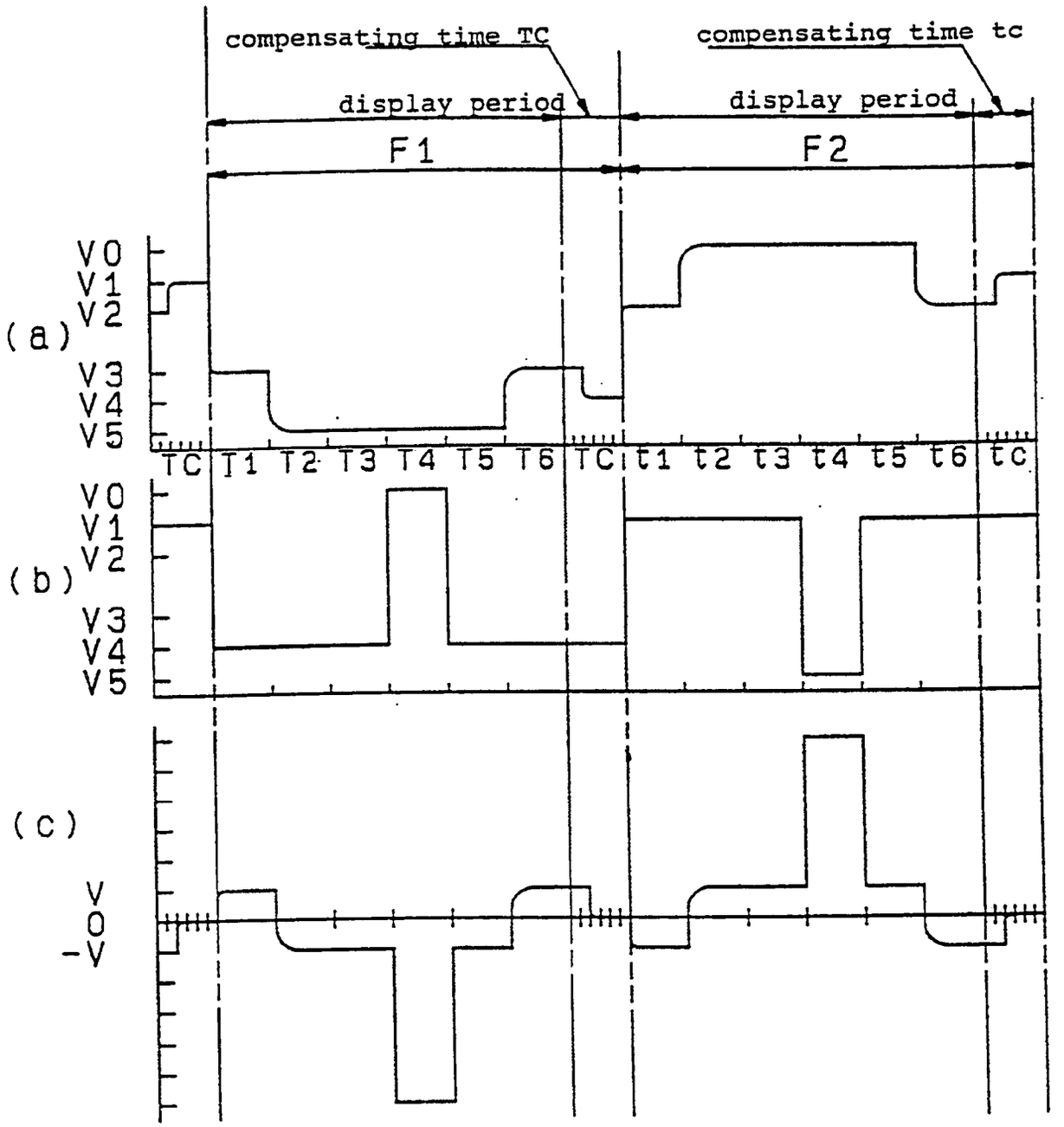
F I G. 1



F I G. 2


compensating time TC
compensating time tc
display period
display period
F1
F2
(a)
V0
V1
V2
V3
V4
V5
TC T1 T2 T3 T4 T5 T6 TC t1 t2 t3 t4 t5 t6 tc
(b)
V0
V1
V2
V3
V4
V5
(c)
V
0
-V

F I G. 3


compensating time TC
compensating time tc
display period
display period
F1
F2
(a)
V0
V1
V2
V3
V4
V5
TC T1 T2 T3 T4 T5 T6 TC t1 t2 t3 t4 t5 t6 tc
(b)
V0
V1
V2
V3
V4
V5
(c)
V
0
-V

F I G. 4

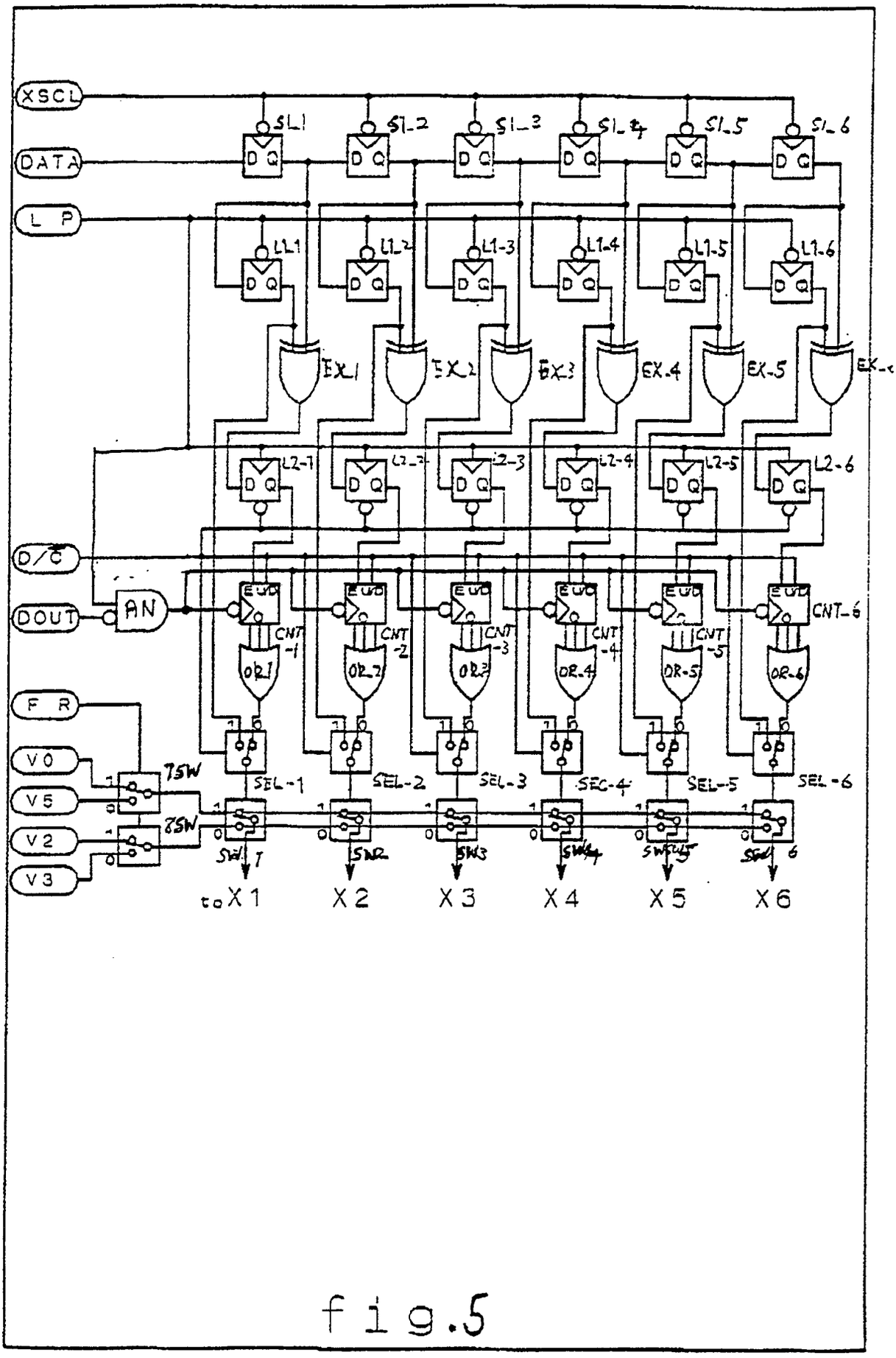

XSCL
DATA
L P
D/C
DOUT
F R
V0
V5
V2
V3
AN
SL1
SL2
SL3
SL4
SL5
SL6
L1-1
L1-2
L1-3
L1-4
L1-5
L1-6
L2-1
L2-2
L2-3
L2-4
L2-5
L2-6
EX-1
EX-2
EX-3
EX-4
EX-5
CNT-1
CNT-2
CNT-3
CNT-4
CNT-5
CNT-6
OR-1
OR-2
OR-3
OR-4
OR-5
OR-6
SEL-1
SEL-2
SEL-3
SEC-4
SEL-5
SEL-6
TSW
BSW
SW1
SW2
SW3
SW4
SW5
SW6
toX1
X2
X3
X4
X5
X6

fig.5

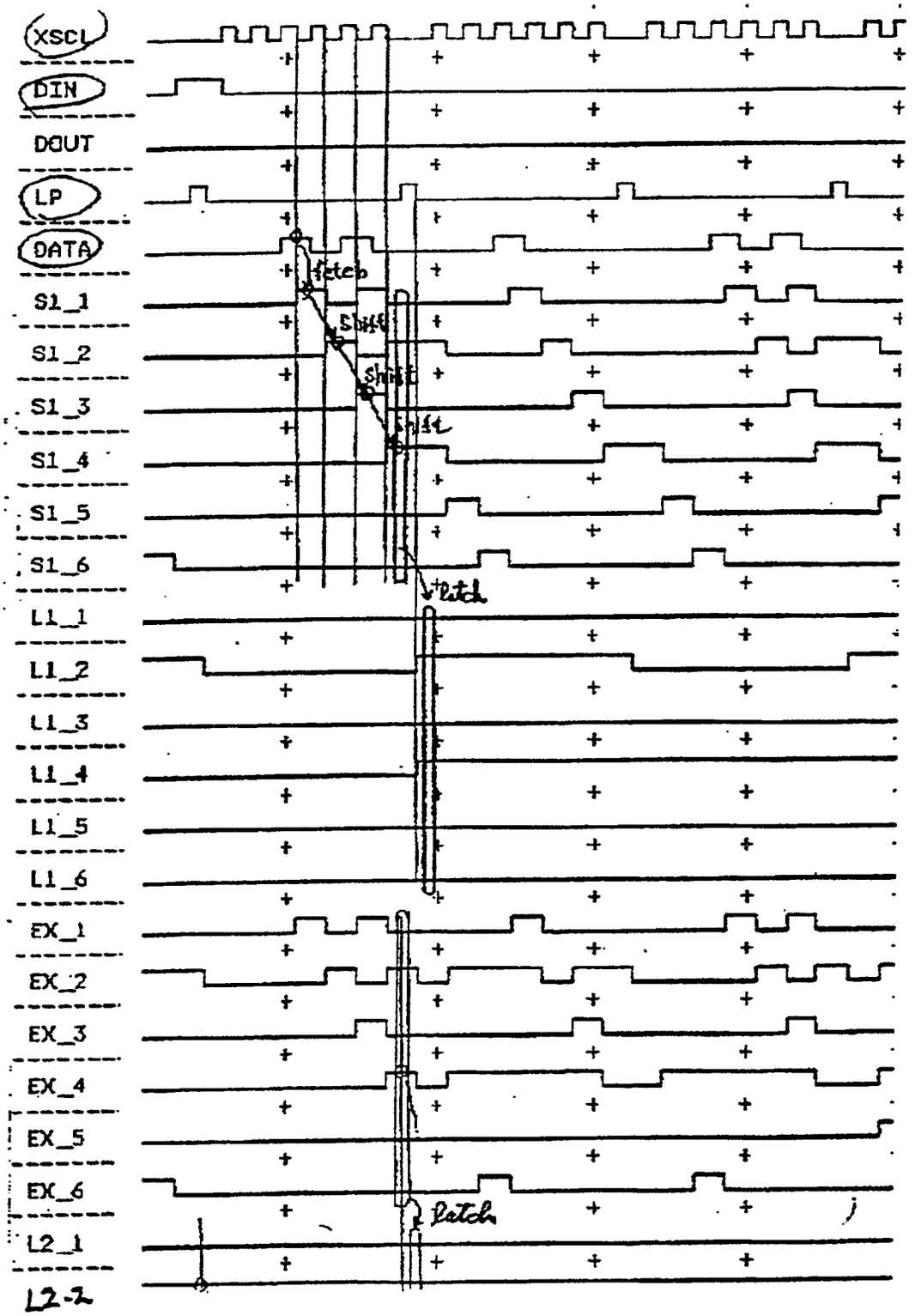


FIG. 6A

FIG. 6

A	B
C	D

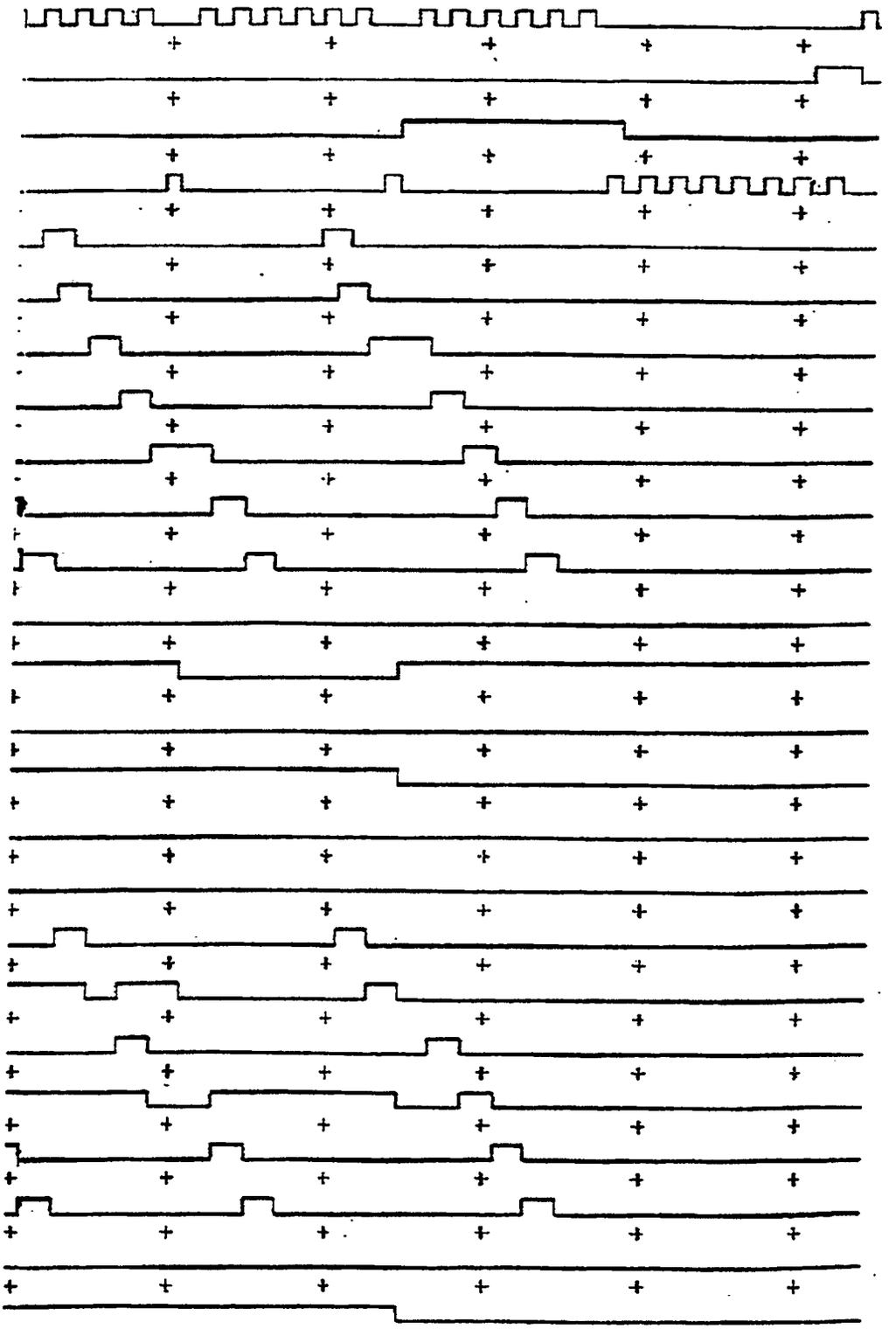


FIG. 6B

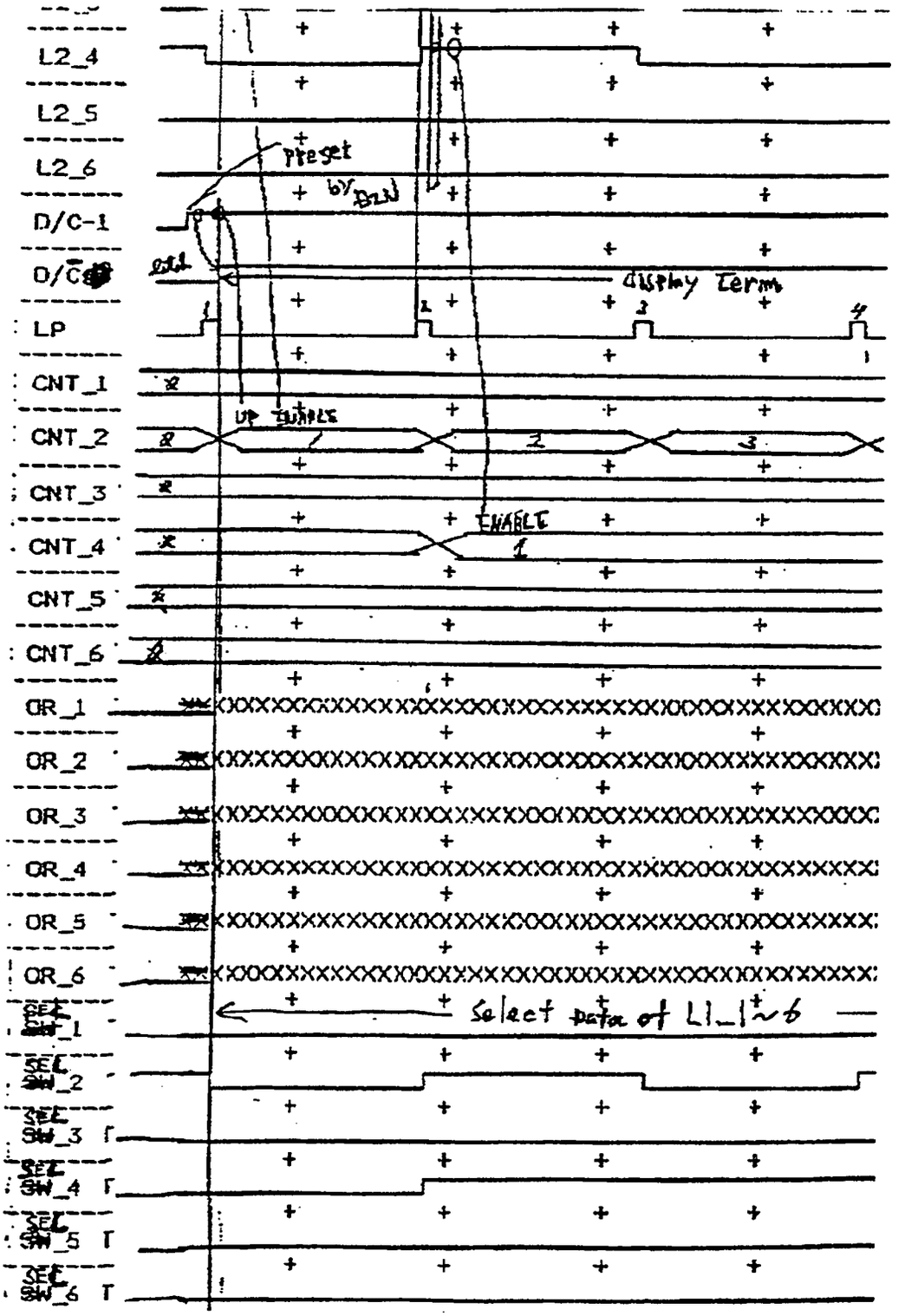

L2_4
L2_5
L2_6
D/C-1
D/C
LP
CNT_1
CNT_2
CNT_3
CNT_4
CNT_5
CNT_6
OR_1
OR_2
OR_3
OR_4
OR_5
OR_6
SEL SW_1
SEL SW_2
SEL SW_3
SEL SW_4
SEL SW_5
SEL SW_6
preset
display term
ENABLE
Select data of L1_1~6

FIG. 6C

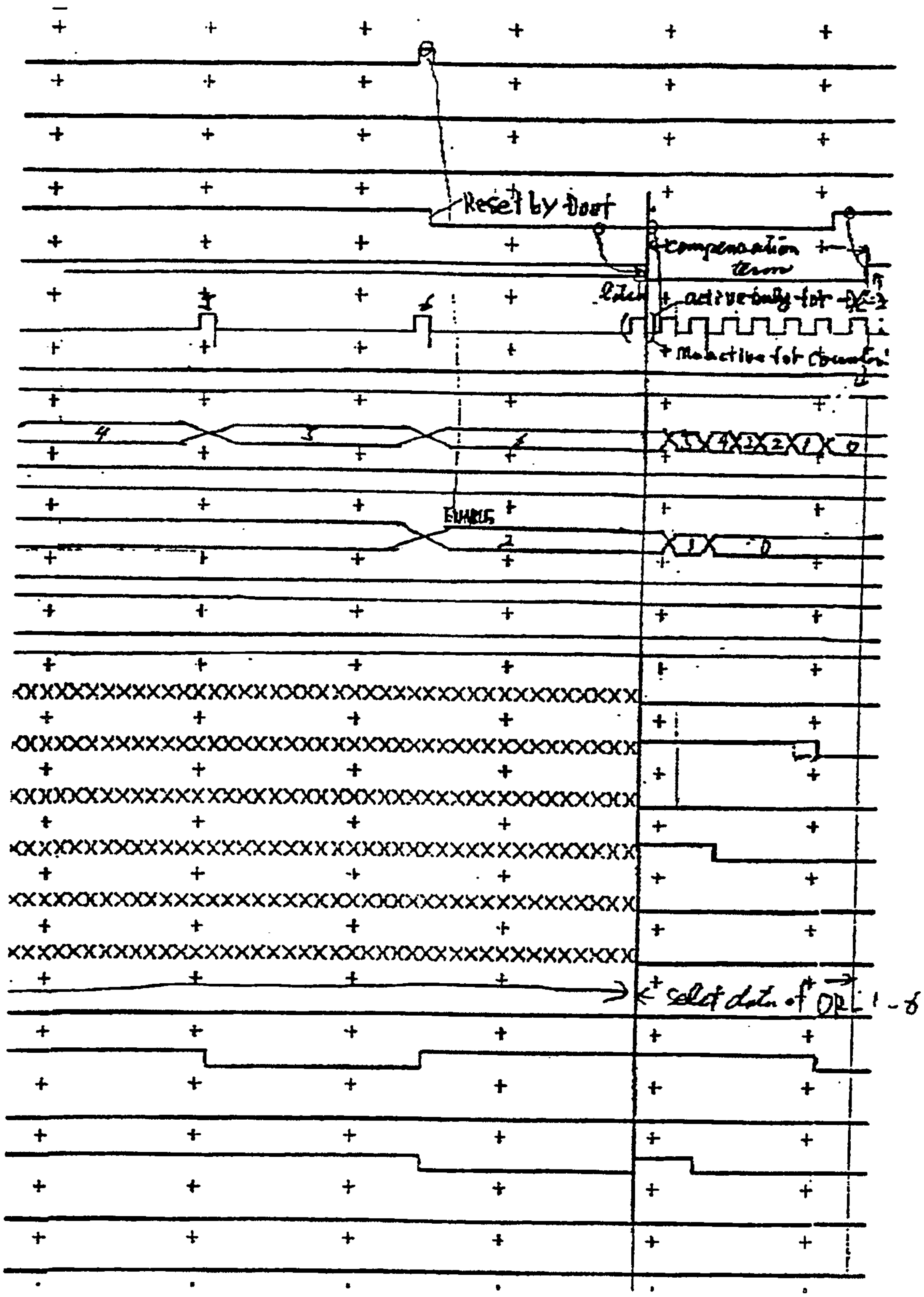

Reset by Dout
compensation term
active only for
select data of

FIG. 6D

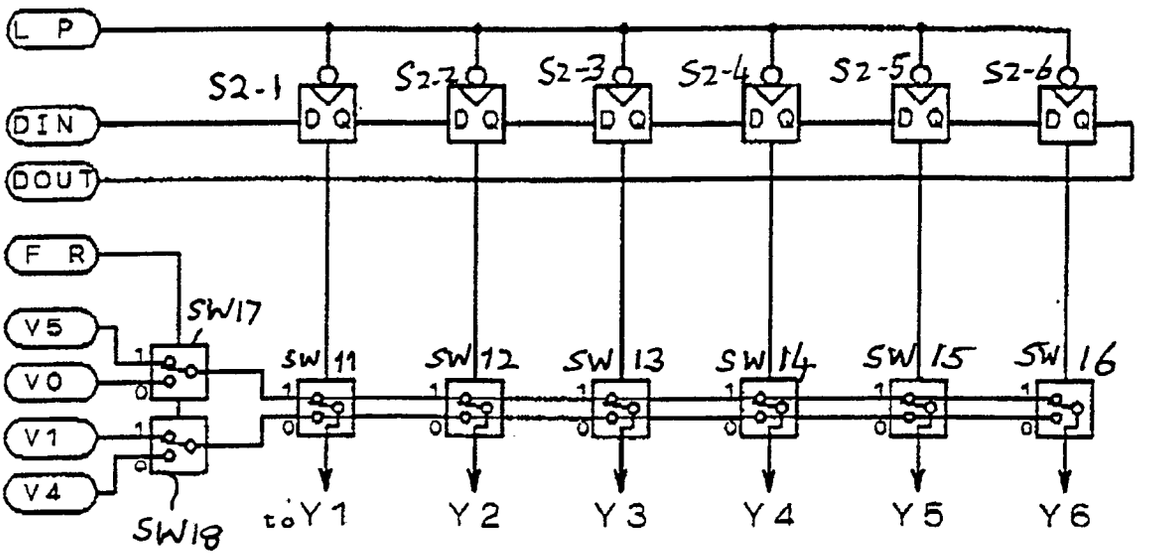


Fig.8

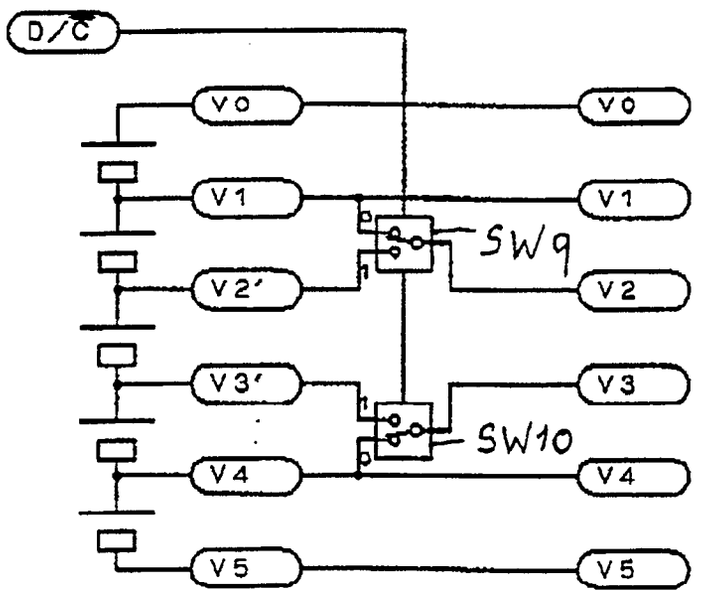


Fig.7

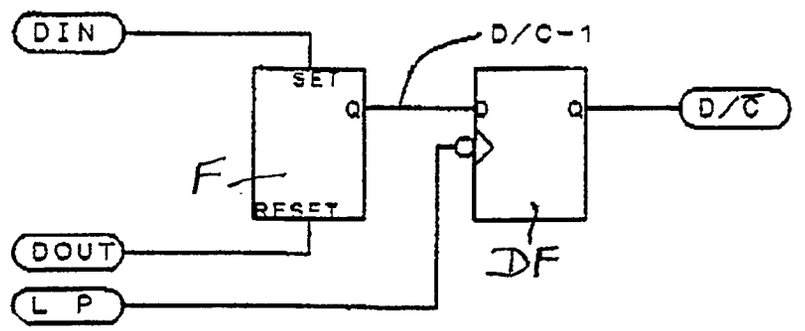


fig. 9

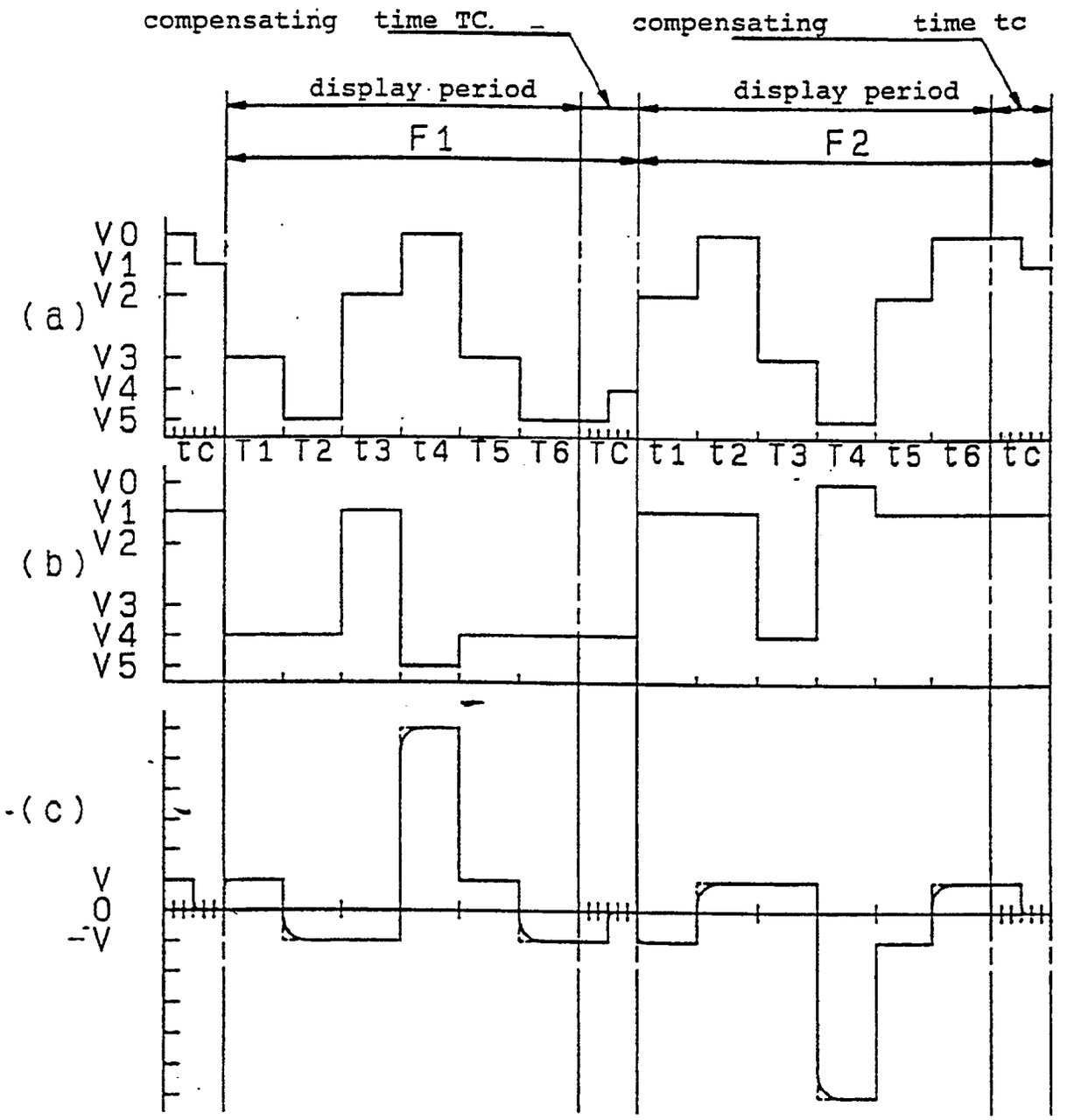

compensating time TC
compensating time tc
display period
display period
F1
F2
(a)
V0
V1
V2
V3
V4
V5
tc T1 T2 t3 t4 T5 T6 TC t1 t2 T3 T4 t5 t6 tc
(b)
V0
V1
V2
V3
V4
V5
(c)
V
0
-V

FIG. 10

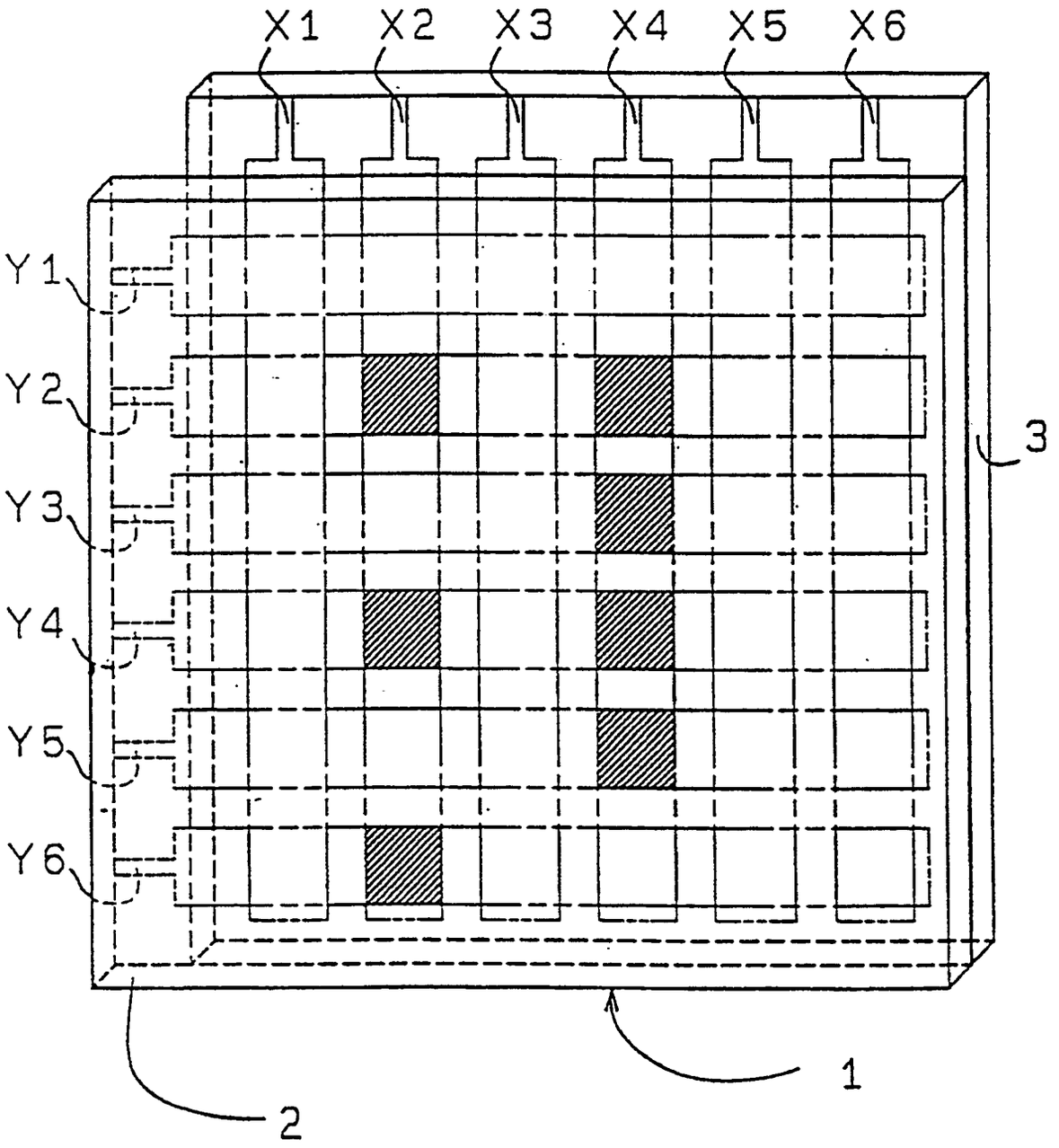


FIG. 11

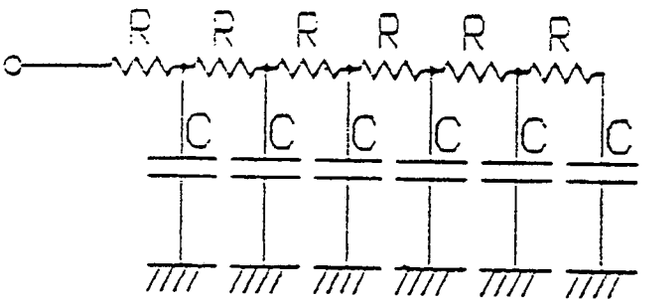


FIG. 12

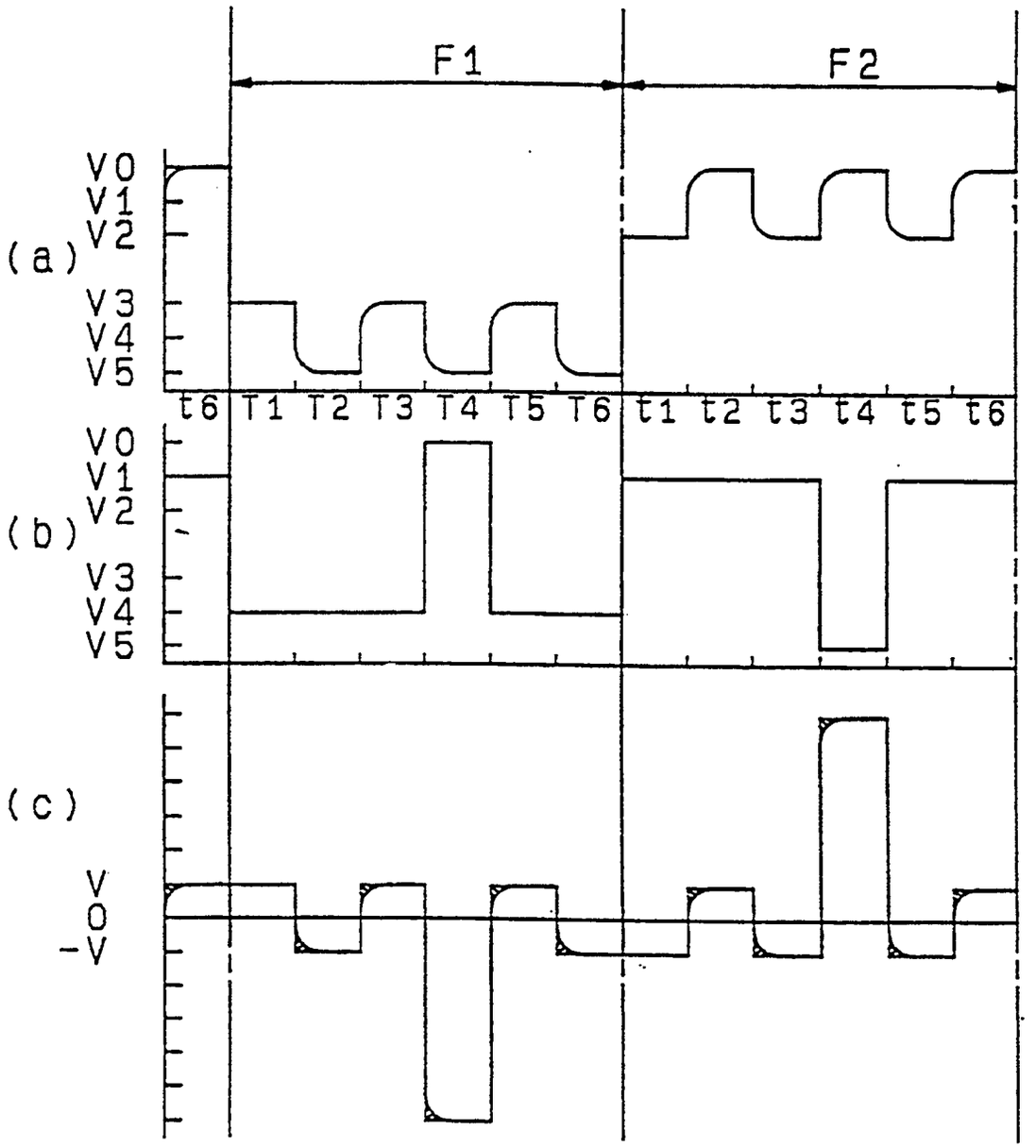

F1
F2
(a)
V0
V1
V2
V3
V4
V5
t6 T1 T2 T3 T4 T5 T6 t1 t2 t3 t4 t5 t6
(b)
V0
V1
V2
V3
V4
V5
(c)
V
0
-V

FIG. 13

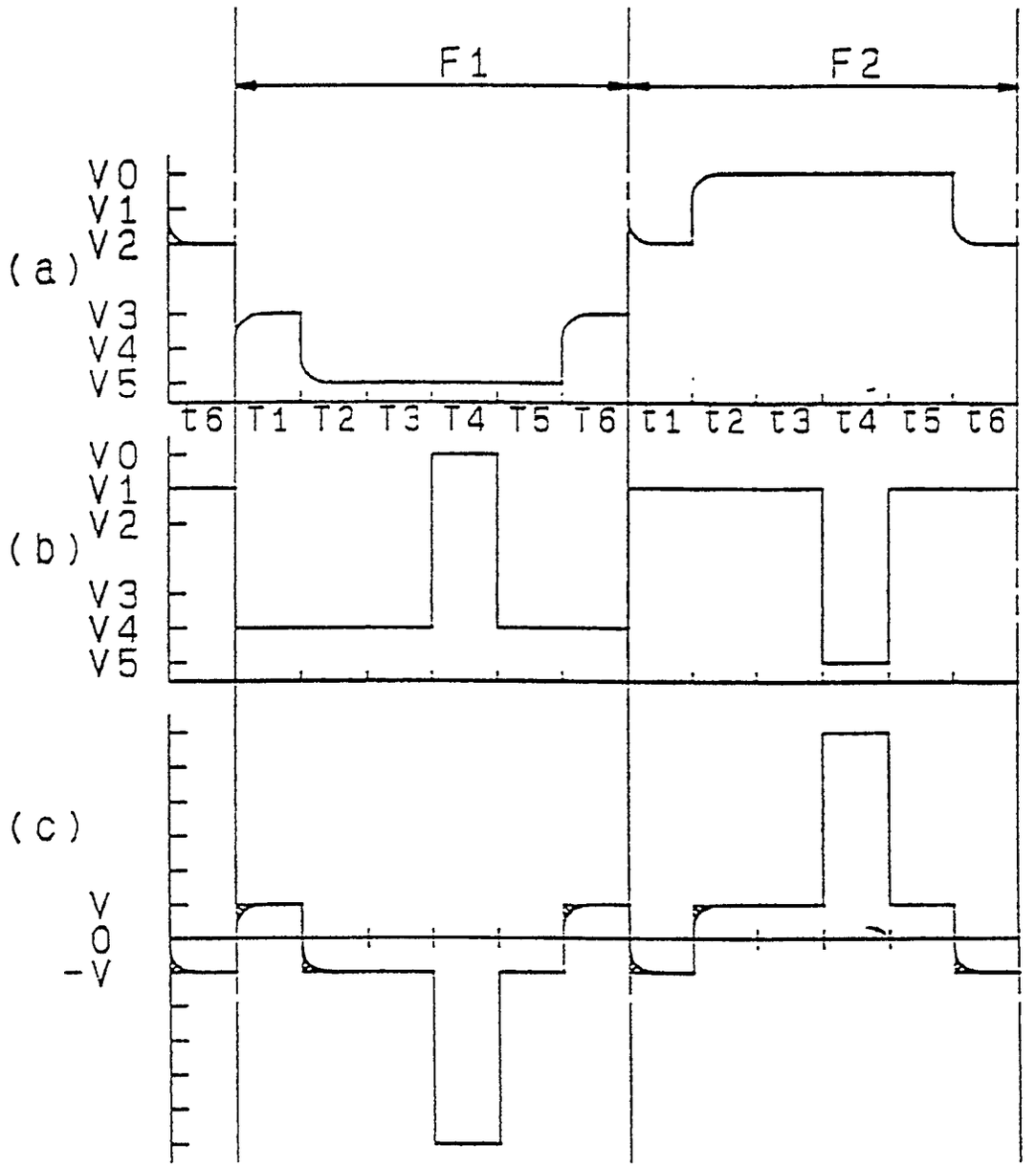

F1
F2
(a)
V0
V1
V2
V3
V4
V5
t6 T1 T2 T3 T4 T5 T6 t1 t2 t3 t4 t5 t6
(b)
V0
V1
V2
V3
V4
V5
(c)
V
0
-V

FIG. 14