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(54) System and method for transferring data.

(57) Organ pedal switches (14) have states determined by the position of the pedals. These switch states are sensed in a peripheral unit (12) through a switch matrix that generates a transmission signal provided by a serially encoded data stream having a sync pulse. Power to the peripheral unit, which is physically isolated from a host unit (16), is provided through magnetically coupled respective primary (34) and secondary (20) windings. Further, clock signals for the peripheral and host units are provided by a power oscillator (30) that drives the primary or tank coil of the oscillator in the host unit. Thus, power and clock signals are transmitted via the coupled windings from the host unit to the peripheral unit and data in one embodiment is relayed back to the host unit through infrared emissions. Alternatively, data is transferred bach through the coupled coils by loading the power oscillating circuit of the host unit during generation of data pulses by the data encoder (26) of the peripheral unit. The host unit then detects the transmitted data, determines whether it is different from previously received data for the same switch, and transfers to a CPU (18) only data that is new. The host unit stores an image of the data stream corresponding to an image stored in the CPU. The clock frequency derived from the power oscillator in the host unit is independent of the frequency of operation of the CPU.

EP 0 441 492 A2

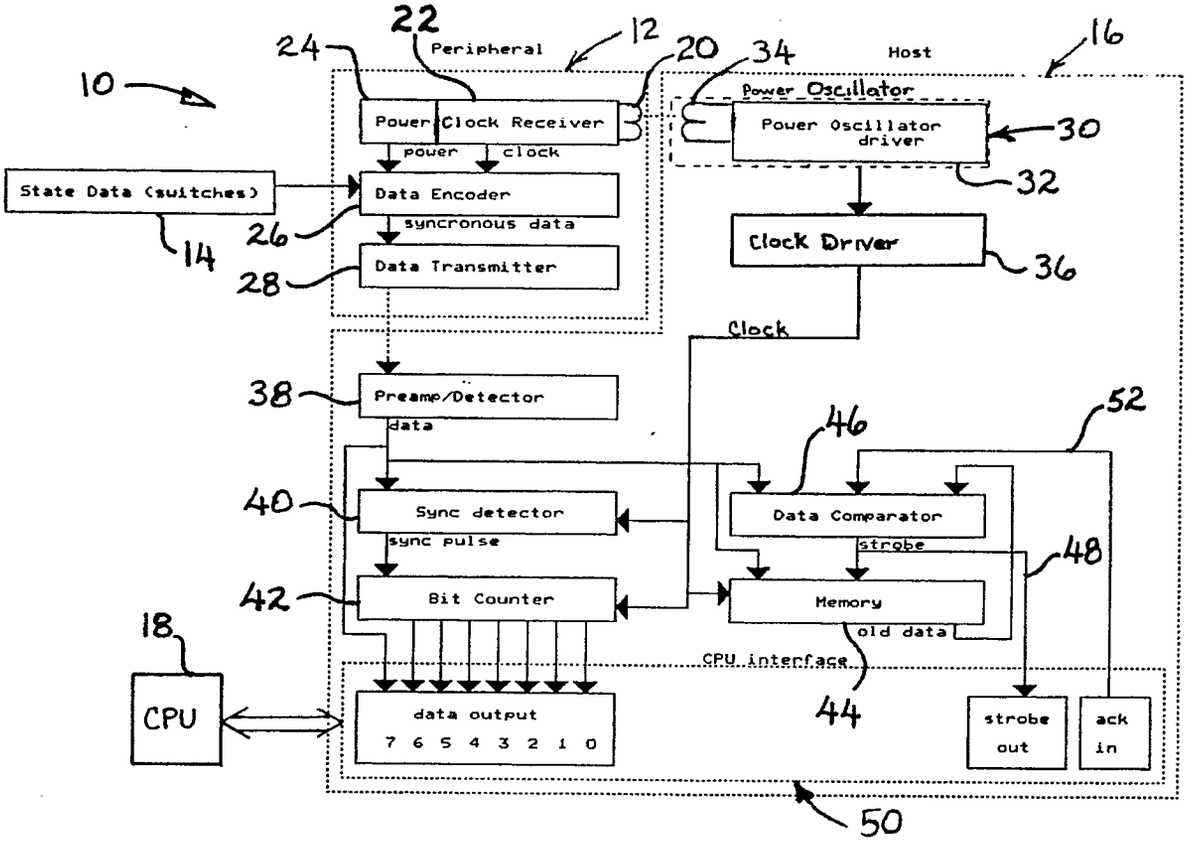
10
22
Peripheral
12
24
20
34
Host
16
Power_Oscillator
Power
Clock Receiver
Power Oscillator driver
30
power
clock
State Data (switches)
Data Encoder
32
14
26
syncronous data
Clock Driver
36
28
Data Transmitter
Clock
38
Preamp/Detector
data
46
52
40
Sync detector
Data Comparator
sync pulse
strobe
48
42
Bit Counter
Memory
18
old data
CPU interface
CPU
data output
7 6 5 4 3 2 1 0
44
strobe out
ack in
50

FIG. 1

SYSTEM AND METHOD FOR TRANSFERRING DATA

FIELD OF THE INVENTION

This invention relates to a system for transferring data between two physically separated locations, and more particularly, to such a system in which data is transferred by encoding a current in a transformer winding that induces a correspondingly encoded current in a magnetically coupled winding.

BACKGROUND AND SUMMARY OF THE INVENTION

The preferred embodiment of the present invention is directed to coupling signals between a panel of foot pedals associated with a music organ with a main or host processing unit which develops audio signals based on the foot pedals selected. However, it will be understood that the present invention provides for the transfer of data between physically separated locations, such as would be useful for coupling any peripheral device to a main or central unit that performs some function on the device received from the peripheral unit.

Traditionally, the foot-pedal panels of organs have been connected to the main organ through cable or other physical connections. More recently, reed switches have been installed in the cabinet of the organ with a magnet located in the foot pedals. When a pedal is pressed, the associated magnet activates the reed switch, thereby producing a corresponding signal in the main processing unit. The use of magnets and reed switches requires that the pedal panel be very closely aligned with the organ body to assure that the magnets activate the reed switches. There is very little tolerance for misalignment between the two.

Various techniques have been developed for coupling physically separate locations without the use of cables or other physical connections, such as by the use of transformer coils and photoelectric devices. Transformer coils are used to transfer power from one circuit to another and photoelectric devices are then used to transfer data. Examples of such systems are illustrated in U.S. Patent No. 2,967,267 issued to Steinman et al. on January 3, 1961 for "Reactive Intercoupling of Modular Units"; U. S. Patent No. 3,764,971 issued to Brobeck on October 9, 1973 for "Electric Alarm Device"; U. S. Patent No. 3,939,391 issued to Winnacker on February 17, 1976 for "Apparatus for Charging a Hermetically Sealed Electrical Energy Source"; U. S. Patent No. 4,737,898 issued to Banfalvi on April 12, 1988 for "Single-Ended Self-Oscillating, DC-DC Converter with Regulation and Inhibit Control"; U. S. Patent No. 4,761,724 issued to Brown et al. on August 2, 1988 for "Transformer Coupling for Transmitting Direct Current through a Barrier"; and in the article "Contactless Coupling for Power and Data", NASA Technical Briefs, September, 1988, pages 22 and 24. These references generally disclose various ways in which transformers are used to transfer power.

However, typically, there is also a need to transfer data between remote locations, and even through a physical barrier. The NASA article describes a system which uses infrared transmission of data and transformer coupling for power transmission. Such systems require that an optical pathway exist between the remote locations so that the infrared or equivalent optical coupling can occur.

It is desirable to have a data and power connection which does not require an optical pathway and also which does not require exact alignment between a base unit and a peripheral unit. Further, it is desirable that the data transmitted from the peripheral unit be synchronous with data processing in the base unit. It is also desirable in such a unit that the clock frequency of the data stream be below radio interference-causing frequencies. This necessitates that the data transmission rate between the peripheral and base units be lower than the typical frequency of a computer or central processing unit. It is additionally desirable to transfer data using sinusoidal waveforms rather than square waveforms in order to further reduce the radio frequency interference emissions. It is therefore also desirable to have a data transfer system in which data is fed to the CPU at a rate that is independent of the clock frequency of the CPU.

SUMMARY OF THE INVENTION

The present invention achieves these goals, and overcomes the associated limitations of the known prior art. In particular, the present invention provides a system for transferring data via a physically separated pair of inductor windings with data encoded in an alternating current signal which is applied to one coil and induced in the other. The encoded data may vary the alternating current in either winding, thereby permitting transfer of data in either or both directions.

In one aspect of the present invention, a system is provided for transferring data from a first location to a second location physically separated from the first location. Included are a first transformer winding, and means for applying an alternating current encoded with predetermined data to the winding. A secondary winding is positionable relative to and physically spaced from the primary

winding appropriately for the primary winding to magnetically induce in the secondary winding a corresponding alternating current encoded with the predetermined data. Means coupled to the secondary winding decodes the data from the induced alternating current.

The present invention further provides a similar system having a primary winding, and means coupled to the primary winding for applying to the primary winding an alternating current. Similarly, a secondary winding is positioned relative to and physically spaced from the primary winding appropriately for the primary winding to magnetically induce in the secondary winding a corresponding alternating current. However, this system further includes means for transmitting a data signal by varying the alternating current in one of the primary and secondary windings to be representative of the data signal. This induces corresponding variations in the alternating current conducted in the other of the primary and secondary windings. Also, means responsive to the variations in the alternating current in the other winding, generates a data signal representative of the variations in the alternating current of the other winding.

In yet another aspect of the present invention, a system, and associated method, are provided for transferring data from an element having at least two states to a data processing unit. This system includes a detector for detecting the current state of the element. Means, coupled to the detector generates, at a first frequency, element data representative of the detected current element state. A memory stores element data representative of the preceding element state. A comparator compares the current element state data with the preceding element state data. A latch stores only element data representative of a current element state that is changed from the preceding element state.

More specifically, the preferred embodiment of the present invention provides a set of state data-generating switches associated with the organ foot pedals, that are sequentially sensed in a peripheral unit by a data encoder that generates an encoded data stream having a sync pulse. Power and clock for the data encoder are provided through physically separate primary and secondary transformer windings, with the secondary windings being in the peripheral unit. The primary winding, located in a host unit, functions as the tank coil of a power oscillator. The alternating current signals conducting in the windings are also used to derive clock signals for data processing.

Data is transmitted by optical devices from the peripheral unit to the host unit. The data stream is detected and transmitted to a sync detector that determines the beginning of the data stream. A bit counter keeps track of the bit sequence and a data comparator determines whether each bit of data is different than the previously corresponding value for the bit. Only changes in the data are then sent to a CPU via a latch that stores the bit number and bit value. Control signals are used so that the CPU can determine when to read the data stored in the latch. This allows the CPU to operate at a frequency independent of the frequency of data generation and manipulation in the peripheral and host units.

In an alternative embodiment, data is also transmitted via the magnetically coupled windings. In this embodiment, the generation of data pulses loads the current in the secondary winding. This loading is reflected in the current produced by the power oscillator driver. This varying amplitude of current is decoded in the host unit to reestablish the data stream for processing as described with reference to the other embodiment. Thus data, in the forms of a clock signal and state data, are shown to be transferred in both directions via the magnetically coupled windings.

These and other features and advantages of the present invention will become more apparent from a review of the following detailed description of the preferred embodiments and the associated drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a system made according to the present invention.

Fig. 2 is a circuit schematic showing a peripheral unit contained within the system of Fig. 1.

Fig. 3 is a diagram of a pedal switch used with the circuit of Fig. 2 for generating state data.

Fig. 4 is a schematic of the host circuit shown generally in Fig. 1.

Fig. 5 is a block diagram showing an alternative embodiment for data transmission between the peripheral and host units of Fig. 1.

Fig. 6 is an illustration of the data stream and clock signals generated in the peripheral unit and received for synchronous sampling in the host unit in both embodiments.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring initially to Fig. 1, shown generally at 10 is a system made according to the present invention. System 10 comprises a peripheral unit 12, housed in a peripheral foot pedal unit, that receives state data from a data source 14, such as switches activated by foot pedals on an organ. These switches are also referred to as elements having two states. Peripheral unit 12 is coupled to a physically and electrically separated host unit 16,

that in turn is coupled to a microprocessor or central processing unit (CPU) 18. Host unit 16 transfers power and clock to, and receives synchronous state data from, peripheral unit 12 without interconnecting wires. Further, host unit 16 also translates the state data into transaction data to be sent to host CPU 18.

Peripheral unit 12 includes a coil 20, that functions as the secondary winding of a power transformer, a clock receiver 22 and a power receiver 24. Both power and a clock signal are derived from the current induced on coil 20. A data encoder 26 determines the switch or element state from data source 14, power from power receiver 24, and the clock signal from clock receiver 22. This data encoder serializes data bits representing switch states and interleaves the string of serial data bits with sync and control bits. The serialized data stream, also referred to as a second data signal, is output to a data transmitter 28. In this preferred embodiment, data transmission is by infrared emission, as will be described with reference to Fig. 2.

Host unit 16 includes a power oscillator 30 formed of a power oscillator driver 32, also referred to as means for applying an alternating current to a coil 34. Coil 34 functions as a primary coil relative to the power and clock pick-up coil 20 of peripheral unit 12. The coils are preferably formed on parallel planar circuit boards with the axes of the coils preferably coaxial. This arrangement allows the coils to be somewhat out of position and still provide magnetic coupling. Coil 34 also is the tank coil of oscillator 30. Oscillator 30 is free running and operates in the 20-40kHz range.

A clock driver 36 rectifies the alternating current signal produced by oscillator 30 to generate a clock signal, synchronous with the clock signal generated by clock receiver 22. A preamp/detector 38 translates detected infrared emissions carrying the data stream from data transmitter 28. Detector 38 is also referred to as means for detecting the second data signal.

The data is then transmitted to a sync detector 40 that monitors the incoming data and resets the count in a bit counter 42 when sync, identifying the start of the data stream, is detected. A first memory 44 holds an image of the last known state of the incoming bit stream. The data is input to a data comparator 46 that compares the prior data from memory 44 with the incoming data. When the data is different, the data in the memory 44 is replaced with the incoming data, and a strobe on a conductor 48 goes active. Further incoming data is ignored while the output strobe is active.

Strobe 48 is stored in a CPU interface functioning as a second memory or latch 50. When the strobe is active, it interrupts CPU 18. The CPU then reads the data output from bit counter 42 and detector 38 and stored in latch 50, as shown. When the CPU has read the new data information, it causes an acknowledge bit connected to data comparator 46 via a conductor 52 to go active. When the comparator senses the acknowledge input line as being active, it resets the output strobe to inactive. The CPU will not read the data existing in latch 50 so long as the strobe is in an inactive state.

Fig. 2 shows the circuit of peripheral unit 12 in further detail. Coil 20 is coupled to a combined circuit forming clock receiver 22 and power receiver 24. The alternating current existing on coil 20 is rectified by a rectifier 54, filtered by filter 56 and maintained at a 12 volt level by zener diode D2. The energy is stored in a capacitor C1. The clock is formed from the alternating current signal by a rectifier formed of diodes D4 and D16, which signal is fed into a counter U3 forming part of data encoder 26. The power generated and held in capacitor C1 is used to power the components of data encoder 26 and data transmitter 28.

Encoder 26 includes a couple of matrix switches U1 and U2. The low three bits from counter U3 are fed into the enabling inputs of switch U1. The upper three bits of counter U3 are fed into the enabling inputs of switch U2. This provides for an 8 X 8 switching matrix with the connecting of the X terminal to the XN terminal of U1 to form what may be considered rows of a switch matrix. Correspondingly, terminal X of switch U2 is selectively connected to the eight XM terminals to form what may be considered columns of a switch matrix. Thus, for each input of the enabling inputs to the switches, one of the XN terminals of switch U1 is connected to one of the XM terminals of switch U2 via a pedal switch 14. As indicated in Fig. 3 the right end of switch SW1 is connected to one of the rows associated with switch U1 and the cathode of a diode D3 is connected to a column defined by switch U2. As the clock count progresses on counter U3, each XN terminal of switch U1 is connected selectively to each XM terminal of switch U2.

The two X terminals to switches U1 and U2 are connected through data transmitter circuit 28, which includes a driving transistor Q1 and light emitting diode (LED) D1 for transmission of the data to the host unit 16.

The switch matrix provides an overall 8 X 8 matrix for generating a 64-bit data stream. However, data encoder 26 encodes the data with sync and control pulses that limit the number of data bits available for the foot pedal switches. As shown in Fig. 2, the X0 terminal of switch U2 is grounded. When this terminal is selected by the appropriate set of enabling inputs, all eight of the corresponding terminals in switch U1 are held low. This forms what is referred to as a sync pulse formed of eight

contiguous low pulses. This is used to identify the beginning of the data stream.

Further, terminal X7 of switch U1 is connected to each of the terminals X1 through X7 of switch U2 through diodes D5-D11. These diodes are always conducting when selected by the matrix switches. They do not sense the state of a pedal switch, as do the other terminal connections. Thus, each eighth bit in the data stream is always high. This guarantees that the only time that eight pulses will appear low is during the sync pulse. There are thus fifteen bits out of the 64-bit data stream that are used for control purposes and are not available for carrying pedal switch state data. A maximum of 49 pedal switches can be sensed with this configuration. It will be recognized that other switch configurations could be used to provide for fewer or more sensing of pedal switches.

The resulting data stream just described is represented by the upper signal in Fig. 6. The clcck signal input to counter U3 is represented by the lower signal. It will be noted that each data stream begins with eight low sync pulses. The sync pulses are followed by seven sets of eight data pulses. The first seven of each set of eight data pulses provide pedal switch state data. The eighth pulse always is a high pulse and does not represent switch data. After each 64-bit data stream is completed, another set of sync pulses identify the next stream of data pulses. These sync pulses and high bit pulses are used to verify the validity of the data that is being transmitted from peripheral unit 12 to host unit 16.

Fig. 4 shows in further detail the circuit schematic associated with host unit 16. The infrared data transmitted by data transmitter 28 in peripheral unit 12 is received and sensed by optical receiver U7. This receiver detects the data stream, and amplifies and transmits it to sync detector 40 and data comparator 46. The data going to the sync detector first passes through an inverter, represented by logic blocks U5A and U6C. This inverter output is connected to the reset of a low bit counter U2 which also receives the clock signal from clock driver 36.

The clock signal is derived from the alternating current applied to primary transformer windings 34 which form the tank coil for oscillator 30. Oscillator driver 32 includes a transistor Q1 and emitter resister R2. The current conducted by the transistor varies according to the loading on coil 34.

If counter U2 counts eight successive low bits (a sync pulse) then bit counter 42 shown as unit U4 is reset and counts the number of clock pulses. This count identifies the bit number in the data stream associated with the data on line D7 input to latch 50. The bit count associated with that data is represented on the input terminals D0-D6.

The preceding data stream values have been stored in memory U1 which is a 64-bit shift register. With each clock pulse, each successive value of prior data is output to a data comparator 46 which also receives the new data. Comparator 46 includes an exclusive OR gate that produces a high output only when there is a difference between the old and new data. This comparator output is input into a flip-flop U3A. The flip-flop generates a strobe on conductor 48, as discussed previously, that is stored in latch 50. This strobe is an interrupt to CPU 18. This interrupt tells the CPU that the data value stored on terminal D7, for the position value stored on terminals D0-D6, is new.

The CPU preferably operates at frequencies much greater than the frequency of the clock signal derived from the sine wave produced by oscillator 30. The values are held in latch 50 until the CPU 18 reads them. Once the values are read, an acknowledge signal, identified in Fig. 4 as "taken", is input to latch 50 from the CPU. This signal is used to reset flipflop U3A, which in turn resets the strobe signal to inactive.

At the time that the strobe value is changed to indicate that the data on D7 is new data, the inverse of the strobe is output from the flip-flop and logically ORed with the 'taken' signal (U5D) inverted again (U6B) and fed to the mode control pin of U1. From the time the signal goes active until the time the 'taken' signal goes active and then inactive again, new data is prevented from being entered into the memory (the old data is recirculated back into the memory).

Comparator 46 thus acts only for new-versus-old data comparison and does not directly affect data recirculation. The recirculation path occurs as stated above, with U1 pin 10 (mode control pin) is active (high). Old data flows from U1 pin 6 back into U1 pin 1 (the recirculate input). Register U1 is an image of the data in CPU 18. It thus serves as a separate memory which is independent of the CPU clock. It will be seen that there is thus no timing relationship between the CPU and the circuit of host unit 16. Further, since only transaction data is transmitted to the CPU, data transfer is at typically irregular times.

In the embodiments described with reference to Figs. 1-4, data in the form of a clock signal is transferred from primary winding 34 to secondary winding 20. Oscillator 30 is made to oscillate at the desired clock rate so that the alternating current signal can be rectified and used as a clock signal for both the components in the peripheral unit and the components in the host unit. This results in synchronous data transmission and reception. Thus, both power and clock signals are transmitted through the winding coils.

The infrared transmitter and receiver must be

aligned more closely than the coils to provide effective data transmission. This requirement may be overcome by providing data transmission from the peripheral unit to the host unit through the windings as well. In this way, an optical path is not required between the two units. This would allow for placement of opaque materials, such as wood, in between the units and still allow for conductorless data and power transmission.

This arrangement is provided by the circuit modifications shown in Fig. 5. In this embodiment the peripheral unit is the same except that diode D1 is not a light emitting diode. Encoder 26, by the nature of its operation, loads down or draws power according to the high or low level of the data bits being formed in the data stream. This produces a current in coil 20 that varies in accordance with the data stream. This change in power draw is correspondingly reflected in primary coil 34. The current delivered by the oscillator reflects the load presented to the oscillator. Thus, the data stream is represented by variations in the oscillator current. A modified data detection circuit 58 shown in Fig. 5 may be used to detect variations in the oscillator current. In this case, instead of using data transmitter 28, the power receiver 24 and coil 20 serve as the data transmitter.

In the embodiment shown in Fig. 5 the oscillator alternating current signal is input into a clock generator 60 very similar to clock driver 36 shown in host unit 16. A signal representative of the current in the emitter resister R2 of power oscillator driver 32, discussed previously, is input into an amplifier or gain block 62. This amplified signal is input into a comparator 64 to re-establish the logic levels of the data stream. These data logic levels are then fed into a data conditioning circuit 66 to produce a data stream equivalent to the data stream output from preamp/detector 38 in the embodiment of system 10. Detection circuit 58 can be seen to provide means for generating a data signal representative of variations in the oscillator current. Thus, both the clock and the data stream are derived from the alternating current applied to the primary winding 34. These signals are then used in an embodiment which is otherwise the same as that described for host unit 16 with reference to Fig. 4. The data is processed in the same way and fed to the CPU in the same fashion. Thus, except for the differences noted, these embodiments are the same.

It will be seen, that the present invention provides for power and clock signal transmission via the transformer windings in both embodiments with data transmission being alternatively provided through infrared optical means or by the load applied by the peripheral unit on the oscillator through the windings, as has just been described with reference to Fig. 5.

The present invention provides a connecterless peripheral unit that is easily moved and which eliminates possible damage due to the existence of a physical connector or cable. Transferring power and data between the peripheral and host units by either of the embodiments reduces physical alignment problems often associated with the other methods. The physical alignment requirements associated with the embodiment of Fig. 5, not including the infrared transmission link, are less rigid than that with the embodiment shown with reference to Figs. 2 and 3. The embodiment of Fig. 5 also provides for the insertion of opaque materials completely between the two units while still providing for power, clock and state data information transfer.

By using the power oscillator also as the data clock allows both units to have a common clock, thereby providing synchronous data transfer without requiring an additional communication channel. Thus, the power oscillator does double duty. In the embodiment of Fig. 5 it does triple duty by also providing data transfer from the peripheral unit to the base or host unit.

A high degree of confidence in data integrity of contiguous state data is maintained by testing for the presence of the sync bit. Loss of sync provides an indication of the removal or failure of the peripheral. Transferring continuous state data instead of transaction data from the peripheral unit to the host unit has the advantages of simpler data encoding and decoding. Then, transfer of transaction data to the CPU reduces CPU service time since only changes in state require attention of the CPU.

Using a free-running oscillator instead of one generated by the CPU further simplifies circuit topology for generation of a sinusoidal waveform, thus reducing RFI emissions. Since state information is not being transferred to the CPU by the free-running oscillator, the oscillator may operate at any convenient frequency. The frequency of oscillation is chosen low enough so as to discourage radio interference, but high enough to maximize the efficiency for the coil type used, and high enough to allow timely servicing of the input data.

It will further be realized that variations in the circuit design and detail may be made without varying from the spirit and scope of the invention as defined in the claims. Thus, although specific embodiments have been described, it will be appreciated by those skilled in the art that variations may be made in the embodiment while still practicing the present invention. For instance, much of the logic and data processing can also as readily be provided using microprocessors or equivalent. Thus, these components and specific circuit configurations are only exemplary. Those skilled in the

art will recognize other equivalent and readily apparent circuits which can be used to practice the invention.

Claims

1. A system for transferring data from a first location to a second location physically separated from the first location, comprising:

primary winding means;

means coupled to the primary winding means for applying to the primary winding means an alternating current encoded with predetermined data;

secondary winding means positionable relative to and physically spaced from the primary winding means appropriately for the primary winding means to magnetically induce in the secondary winding means a corresponding alternating current encoded with the predetermined data; and

means coupled to the secondary winding means for decoding the data from the induced alternating current.

2. A system according to claim 1 where the alternating current has a predetermined frequency, and the predetermined data is formed as a first data signal having a frequency proportional to the frequency of the alternating current, the decoding means converting the induced alternating current into a second data signal having the frequency of the first data signal.

3. A system according to claim 1 where the first data signal is a first clock signal having pulses occurring with the same frequency as the alternating current frequency, the decoding means converting the induced alternating current into a second clock signal.

4. A system according to claim 3 wherein the applying means and primary winding means, in combination, comprise oscillator means tuned to produce the alternating current with a frequency the same as the first clock signal frequency.

5. A system according to claim 4 further comprising:

means responsive to the second clock signal for transmitting a second data signal having a frequency equal to the frequency of the second clock signal;

means coupled to the oscillator means for producing the first clock signal with the same frequency as the alternating current frequency so that the first and second clock signals are synchronous; and

means, responsive to the first clock signal, for detecting the transmitted second data signal at intervals corresponding to the first clock signal.

6. A system according to claim 5 further comprising:

an element having at least two states;

means coupled to the element and the transmitting means for periodically determining the state of the element and producing the second data signal to be representative of the current state of the element;

means, coupled to the means for detecting the transmitted second data signal, for comparing the data representative of the current element state with the preceding element state; and

memory means, coupled to the comparing means, for storing data representative of an element state; the comparing means writing into the memory means only data representative of a current element state that is changed from the preceding element state.

7. A system according to claim 6 further comprising data processing means coupled to the memory means for sampling the value of the data stored in the memory means at a frequency different than the frequency of the first clock signal.

8. A system according to claim 7 wherein the comparing means transmits status data indicative of whether the data representative of the element state stored in the memory means is representative of the current element state, the data processing means being responsive to the status data stored in the memory means for determining whether to receive the data representative of the element state stored in the memory means.

9. A system according to claim 5 wherein the means for transmitting the second data signal varies the amplitude of the induced alternating current according to the second data signal, thereby inducing corresponding amplitude variation in the alternating current conducted in the primary winding means; the means for detecting the second data signal further being coupled to the oscillating means for detecting the transmitted second data signal by detecting the amplitude variation in the alternating current conducted in the primary winding means.

10. A system for transferring data from a first location to a second location physically separated from the first location comprising:

primary winding means;

means coupled to the primary winding means for applying to the primary winding means an alternating current;

secondary winding means positionable relative to and physically spaced from the primary winding means appropriately for the primary winding means to magnetically induce in the secondary winding means a corresponding alternating current;

means for transmitting a data signal by varying the alternating current in one of the primary and secondary winding means to be representative of the data signal, thereby inducing corresponding variations in the alternating current conducted in the other of the primary and secondary winding means; and

means, responsive to the variations in the alternating current in the other winding means, for generating a data signal representative of the variations in the alternating current of the other winding means.

11. A system according to claim 10 wherein the applying means applies an alternating current having a predetermined frequency, thereby inducing in the secondary winding means an induced alternating current of the same frequency; the transmitting means is responsive to the alternating current for varying the alternating current amplitude at a frequency equal to the frequency of the alternating current; and the generating means detects the alternating current amplitude variations at intervals corresponding to the alternating current frequency so that the generated data signal is synchronous with the transmitted data signal.

12. A system for transferring data from an element having at least two states to a data processing means comprising:

means for detecting the current state of the element;

means coupled to the detecting means for generating, at a first frequency, element data representative of the detected current element state;

first memory means, coupled to the generating means, for storing element data representative of the preceding element state;

means, coupled to the generating means and the first memory means, for comparing the element data representative of the current element state with element data representing the preceding element state; and

second memory means, coupled to the comparing means and to the data processing means, for storing element data representative of a state of the element, the comparing means writing to the second memory means only element data representative of the current element state that is changed from the preceding element state.

13. A system according to claim 12 further comprising data processing means coupled to the second memory means for sampling the element data stored in the second memory means at a frequency different than the first frequency.

14. A system according to claim 12 wherein the comparing means further writes to the second memory means status data indicative of whether the element data stored in the second memory means is representative of the current element state, the data processing means being responsive to the status data stored in the second memory means for determining whether to sample the element data stored in the second memory means.

15. A system according to claim 14 wherein the data processing means writes to the second memory means response data indicating whether the data processor means has sampled the element data stored in second memory means, the comparing means writing element data to the second memory means only after the data processing means has sampled the element data in the second memory means.

16. A system according to claim 15 wherein the comparing means, responsive to the response data, writes to the second memory means status data indicating that the data processing means has sampled the element data stored in the second memory means.

17. A method for transferring data from an element having at least two states to a data processing means comprising:

detecting the current state of the element;

generating, at a first frequency, element data representative of the detected current element state;

storing, in a first memory, element data representative of the preceding element state;

comparing the element data representative of the current element state with the stored element data representing the preceding element state; and

storing, in a second memory means, only element data representative of a current element state that is changed from the preceding element state.

18. A method according to claim 17 further comprising sampling, by the data processing means, the element data stored in the second memory means at a frequency different than the first frequency.

19. A method according to claim 17 further comprising storing, in the second memory means, status data indicative of whether the element data stored in the second memory means is representative of the current element state; and prior to the step of transmitting, determining the status data stored in the second memory means.

20. A method according to claim 19 further comprising storing, in the second memory means, response data indicating whether the element data has been transmitted to the data processing means, the step of transferring element data to the second memory means occurring only after the response data indicates that the element data has been transmitted to the data processing means.

21. A method according to claim 20 further comprising the step of storing status data, in the second memory means, indicating that the element data has been transferred to the data processing means.

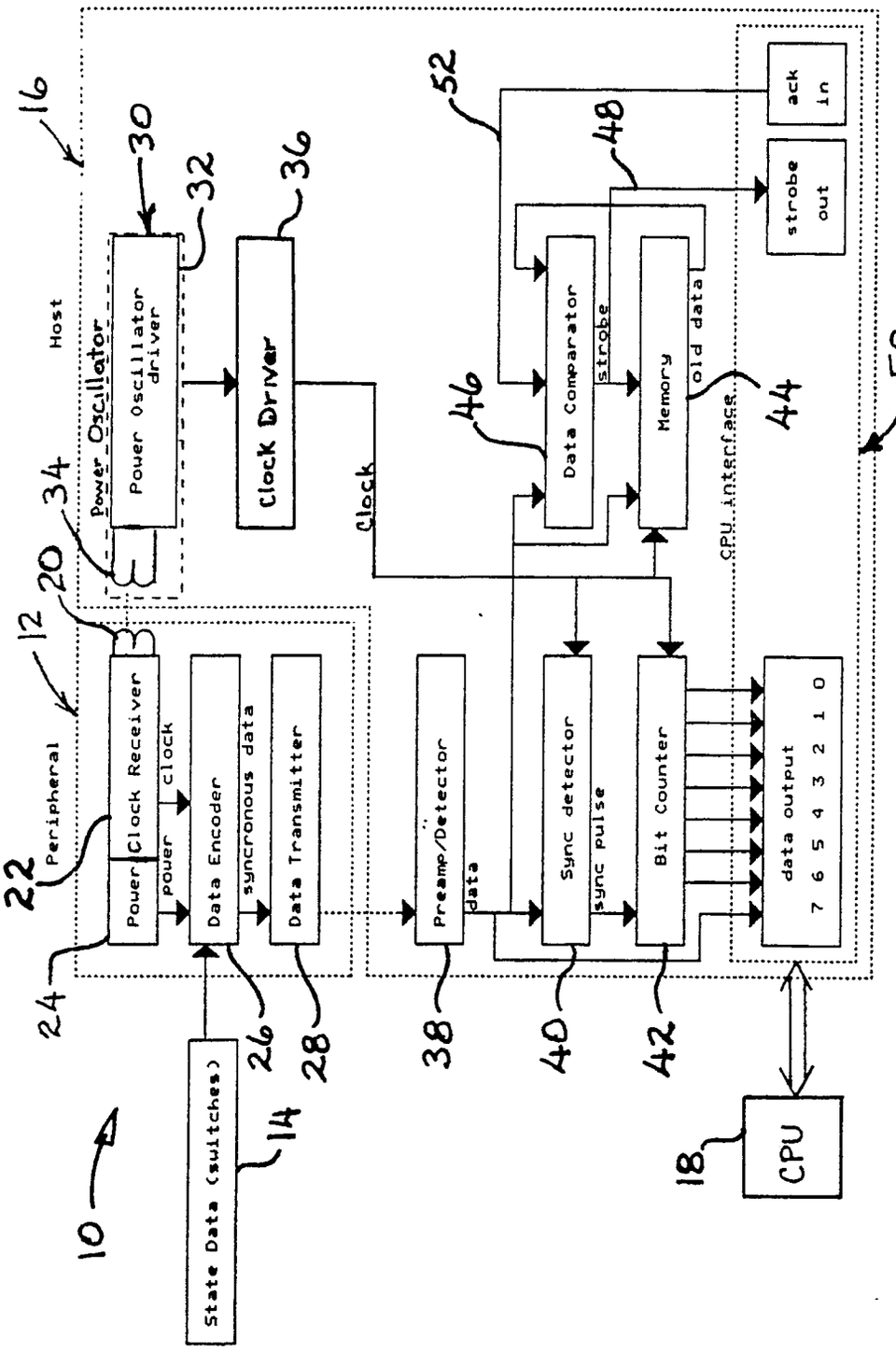
16
Host
Power Oscillator
Power Oscillator driver
30
32
34
36
Clock Driver
Clock
20
12
Peripheral
22
Power
Clock Receiver
clock
power
Data Encoder
syncronous data
Data Transmitter
24
26
28
State Data (switches)
14
10
Preamp/Detector
data
38
Sync detector
sync pulse
40
Bit Counter
42
data output
7 6 5 4 3 2 1 0
CPU
18
52
48
46
Data Comparator
strobe
Memory
old data
44
CPU interface
50
ack in
strobe out

FIG. 1

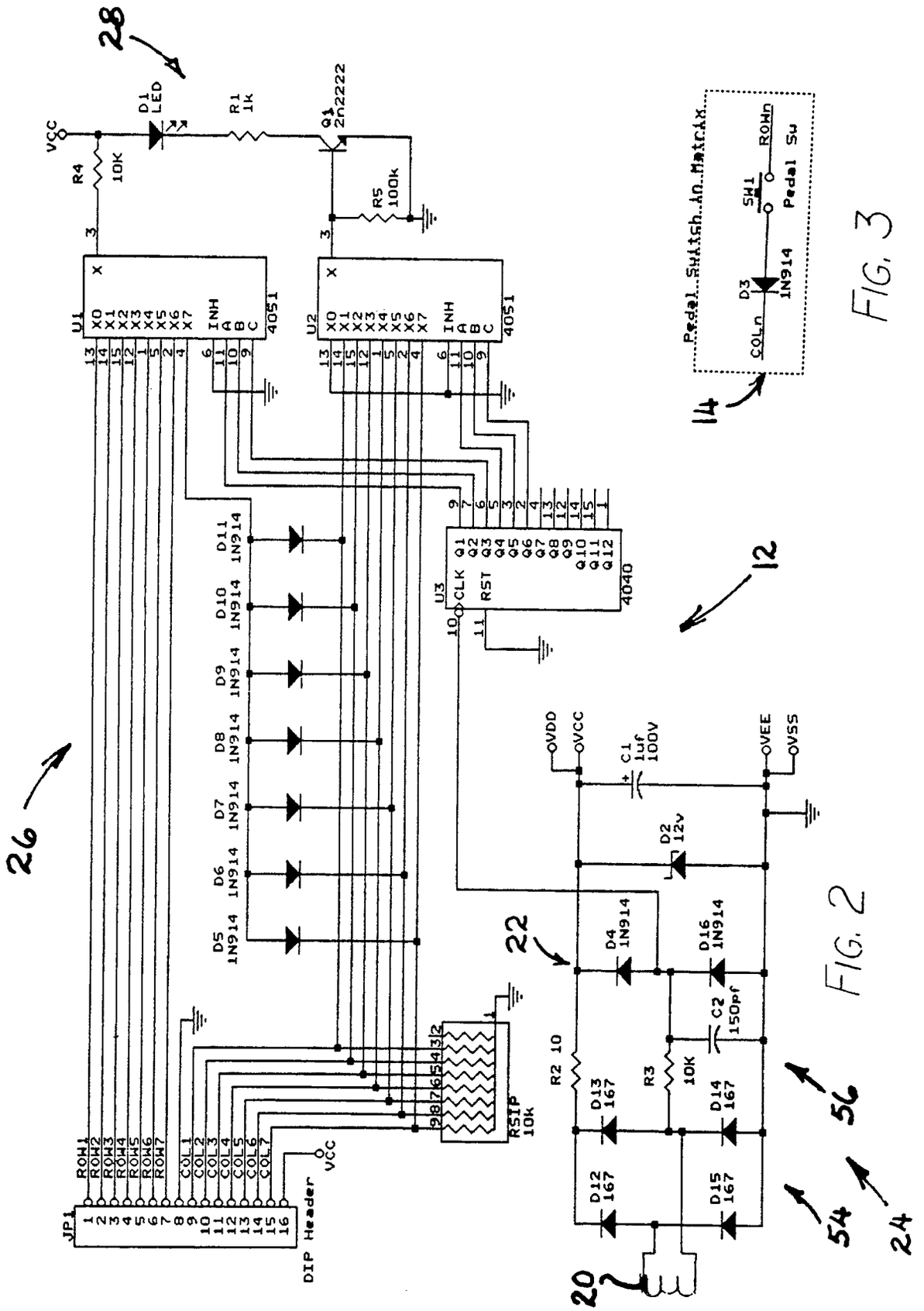
28
VCC
D1 LED
R1 1k
Q1 2n2222
R4 10K
R5 100k
U1 4051
U2 4051
U3 4040
CLK
RST
D11 1N914
D10 1N914
D9 1N914
D8 1N914
D7 1N914
D6 1N914
D5 1N914
26
12
VDD
VCC
C1 1uf 100V
VEE
VSS
D2 12v
22
D4 1N914
D16 1N914
C2 150pf
R2 10
R3 10K
D13 167
D14 167
D12 167
D15 167
56
54
24
20
RSIP 10K
JP1
DIP Header
ROW1
ROW2
ROW3
ROW4
ROW5
ROW6
ROW7
COL1
COL2
COL3
COL4
COL5
COL6
COL7
Pedal Switch Matrix
SW1
Pedal Sw
D3 IN914
COLn
ROWn
14

FIG. 2

FIG. 3

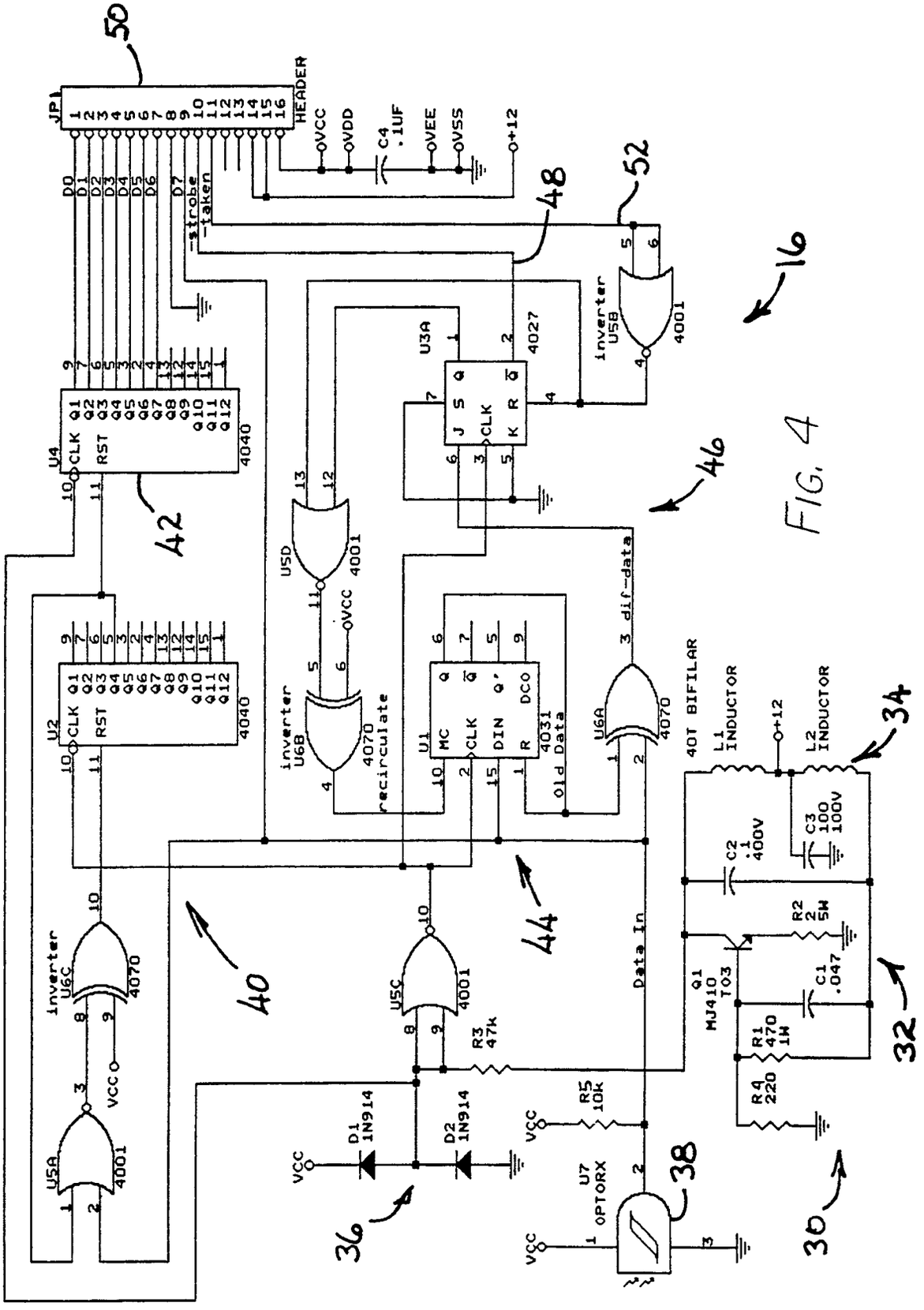
50
JP1
HEADER
VCC
VDD
C4
.1UF
VEE
VSS
+12
D0
D1
D2
D3
D4
D5
D6
D7
-strobe
-taken
48
52
16
U4
CLK
RST
4040
42
U3A
4027
J
S
CLK
K
R
inverter
U5B
4001
46
U5D
4001
VCC
inverter
U6B
4070
recirculate
U2
4040
U1
MC
CLK
DIN
DCO
4031
Old Data
3 dif-data
U6A
4070
40T BIFILAR
L1
INDUCTOR
L2
INDUCTOR
34
C2
.1
400V
C3
100
100V
R2
2
5W
Q1
MJ410
TO3
C1
.047
R1
470
1W
R4
220
32
40
inverter
U6C
4070
U5A
4001
VCC
U5C
4001
R3
47K
44
Data In
D1
1N914
D2
1N914
R5
10K
U7
OPTORX
38
36
30

FIG. 4

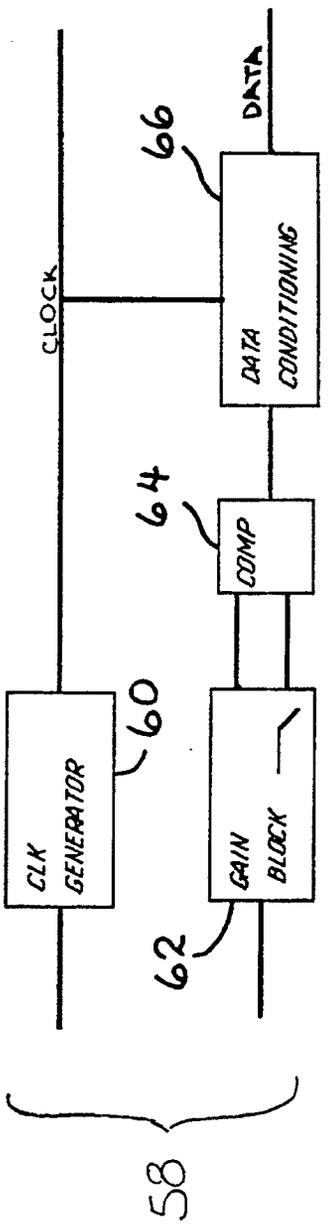
CLK GENERATOR
60
GAIN BLOCK
62
COMP
64
DATA CONDITIONING
66
CLOCK
DATA
58

FIG. 5

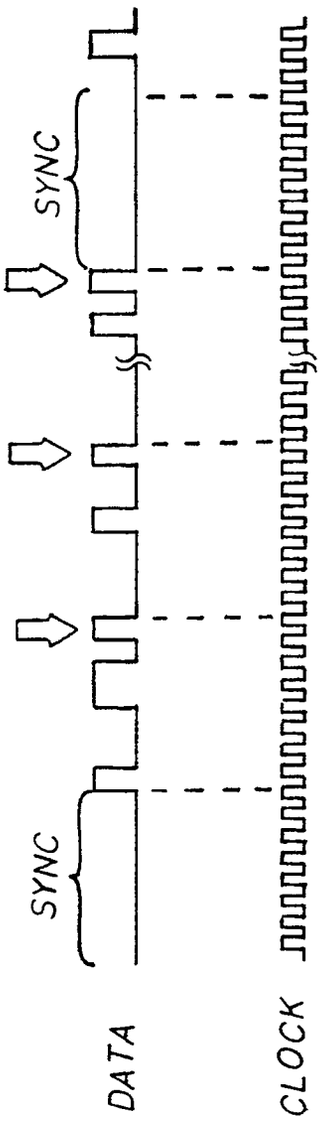
SYNC
SYNC
DATA
CLOCK

FIG. 6