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(54) Current mirror with base current compensation.

(57) A current mirror circuit with master (T1) and slave bipolar transistors (T2, T3) has an insulated gate field effect transistor (FET) (M1) connected across the collector-base circuit of the master transistor (T1) to provide base compensation current for the various bipolar transistors (T1, T2, T3). The FET (M1) is scaled so that the collector-emitter voltage of the master transistor (T1) is set at a value at which it operates in the vicinity of its saturated region, and the collector-base voltages of the master (T1) and slave transistors (T2, T3) are generally equal. This results in an accurate mirroring of the master transistor (T1) current, while the current through the master transistor (T1) is itself preserved at the desired reference level because the FET (M1) does not draw any gate current away from the master transistor (T1).

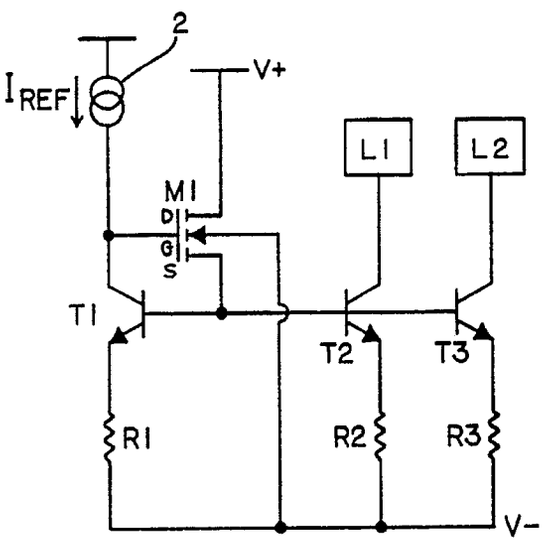

Fig. 4

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BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to current mirror circuits with base current compensation for the transistor which carries a reference current.

Description of the Prior Art

Current mirror circuits are used to establish one or more load currents which are matched to a reference current. A typical prior current mirror circuit is shown in FIG. 1. A reference current I_{REF} is delivered from a current source 2 to a diode-connected bipolar transistor T1. The collector of T1 is connected to its base and receives I_{REF}, while the emitter of T1 is connected through a resistor R1 to a negative voltage bus V-1. T1 may be considered as a master transistor, since it acts as a reference which controls the output of the current mirror.

One or more slave transistors, illustrated as a pair of bipolar transistors T2 and T3, have a common base connection with master transistor T1. The collector-emitter circuits of T2 and T3 are connected respectively to loads L1 and L2 on one side, and through resistors R2 and R3 to V- on the other side. By scaling the dimensions of T2 and T3 appropriately, they can be proportionately matched to T1 so as to deliver load currents which are similarly proportionately matched with the reference current through T1. The values of resistors R1, R2 and R3 are generally inversely proportional to their respective transistor scalings, so that the base-emitter voltages of the various transistors are equal and the voltages across the resistors are also equal. This resistor arrangement helps to compensate for transistor processing variations.

There is an inherent error in the FIG. 1 current mirror, resulting from the base currents drawn by T1, T2 and T3. The combined base currents are subtracted from I_{REF} before the reference current reaches the collector of T1, and thus reduce the T1 collector current. This in turn reduces the reference current seen by T2 and T3, dropping their slaved output currents to values which are proportionately less than the desired load currents.

A prior circuit design which compensates for this base current error is shown in FIG. 2. Another bipolar transistor T4 has been added to provide base current compensation for the current mirror transistors. The base of T4 is connected to receive a control signal from the output of current source 2, while its collector-emitter circuit is connected between a positive voltage bus V+ and the common base connection for T1, T2 and T3. The compensation transistor T4 is scaled so that it provides a current equal to the combined base currents of T1, T2 and T3, and thus ideally eliminates the base current error of FIG. 1.

The improved circuit of FIG. 2 is unfortunately still subject to errors. T4 obtains its base current from I_{REF}, and thus introduces a second order error into the reference current through T1. In addition, T4 places restrictions on the voltages across T1 that introduce further inaccuracies. T2 and T3 are normally operated with collector-emitter voltages of about 2-3 volts, which is the voltage region at which the collector current (I_c)/ collector-emitter voltage ($V_{c\text{-}e}$) curve becomes saturated, as illustrated in FIG. 3. However, the collector-base voltage of T1 is limited to a voltage drop of about 0.7 volts by the parallel base-emitter circuit of T4, and the base-emitter voltage drop of T1 is similarly limited to an approximately 0.7 volt diode drop. The total collector-emitter voltage across T1 is thus limited to about 1.4 volts, which is significantly less than the saturation level. The 0.7 volt collector-base restriction on T1 also introduces an error in the actual master/slave current ratio, since the collector-base voltages of T2 and T3 are typically greater than 0.7 volts.

When the current mirrors of FIGs. 1 or 2 are used over the full military temperature range (-40° - 160° C), the transistor current gain β varies by a factor of between approximately 2 and 5. This can significantly change the base current taken by T4, and thus the reference current through the collector-emitter circuit of T1, thereby adding to the error already present in the circuit.

SUMMARY OF THE INVENTION

The present invention seeks to provide a current mirror circuit which produces effective base current compensation for a bipolar master transistor, does not restrict the master transistor voltages to values less than the slave transistor voltages, is less subject to temperature-induced errors, and generally has a more accurate and predictable mirror ratio than the prior circuits.

These goals are accomplished by connecting an insulated gate field effect transistor (FET) to provide a base compensation current for a bipolar current mirror circuit. The FET gate is connected to the collector of the master bipolar transistor, but draws no current therefrom. The gate-source circuit of the FET is connected to provide a compensating base current to the bipolar mirror transistors. The FET is geometrically scaled so that the collector-base voltages of the master and slave bipolar transistors are generally equal, and to establish the collector-emitter voltages of the bipolar transistors at values at which the bipolar transistors operate in the vicinity of their saturated regions. Since the

collector-base voltage of the master bipolar transistor is no longer limited to about 0.7 volts, the errors associated with such a limitation are also removed.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of a preferred embodiment, taken together with the accompanying drawings, in which:

DESCRIPTION OF THE DRAWINGS

FIGs. 1 and 2 are circuit diagrams of prior current mirror circuits, discussed above;

FIG. 3 is a graph showing the collector current/collector-emitter voltage characteristic for a typical bipolar transistor; and

FIG. 4 is a circuit diagram of a preferred embodiment for the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The preferred embodiment of the invention is illustrated in FIG. 4, in which elements that are common with the elements of FIGs. 1 and 2 are identified by the same reference numerals. As with the prior circuits, current source 2 delivers a reference current through the collector-emitter circuit of a bipolar master transistor T1. Bipolar slave transistors T2 and T3 have a common base connection with T1, and provide load currents to loads L1 and L2, respectively. The transistor emitters are connected to negative voltage bus V- through respective process-compensating resistors R1, R2 and R3.

Reference current source 2 is implemented as a temperature compensated, source compensated current source which is carefully set up to obtain an exact desired value. This precise reference current is preserved by using an insulated gate FET such as metal oxide FET (MOSFET) M1 to supply base compensation current to the bipolar transistors. M1 has its gate connected between the collector of master bipolar transistor T1 and the reference current source 2, its drain connected to positive voltage bus V+, and its source connected to the common base connection of T1, T2 and T3. The back gate is connected to the body of the substrate upon which the circuit is formed, which is typically held at V-. Since the current through an insulated gate FET such as M1 is controlled by the gate voltage, without drawing any gate current, all of I_{REF} flows through master bipolar transistor T1, thus preserving the accuracy of the reference current that reaches the current mirror.

The use of an insulated gate FET as a base compensation current device permits a much more desirable control over the voltages for master transistor T1. M1 is scaled so that, given its desired base current compensation current flow as established by the value of V+, the gate-source voltage of M1 equals the desired collector-base voltage for T1. This M1 gate-source voltage is imposed upon the parallel collector-base circuit of T1. With a conventional diode drop of about 0.7 volts across the base-emitter circuit of T1, the gate-source voltage of M1 (and thus the collector-base voltage of T1) will generally be set at about 1.3-2.3 volts so that M1 operates in the vicinity of its saturated region, as illustrated in FIG. 3. The precise value selected for the collector-base voltage of T1 will set that voltage equal to the collector-base voltages of slave transistors T2 and T3, and thus preserve the designed proportionality of the mirror.

The exact scaling of M1 that will produce this voltage level is highly dependent upon the particular process used to fabricate the circuit; several "BICMOS" processes are known that can be used to fabricate bipolar and CMOS devices on the same chip. Given a particular process and a knowledge of the invention, a scaling for M1 can readily be determined that will produce the desired gate-source voltage level.

M1 is illustrated as an enhancement device, and can be used to provide a collector-emitter voltage for T1 in the two-three volt range. If a substantially lower collector-emitter voltage for T1 is desired, or even a marginally negative voltage, M1 could be implemented as a depletion device.

While a particular embodiment of the invention has thus been shown and described, it should be understood that numerous variations and alternate embodiments will occur to those skilled in the art. For example, while bipolar transistors T1, T2 and T3 are shown in FIG. 4 as npn devices, the circuit could also be implemented with pnp transistors. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

Claims

1. A base current compensated current mirror circuit comprising:

   a master bipolar transistor (T1) and at least one slave bipolar transistor (T2, T3) having a common base connection with the master transistor (T1) in a current mirror configuration and proportionately matched with said master transistor (T1), and

   an insulated gate field effect transistor (FET) (M1) having a gate connected to the collector of the master bipolar transistor (T1), and a source-drain circuit connected to provide a base current compensation current to said common base connection.

2. The current mirror circuit of claim 1, wherein said insulated gate FET (M1) is geometrically

scaled so that the collector-base voltages of the master (T1) and slave transistors (T2, T3) are generally equal.

3. The current mirror circuit of claim 1, wherein said insulated gate FET (M1) is geometrically scaled to establish the collector-emitter voltages of the master (T1) and slave transistors (T2, T3) at values at which said transistors operate in the vicinity of their saturated regions.

4. The current mirror circuit of claim 3, wherein said insulated gate FET (M1) is geometrically scaled to establish the collector-emitter voltage of the master (T1) and slave transistor (T2, T3) at approximately 2-3 volts.

5. A base current compensation current mirror circuit, comprising:

a master bipolar transistor (T1) and at least one slave bipolar transistor (T2, T3) having a common base connection with the master transistor (T1) in a current mirror configuration and proportionately matched with said master transistor (T1),

a current source (2) connected to supply a reference current (I_{REF}) to the collector-emitter circuit of said master transistor (T1),

a voltage supply (V+), and

an insulated gate field effect transistor (FET) (M1) having a gate connected to the collector of the master bipolar transistor (T1), and a source-drain circuit connected between said voltage supply (V+) and said common base connection, said FET (M1) being configured to substantially supply the base currents of said master (T1) and slave bipolar transistors (T2, T3).

6. The current mirror circuit of claim 5, wherein said insulated gate FET (M1) is geometrically scaled so that the collector-base voltages of the master (T1) and slave transistors (T2, T3) are generally equal.

7. The current mirror circuit of claim 5, wherein said insulated gate FET (M1) is geometrically scaled to establish the collector-emitter voltages of the master (T1) and slave transistors (T2, T3) at values at which said transistors operate in the vicinity of their saturated regions.

8. The current mirror circuit of claim 7, wherein said insulated gate FET (M1) is geometrically scaled to establish the collector-emitter voltages of the master (T1) and slave transistors (T2, T3) at approximately 2-3 volts.

9. The current mirror circuit of claim 5, further comprising respective resistors (R1, R2, R3) connected to the collector-emitter circuits of said master (T1) and slave bipolar transistors (T2, T3), the resistance values of said resistors (R1, R2, R3) being generally inverse to the intended scalings of their respective bipolar transistors (T1, T2, T3) to at least partially compensate for manufacturing tolerances in said transistor scalings.

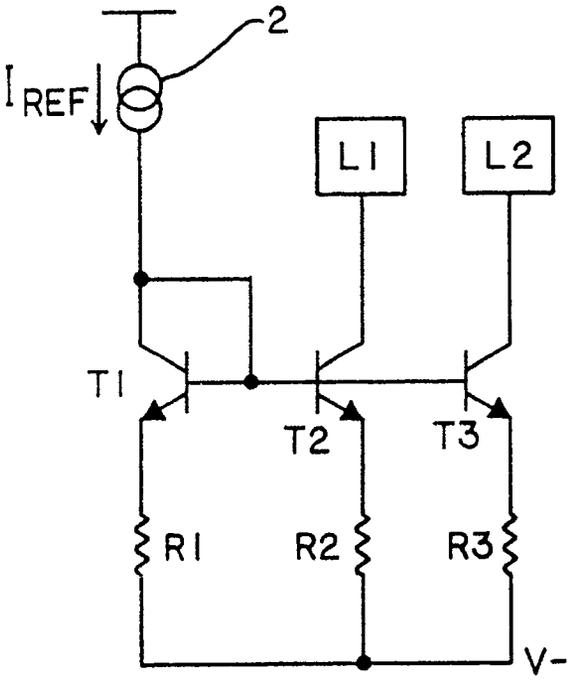

Fig. 1 (Prior Art)

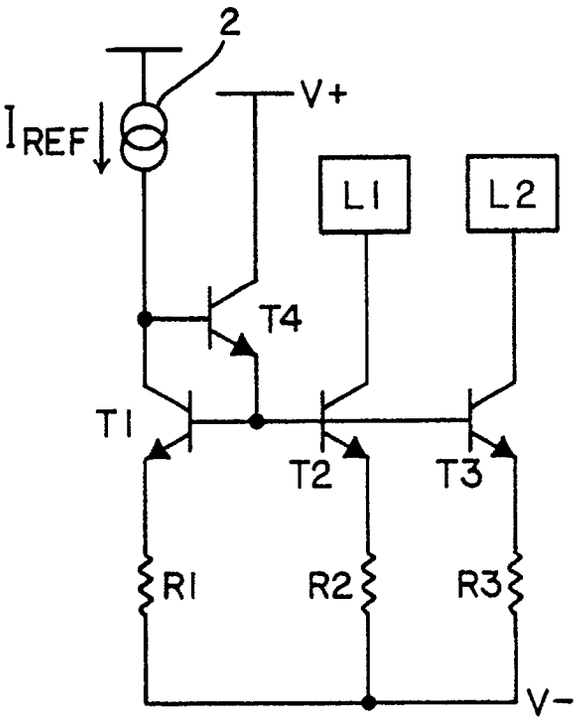

Fig. 2 (Prior Art)

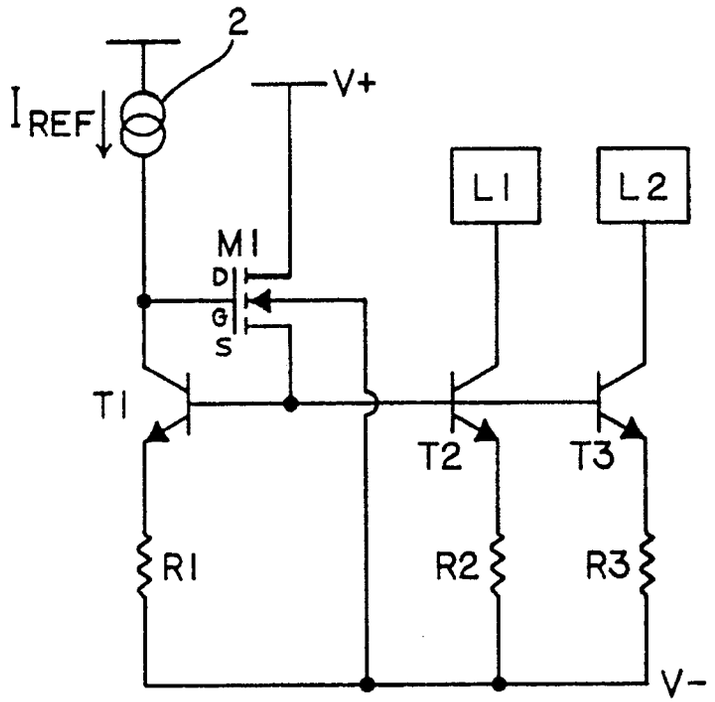

Fig. 4

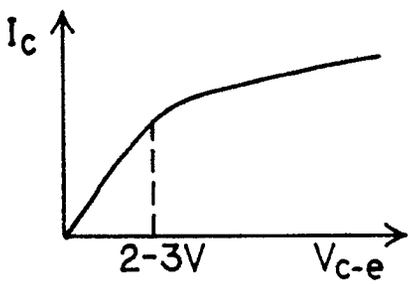

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 30 9886

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 008 441 (SCHADE) * The whole document *	1,2,5,6,9	G 05 F 3/26
A		3,4,7,8	
A	US-A-4 673 867 (DAVIS) * Abstract; column 1, line 1 - column 2, line 4; figure 1 *	9	
A	J. MILLMAN et al.: "Integrated electronics", 26th printing, 1971, pages 322-328, McGraw-Hill International Book Co., JP * Pages 322-323; figures 10-14 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 05 F 3

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	10 May 91	SAEAEW L.J.P.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
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