(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 444 845 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.04.1996 Bulletin 1996/17

(51) Int Cl.[6]: **G06F 11/26**

(21) Application number: **91301483.3**

(22) Date of filing: **25.02.1991**

(54) **Semiconductor apparatus including semiconductor integrated circuit and operating method thereof**

Halbleitervorrichtung mit integrierter Halbleiterschaltung und Betriebsverfahren dafür

Appareil semiconducteur avec circuit intégré semiconducteur et son mode opératoire

(84) Designated Contracting States:
DE GB NL

(30) Priority: **26.02.1990 JP 46569/90**

(43) Date of publication of application:
04.09.1991 Bulletin 1991/36

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EP 0 444 845 B1

Description

The present invention relates to integrated circuit testing and concerns boundary scan semiconductor integrated circuits (these have an internal facility for conducting tests of the integrity of internal connections and also external connections between themselves and the semiconductor integrated circuits), circuit board assemblies of such circuits, and methods of internal and external testing using the same.

Recent development of surface mounting technique has rendered tests (mainly in-circuit tests) of printed boards difficult.

In the in-circuit test, after chips have been mounted on a board, probes of spring type arranged with spacings of several millimeters are applied onto a rear surface of a substrate so as to individually test every chip for the test of the board. Because of the recent development of the surface mounting technique, however, the in-circuit test has such a problem that the probes cannot be applied to terminals of the chips. Further, specially manufactured jigs may often be too expensive. In order to solve these problems, such a boundary scan has conventionally been employed that a scan design, as used for facilitating an internal test of a chip, is extended to a board level. The boundary scan is a method in which a shift register including a latch circuit is connected to an input/output of each chip to form a serial connection for establishing a scan path. This method is described in detail in, for example, IEEE Std. 1149.1-1990, Standard Test Access Port and Boundary-Scan Architecture, issued by The Institute of Electrical and Electronics Engineers on May 21, 1990.

Fig. 15 is a block diagram of a board including chips which have a boundary scan facility as specified in the above article.

Referring to Fig. 15, there are provided at edges of a board 1, input/output terminals 2 a scan input terminal 3 for supplying test data as an input, a scan output terminal 4 for supplying test data as an output, and so forth. A plurality of chips 5 are mounted on the board 1. Circuit blocks 6, boundary scan registers 7, control circuits 8 and the like are integrated in the chips 5. Each circuit block 6 is connected to input/output terminals 9 arranged at the peripheries of the chip 5 through boundary scan registers 7. The input/output terminals 9 are connected through system signal lines 10 to the other input/output terminals 9 or input/output terminals 2 of the board. The above-described control circuits 8 each generate control signals for performing an operation test (internal test) of the chips 5, a connection test (external test) between the chips 5 and an operation test (sample test) of the entire board by employing the boundary scan registers 7. The control circuits 8 also generate control signals for performing a normal operation. Further, the control circuits 8 transmit a test signal from the scan input terminal 3 or another chip 5 and supply as an output test data from the scan output terminal 4 via a test signal line 11.

Fig. 16 is a block diagram of the above-described chip 5. Referring to Fig. 16, the boundary scan registers 7 are each connected through input/output buffers 9' to the input/output terminals 9 of the chip 5. The control circuit 8 receives through shift paths 11 test data TDI, a test mode select signal TMS and a test clock signal TCK. The control circuit 8 responds to these signals to generate clock signals SCLK1, SCLK2, UPCLK and CPCLK for controlling the boundary scan registers 7 and also generate a signal LT for switching data input terminals DI and scan input terminals SI of the boundary scan registers 7. The control circuit 8 applies the test data TDI through a scan output terminal SO to the data input terminals SI of the boundary scan registers 7 and also applies the clock signals SCLK1, SCLK2, UPCLK and CPCLK and the control signal LT to the boundary scan registers 7. Each of the boundary scan registers 7 responds to a control signal from the control circuit 8 to select either the input terminal DI connected to each input/output terminal 9 of the chip 5 or the scan input terminal SI connected to each output terminal SO of the control circuit 8 and also select either the scan output terminal SO or a data output terminal DO. The test data supplied from the scan output terminal SO of the boundary scan register 7 is sequentially shifted by the boundary scan register 7. The shifted test data is then applied to the scan input terminal SI of the control circuit 8. The control circuit 8 outputs the scan-input test data through a test data output port TDO at a predetermined timing. Fig. 19 shows the waveforms of the control signal LT, test data SI, clock signals SCLK1, SCLK2, CPCLK and UPCLK generated by the control circuit 8, an input signal of the input terminal DI of the boundary scan register 7, the scan output terminals SO, and the data output terminals DO.

Figs. 17A, 17B and 17C are block diagrams schematically showing the flow of test data in portions (a), (b) and (c) surrounded by a chain-dotted line. Referring to Figs. 17A, 17B and 17C, a reference character 7i denotes a boundary scan register connected to an input terminal 9i of a chip 5, and 7o denotes a boundary scan register connected to an output terminal 9o of the chip 5. Although a plurality of boundary scan registers are provided, and all the boundary scan registers provided on the same chip are serially connected to form a single shift bus, only one input and one output are shown in the figures for simplification of the description. A description will now be made on the flow of test data in the above-described three types of tests with reference to those figures.

[I] Internal Test

Referring to Fig. 17(A), the shift bus transmits the test data, which is input to the scan-in terminal SI of the boundary scan register 7i connected to the input terminal 9i of the chip 5. As a result thereof, the data is set.

The data set in the boundary scan register 7i is applied through the data output terminal DO of the boundary scan register 7i to the circuit block 6 and is processed therein. A processed result of the circuit block 6 is input to the data input terminal DI of the boundary scan register 7o connected to the output terminal 9o, and thus the data is set in the boundary scan register 7o. A processed result of the circuit block 6 set in the boundary scan register 7o is shifted-out through the scan terminal SO of the boundary scan register 7o. The shifted-out data is output via the shift bus and further via the test signal line 11 to the scan output terminal 4. The test output data output from the output terminal 4 may be observed to confirm whether the chip 5 has operated correctly or not.

[II] External Test

Referring to Fig. 17B, in order to perform the test of connection between the chips, the test data for the external test is shifted into the scan input terminal SI of the boundary scan register 7o connected to the output terminal 9o of the chip 5. As a result thereof, the test data is set in the boundary scan register 7o. The set test data is output through the data output terminal DO to the output terminal 9o. This output data is applied through the system signal line 10 to the input terminal 9i of another chip. The test data input through the input terminal 9i of another chip 5 is captured in the boundary scan register 7i connected to the input terminal 9i. The captured test data is shifted-out from the scan output terminal SO. Similarly to the internal test, the shifted-out data is output from the scan output terminal 4. The output test data may be observed to confirm the connection of the signal connection 10 between the chips 5. By this test, it is possible to test disconnection between the chips as well as openings and short-circuiting of the connection between the chips due to a failure of soldering between the chips and the board.

[III] Sample Test

By the internal test and the external test described above, it is possible to test the connections in and between the individual chips 5 forming the board 1. However, it is impossible to confirm the mutual effect of the chips 5 after the chips are mounted on the board 1 and the function thereof in the operation of the system. For the confirmation of those effect and function, the system (i.e., board) will be operated normally. In this operation, a signal at a node connected to the boundary scan register 7 is captured into the boundary scan register at a given timing without preventing the normal operation to observe them. This makes it possible to confirm the mutual effect of the circuits in the normal operation and the function thereof in the system operation. An operation of the sample test will be described below with reference to Fig. 17C.

The data input through the input terminal 9i of the chip 5 is input to the circuit block 6, and is simultaneously captured in the boundary scan registers 7i and 7o connected to the input terminal 9i and output terminal 9o, respectively, whereby the data is shifted-out from the scan output terminal SO without affecting the operation of the circuit block 6. Thus, the functions of the boundary scan register required for performing the internal and external tests are: (1) to capture the data input through each data input terminal DI into the boundary scan registers 7, (2) to shift the data from the scan input terminal SI to the scan output terminal SO, and (3) to apply the data held in the boundary scan register 7 to the data output terminal DO, (the functions (1), (2) and (3) will be called as CAPTURE, SHIFT and UPDATE hereinafter, respectively). The sample test requires the functions (1) and (2). For carrying out the sample test, the capture and shift operations themselves should not exert influence on the output terminals DO. The internal test and external test are carried out in the order of SHIFT → UPDATE → CAPTURE → SHIFT, and the sample test is carried out in the order of CAPTURE → SHIFT.

Fig. 18A is a circuit diagram specifically illustrating the above boundary scan register 7. Referring to Fig. 18, the boundary scan register 7 includes a selector circuit 12 having two inputs and one output, a latch circuit 13, a latch circuit 14 and a latch circuit 15 as well as the above-described data input terminal DI, scan input terminal SI, data output terminal DO and scan output terminal SO, and also includes input terminals 16, 17, 18, 19 and 20 of which inputs are the control signals LT, CPCLK forming the timing for CAPTURE, shift clocks SCLK1 and SCLK2 for shifting the input data and the clock signal UPCLK for outputting the data, respectively. The selector circuit 12 is a circuit for switching and selecting the input terminal D1 or D2 in accordance with the control signal LT from the control circuit 8. This circuit 12 includes an input terminal D2 connected to an output terminal Y of the latch circuit 15, an input terminal D1 connected to the data input terminal DI, a data output terminal D0 and an output terminal Y connected to an input terminal D1 of the latch circuit 13. The latch circuit 13 includes two data input terminals D1 and D2, and control terminals C1 and C2. The circuit 13 latches data input to the terminal D1 in response to the clock signal CPCLK input to the control terminal C1, and also latches the input data for the terminal D2 in response to the clock signal SCLK1 input to the terminal C2. To an input terminal D1 of the latch circuit 14 is connected the output terminal Y of the latch circuit 13 so as to latch the data in response to the clock signal SCLK2 input to the terminal C1. To an input terminal D1 of the latch circuit 15 is connected the output terminal Y of the latch circuit 13 so as to latch the data in response to the clock signal UPCLK input to the terminal C1.

A description will now be given of the path of test data in each of the operations (1) CAPTURE, (2) SHIFT and (3) UPDATE and the normal operation in the above

test circuit device, with reference to Figs. 18B, 18C, 18D and 19. The thick solid lines in Figs. 18B, 18C and 18D denote data transmission paths. The hatched portions in Fig. 19 represent arbitrary conditions.

(1) CAPTURE

Referring to Figs. 18B and 19, the selector circuit 12 selects the input terminal D1 in response to the control signal LT (low level) from the control circuit 8, whereby the signal from the data input terminal D1 is transmitted to the data output terminal DO. Then, the latch circuit 13 captures the data of the input terminal DI (i.e., the output data of the selector circuit 12 connected to this) in response to the capture clock CPCLK. The shift clock SCLK2 is then applied to the input terminal C1 of the latch circuit 14. In response to this clock SCLK2, the data latched in the latch circuit 13 is transmitted to the latch circuit 14.

(2) SHIFT

Referring to Figs. 18C and 19, the non-overlapped clocks SCLK1 and SCLK2 of two phases cause the shift operation from the scan input terminal S1 to the scan output terminal S0. By this operation, the data captured in the latch circuits 13 and 14 in CAPTURE is shifted-out. Further, serial data is externally shifted-in the chip 5 and is held in the latch circuit 13.

(3) UPDATE

Referring to Figs. 18D and 19, the data shifted-in from the scan input terminal SI in response to the non-overlapped shift clocks SCLK1 and SCLK2 of two phases are held in the latch circuit 13 and the latch circuit 14. In order to output the shifted-in data SI from the data output terminal DO, the control circuit 8 sets the control signal LT at a high level. The selector circuit 12 responds to this control signal LT at the high level to select the input D2. Accordingly, the data held in the latch circuit 15 is output to the data output terminal DO. Then, the control circuit 8 applies the data output clock UPCLK to the terminal C1 of the latch circuit 15. The latch 15 responds to this data output clock UPCLK to capture the data held in the latch circuit 13 and updates the data.

The normal operation is basically the same as the operation in the sample test, and the signal LT is always set at the low level. However, CAPTURE and SHIFT are not carried out, so that SCLK1, SCLK2, CPCLK, UPCLK, and signals at the terminals SI and SO are set at fixed values. In Fig. 19, SCLK1, SCLK2, and CPCLK are fixed at the low level, and UPCLK is fixed at the high level. Accordingly, the selector circuit 12 can be maintained at a state in which the terminal D1 is selected, and thus the signal input to the shift-in terminal SI will not exert any influence on the transmission of the data from the data input terminal DI to the data output terminal DO.

Fig. 20A is a circuit diagram showing another manner of the above-mentioned boundary scan register. Referring to Fig. 20A, input terminals as well as components thereof are the same as those in Fig. 18A, except for connections thereof. Although, in Fig. 18A, the input of the latch circuit 13 is connected to the output terminal of the selector circuit 12, the boundary scan register shown in Fig. 20A is designed to connect the input terminal of the latch circuit 13 to the data input terminal DI directly without going through the selector circuit 12.

Figs. 20B, 20C and 20D show the paths of test data, and Fig. 21 is a timing chart showing the operation in Fig. 20A.

The operation of this boundary scan register is the same at that in Fig. 18A except for the fact that the selector circuit 12 may be arbitrarily selected in the capturing operation. The boundary scan register 7 shown in Fig. 20A has the following advantages with respect to the test of the test circuit itself. That is; by the shift operation (shift test), it is possible to test a path between the scan input terminal SI and the scan output terminal SO (together with the shift functions of the latch circuits 13 and 14). Further, it is possible to confirm the bus from the data input terminal DI to the latch circuit 13 and the latch function of the latch circuit 13 by virtue of the capture operation. It is also possible by the update operation to confirm the bus from the output terminal Y of the latch circuit 13 to the latch circuit 15 and the bus therefrom to the data output terminal D0 through the selector circuit 12 as well as the functions of the selector circuit 12 and the latch circuit 15.

By a series of these operations, the boundary scan register 7 can be tested.

However, in the capture operation of the boundary scan register 7 shown in Fig. 18B, the data to be latched is transmitted to the output terminal D0 without any change at the same time as the data is latched in the latch circuit 13. If the boundary scan register 7 is connected to an output buffer 9', this capture operation causes simultaneous changes of the many output buffers 9'. The simultaneous changes of the output buffers cause a noise due to fluctuation of a source voltage, resulting in capturing of error data.

The boundary scan register in Fig. 20A can carry out the circuit test of the boundary scan register itself. However, a circuit test cannot be carried out at the path from the data input terminal DI to the input terminal D1 of the selector circuit 12. That is; it is impossible to test the path through which normal data (system data) is transmitted in the normal operation. Therefore, this path test can be carried out only by operating the whole chips in the system. The checking of this path is however, important, and thus, the insertion of this test circuit should not reduce a failure detectability.

SUMMARY OF THE INVENTION

The present invention is intended as a solution to the problems just outlined.

A boundary scan semiconductor integrated circuit, a circuit board incorporating a plurality of such semiconductor integrated circuits, and methods of testing such semiconductor integrated circuits and their interconnection on a circuit board, each in accordance with the present invention, are defined in the claims appended to the description.

Unlike the conventional examples, the data selected by the selector circuit is applied to a data output circuit. The applied data is not output untila data output clock signal is applied to the data output circuit. This prevents simultaneous changes of a plurality of output buffers connected to the adjacent succeeding registers, and thus prevents the capture of erroneous data.

In addition, since the data transmitted from the data input terminal means or the circuit block is applied to the capture latch circuit after selection by the selector circuit, the checking of the data captured by the capture latch circuit enables the checking of the path from the data input terminal or the circuit block to the selector circuit.

The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings given by way of example.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a control circuit for use in embodiments of the invention;
Fig. 2 is a diagram showing a sequence of a control circuit in Fig. 1;
Figs. 3 (a) - (ℓ) are circuit diagrams showing details of test access port controllers;
Fig. 4 is a circuit diagram of an instruction register;
Fig. 5 is a circuit diagram of a bypass register;
Fig. 6A is a circuit diagram showing details of a boundary scan register according to a first embodiment of the invention;
Figs. 6B, 6C and 6D are diagrams showing test data paths of Fig. 6A;
Fig. 7 is a circuit diagram showing details of a selector circuit;
Fig. 8 is a circuit diagram showing details of a latch circuit having two inputs;
Fig. 9 is a circuit diagram showing details of a latch circuit having one input;
Fig. 10 is a timing chart of the boundary scan register shown in Fig. 6;
Fig. 11 is a circuit diagram showing a second embodiment;
Fig. 12 is a timing chart of the embodiment of Fig. 11;
Figs. 13 and 14 are circuit diagrams showing embodiments which are variants of the first embodiment;
Fig. 15 is a diagram showing a board experimentally designed by a boundary scan design;
Fig. 16 is a block diagram showing details of a chip;
Figs. 17A, 17B and 17C are block diagrams showing three types of tests by a boundary scan register;
Figs. 18A and 20A are block diagrams of conventional boundary scan registers;
Figs. 18B, 18C and 18D are diagrams showing test data paths of Fig. 18A;
Figs. 20B, 20C and 20D are diagrams showing test data paths of Fig. 20A; and
Figs. 19 and 21 are timing charts of boundary scan registers in Figs. 18A and 20A, respectively.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a test circuit device (a boundary scan semiconductor integrated circuit) according to the invention will be described in detail hereinafter with reference to the accompanying drawings. The test circuit device according to the invention differs from those of the conventional art in boundary scan registers and a control circuit 8, and they are the same in other respects.

Fig. 1 is a block diagram showing details of a control circuit 8 for use in the test circuit device according to the invention. Referring to Fig. 1, the control circuit 8 receives through test access port TAP test data TDI, a test mode select signal TMS and a test clock TCK. The test data TDI is applied to a scan output terminal SO, a bypass register 8a and an instruction register 8b. The test mode select signal TMS and the test clock TCK are applied to a test access port controller 8c (which will be called a "TAP controller" hereinafter). The TAP controller 8c generates signals LT, SCLK1, SCLK2, CPCLK and UPCLK for controlling boundary scan registers 7, and also generates signals ISCLK1 and ISCLK2, a capture clock ICPCLK and a data output clock IUPCLK which are readable by the instruction register 8. Thus, the TAP controller 8c is a state-transition machine, by which the same state as the sequence defined by IEEE Std. 1149.1-1990 is formed by the test mode select signal TMS and the test clock TCK (see Fig. 2). The instruction register 8b responds to the clocks ISCLK1, ISCLK2, ICPCLK and IUPCLK to apply the test data TDI to a multiplexer 8d and a decoder 8e. The decoder 8e decodes data (instruction) from the instruction register 8b, and applies a signal at a high level to an input terminal T of the above TAP controller when it determines as an internal test or an external test. The decoder 8e further responds to the instruction from the instruction register 8b to control a multiplexer 8f. The TAP controller 8c responds to the signal at the high level applied to the input terminal T from the decoder 8e to generate a signal for

controlling each boundary scan register 7. Said multiplexer 8f receives test data from the bypass register 8a and data input to a scan input terminal SI through a shift pass. The multiplexer 8f responds to the control signal from the decoder 8e to select either one of the signals and apply the selected data to the multiplexer 8d. The multiplexer 8d responds to the control signal from the TAP controller 8c to select either one the data from the multiplexer 8f or the data from the instruction register 8b and apply the selector signal to a latch 8g. The latch 8g responds to the test clock TCK from the TAP controller 8c to apply the data from the multiplexer 8d to a test output terminal TDO.

Fig. 2 shows a sequence of the control circuit in the above Fig. 1. This sequence is the same as that described in IEEE Std. 1149.1-1990. This sequence shows the following states:

Test-Logic-Reset

A state in which a test logic is disabled, and a normal operation of a system logic is enabled.

Run-Test Idle

A basic state during execution of the test. A particular instruction can be executed at an intermediate state during a scan operation.

Select-DR-Scan

A scan sequence of the test data registers (boundary scan registers and a bypass register) are initialized.

Select-IR-Scan

A scan sequence of the instruction register is initialized.

Capture-DR

A basic state for capturing a response. Data is loaded in parallel in the test data register selected by an instruction of an execution length.

Shift-DR

The test data registers are connected in a shift state between the shift data input port TDI and the test data output port TDO, and the data is shifted one by one toward the data output port TDO every time when the shift clock TCK is raised.

Exit1-DR

The scan is terminated.

Pause-DR

The shift operation of the test data register at the serial pass between the test data input port TDI and the test data output port TDO is paused.

Ext2-DR

The scan is terminated.

Update-DR

The data is latched to the parallel outputs of the test register group from the shift register pass.

Capture-IR

A fixed pattern is captured in the instruction register.

Shift-IR

The instruction register is connected between the test data input port TDI and the test data output port TDO, and the data is shifted toward the test data output port TDO every time when the test clock TCK is raised.

Exit1-IR

The scan is terminated.

Pause-IR

The shift operation of the instruction register at the serial pass between the test data input port TDI and the test data output port TDO is paused.

Exit2-IR

The scan is terminated.

Update-IR

A new instruction is loaded in the instruction register. The instruction shifted in the instruction register is latched, and is output in parallel. After the completion of the latching, the execution of the instruction starts.

Said TAP controller 8c is illustrated in detail in Figs. 3 (a) - (ℓ). Referring to these figures, a circuit in Fig. 3 (a) and a circuit in Fig. 3(b) form a loop, and an output in Fig. 3(b) is applied to circuits in Figs. 3(d) - (l). Signals C1 and C2 applied to the circuit in Fig. 3(b) are formed by inverters, delay circuits and gates. More specifically, a plurality of gate circuit shown in Fig. 3(a) receive the test mode select signal TMS a well as output signals $\overline{A}$, A, $\overline{B}$, B, $\overline{C}$, C, $\overline{D}$, D from a plurality of latch circuits shown in Fig. 3(b). These signals are combined together by a plurality of AND gates to obtain predetermined output signals NA, NB, NC and ND. The circuit shown in Fig.

3(b) receives the signals NA, NB, NC and ND input from the circuit shown in Fig. 3 and the signals C1 and C2 formed by the circuit shown in Fig. 3(c). The latch circuits form signals including AL, $\overline{AL}$, A, $\overline{A}$, BL, $\overline{BL}$, B, $\overline{B}$, CL, $\overline{CL}$, C, $\overline{C}$, DL, $\overline{DL}$, D, $\overline{D}$ in response to these signals. The circuit in Fig. 3(d) is a circuit for generating a signal which attains a high level at the internal test and the external test applied from the decoder 8e. In response to the input signals T, A, $\overline{B}$, C, and $\overline{D}$, it generates the signal LT for controlling the selector circuit 12. The circuits described below and shown in Figs. 3(e) - (ℓ) generate the select signal LT, clock signals SCLK1, CPCLK, UPCLK, SCLK2, ISCLK1, ISCLK2, ICPLCK2, ICPCLK and IUPCLK to be applied to the boundary register 7 and the instruction register 8b.

Fig. 4 is a circuit diagram showing details of said instruction register. Referring to Fig. 4, the instruction register 8b includes a latch circuit 8L1 having two inputs, a latch circuit 8L2 having one input and a latch circuit 8L3 having one input. Operations of these circuits are as follows. A state-maintaining code is applied from the system to the data input D1 of the latch circuit 8L1, which applies the state-maintaining code to the latch circuit 8L3 in response to the capture clock ICPCLK1. Then, the data output clock IUPCLK is applied to the terminal T of the latch circuit 8L3. Accordingly, the state-maintaining code from the system is output through the output terminal D0 to the multiplexer 8f. The test data TDI is applied to the data input D2 of the latch circuit 8L1. In response to the incoming of the shift clocks ISCLK1 and ISCLK2, the test data TDI is shifted from the latch circuit 8L1 to the latch circuit 8L2, and the shifted test data TDI is output through the scan output terminal SO to the decoder 8ℓ, and is further output therefrom to the multiplexer 8f.

Fig. 5 is a circuit diagram showing details of said bypass register. Referring to Fig. 5, the bypass register 8a includes a latch circuit 8L4 and a latch circuit 8L5. The latch circuit 8L4 receives at a data input D the test data TDI. The latch circuit 8L4 responds to the shift clock SCLK1 applied from the TAP controller 8c to apply the received test data TDI to the latch circuit 8L5. The latch circuit 8L5 responds to the shift clock SCLK2 input to a clock terminal T to output the data latched therein from a scan output terminal SO. The output data is applied to the multiplexer 8f.

Fig. 6A is a block diagram of a boundary scan register. Referring to Fig. 6A, this boundary scan register includes, like the boundary scan register shown in Fig. 18A, a selector circuit 12, a 2-input latch circuit 13, a latch circuit 14 and a latch circuit 15. The connections between the respective circuits are different as follows:

(1) the data input D2 of the selector circuit 12 is not connected to the output terminal Y of the latch circuit 15 but to the output terminal Y of the 2-input latch circuit 13.

(2) the output terminal Y of the selector circuit 12 is not connected to the data output terminal DO but to a data input DI of the latch circuit 15 and a data input D1 of the 2-input latch circuit 13.

(3) the output terminal Y of the latch circuit 15 is not connected to the data input D2 of the selector circuit 12 but to the data output terminal DO.

Given such connections, each of the circuits of Fig. 6A handles data in the following manner. The selector circuit 12 responds to a control signal LT to select either data from the data input terminal DI (data from the system data terminal 9 or data from the circuit block 6) or test data from the 2-input latch circuit 13 and then applies the selected data to the 2-input latch circuit 13 and the latch circuit 15. The 2-input latch circuit 13 responds to the clock CPCLK to latch data transmitted from the selector circuit 12 to apply the latched data to the latch circuit 14 and the data input D2 of the selector circuit 12. The 2-input latch circuit 13 responds to the clock SCLK1 to latch test data transmitted from a scan-in terminal SI and to apply the latched data to the latch circuit 14 and the data input D2 of the selector circuit 12. The latch circuit 14 responds to the clock SCLK2 to latch data transmitted from the 2-input latch circuit 13 to apply the latched data to a scan-output terminal SO. The latch circuit 15 responds to the clock UPCLK to apply test data transmitted from the selector circuit 12 to the data output terminal DO.

Figs. 6B, 6C and 6D are diagrams showing data paths in a capture operation, shift operation and update operation of the boundary scan register of Fig. 6A, respectively.

Referring to Fig. 6B, in the capture operation, the selector circuit 12 responds to a control signal LT at the low level to select a data input D1; the 2-input latch circuit 13 responds to the clock CPCLK to latch the data to be applied to the data input D1; and the latch circuit 14 responds to the clock SCLK2 to latch data. A path for capture is established from the data input terminal DI to the scan output terminal SO.

Referring to Fig. 6C, in the shift operation, the 2-input latch circuit 13 responds to the clock SCLK1 to latch test data to be applied to the data input D2, and the latch circuit 14 responds to the clock SCLK2 to latch data to be applied to the data input DI. A path for shifting is thus established from the scan input terminal SI to the scan output terminal SO.

Referring to Fig. 6D, in the update operation, the selector circuit 12 responds to a control signal LT at the high level to select the data input D2, and the latch circuit 15 responds to the clock UPCLK to latch test data to be applied to the data input DI. A path for data output is thuus established from the outpu Y of the latch circuit 13 to the data output terminal DO. The data latched in the latch circuit 13 is applied to the circuit block 6 or the system data terminal 9 through this data output path by the shift operation.

As has been described heretofore, in this boundary

scan register, since the latch circuit 15 is connected between the output Y of the selector circuit 12 and the data output terminal DO, no data is directly applied to the output buffers 9' in the capture operation. Accordingly, no error is produced in data due to simultaneous changes of the plurality of output buffers 9'.

Moreover, since the data captured by the 2-input latch circuit 13 is transmitted through the path established from the system or block data input terminal DI to the output terminal Y of the selector circuit 12, this path can be checked on the basis of the captured data. This makes it possible to check all the data transmission paths as well as a test path.

Fig. 7 is a circuit diagram showing details of the selector circuit 12 shown in Fig. 6. Referring to Fig. 7, the signals input to the data input terminal D1 and D2 are inverted by inverters 30 and 31 and then applied to transfer gates 32 and 33, respectively. The signals applied to these transfer gates are selected by the control signals LT which are applied to a selector terminal SEL, and are inverted and not inverted. The selected signal is output after inversion by an inverter 35. Therefore, if the signal at the high level is applied to the clock input terminal C1 of the latch circuit 15 in the normal operation, then the latch circuit 15 can serve as a mere non-inversion driver (buffer) from the input terminal DI to the output terminal Y.

Fig. 8 is a circuit diagram showing details of said latch circuit 13 having two inputs. Referring to Fig. 8, an n-channel MOSFET 36 responds to the clock signal from the clock input terminal C1 to become conductive and apply the data input from the data input terminal D1 to a flipflop composed of an inverter 38 and an inverter 39. To the input side of this flipflop, an n-channel MOSFET 37 is connected as well as the n-channel MOSFET 36. The MOSFET 37 responds to the clock signal applied to the clock input terminal C2 to become conductive and apply the data input from the data input terminal D2 to the flip-flop. To the output side of the flip-flop is connected an inverter 40, which outputs the input data without inverting the same. Thus, the latching of the data is executed by applying the clock signal to the terminal C1 or C2 and controlling the n-channel transfer gates 36 and 37. Therefore, in the latch circuit having two inputs, the control signals SCLK1 and SCLK2, which are not overlapped with each other, can be applied to the terminals C1 and C2 to suppress contention of the data, respectively.

Fig. 9 is a circuit diagram showing details of each of the latch circuits 14 and 15. Referring to Fig. 9, the illustrated circuit is of a ratio type having one input, i.e., the clock signal input terminal C1, for receiving a signal, by which the data input in the data input terminal D1 is applied through an n-channel MOSFET 41 to a flip-flop composed of inverters 42 and 43. Accordingly, the input data is held. Thus, the latching of the data is executed by applying the clock signal to the clock input terminal C1 and controlling the n-channel MOSFET 41.

Three types of the test functions, i.e., CAPTURE, SHIFT, UPDATE, at the internal test, external test and sample test in the test circuit device having said structures will be described below. In the description of these operations, reference is made to a timing chart in Fig. 10, wherein hatched portions indicate arbitrary condition.

[I] Internal Test

(1) CAPTURE

The selector circuit 12 responds to the control signal LT (low level) from the control circuit 8 to select the data input DI. The signal input through the data input terminal DI is applied from the output terminal Y of the selector circuit to the latch circuit 15 and the latch circuit 13. At this time, since the data output clock UPCLK is not applied to the clock input terminal CI of the latch circuit 15, the output state at the data output terminal DO remains unchanged as previous state. Then, by applying the capture clock CPCLK from the control circuit 8 to the clock input terminal C1 of the latch circuit 13, the data at the input terminal D1 of the latch circuit 13 (i.e., the output terminal of the selector circuit 12 connected thereto) is captured. Then, by applying the shift clock SCLK2 to the clock input terminal CI of the latch circuit 14, the data latched in the latch circuit 13 is transmitted to the latch circuit 14.

(2) SHIFT

The control circuit 8 applies the non-overlapped clocks SCLK1 and SCLK2 of two phases to the clock input terminal C1 of the latch circuit 13 and the clock input terminal CI of the latch circuit 14 to carry out the shift operation from the scan input terminal SI to the scan output terminal SO. In this operation, the data captured in the latch circuit 13 in CAPTURE is shifted-out, and external serial data of the chip 5 is shifted-in and held in the latch circuit 13.

(3) DATA OUTPUT

The data, which was shifted-in from the scan input terminal SI by the non-overlapped clocks SCLK1 and SCLK2 of two phases in the shift operation, is held in the latch circuit 13 and the latch circuit 14. For outputting the held data from the data output terminal DO, the control circuit 8 set the control signal LT at the high level. In response to this, the selector circuit 12 selects the data input D2. At this time, the data held in the latch circuit 15 is output at the data output terminal DO. Then, by applying the data output clock UPCLK to the clock input terminal CI of the latch circuit 15, the data held in the latch circuit 13 is captured in the latch circuit 15, and thus the data is updated.

[II] External Test

The input and output signals in the respective op-

erations (CAPTURE, SHIFT and DATA OUTPUT) are the same as those at the internal test described before.

[III] Sample test

(1) CAPTURE

In the sample operation, a transmission path for normal data is the same as that in the normal operation. Therefore, the control circuit sets the control signal LT at the low level, and sets the data output clock UPCLK at the high level. The selector circuit 12 selects the data input D1 in response to the control signal LT at the low level. Thus, the signal input through the data input terminal DI is transmitted through the latch circuit 15 to the data output terminal DO. Then, the control circuit applies the capture clock CPCLK to the clock input terminal C1 of the latch circuit 13. The data from the output terminal of the selector circuit 12 is captured by the latch circuit 13. By a series of these operations, the data can be transmitted from the data input terminal DI to the data output terminal DO, and the data can be held in the latch circuit 13. Since this capture operation is performed by the clocks, which are output at a timing different from that in the normal operation, no influence is exerted on the signals from the data input terminal DI to the data output terminal DO.

(2) SHIFT

The shift operation from the scan input terminal SI to the scan output terminal SO is carried out by the non-overlapped clocks SCLK1 and SCLK2 of two phases input from the control circuit 8. In this operation, the data which was captured in the latch circuit 13 at CAPTURE is shifted out.

(3) DATA OUTPUT

Since the sample operation is such an operation that the signal in the circuit during the normal operation is sampled at a given timing and is output from the chip by the shift operation, the update operation is not performed. Thus, the data output clock CPCLK is set at the high level and the data from the select circuit 12 is passed to the output terminal DO.

[IV] Normal Operation

The control circuit 8 sets the control signal LT, clock signals SCLK1, SCLK2, CPCLK and UPCLK at the low level, the selector circuit 12 selects the data input D1, and the latch circuits 13 and 14 stop the shift operations and function as data-through. Thus, the bus for transmitting the normal data is maintained, and no influence is exerted on the normal operation.

Fig. 11 is a block diagram showing another embodiment of the invention, and Fig. 12 is a timing chart illustrating an operation thereof. This embodiment differs from that in Fig. 6 in that the data from the data input terminal DI is captured and the capture operation is performed in a latch circuit 46. For the purpose of it, the latch circuit 46 has two inputs and is preceded by a latch circuit 45 which has one input. Input/output waveforms in connection with the respective functions (CAPTURE, SHIFT and UPDATE) in the operations for the respective tests (internal test, external test and sample test) in these circuits are illustrated in Fig. 12. Compared with Fig. 10, it is the same except for the fact that it does not require the clock SCLK2 in CAPTURE because the data is captured directly in the latch circuit 45.

Fig. 13 is a block diagram showing still another embodiment. Referring to Fig. 13, it differs from the first embodiment in that, instead of the latch circuit 15, an AND gate 47 is connected to the output terminal DO. In such a structure, the data from the latch circuit 13 can be used to control the externally applied data output clock UPCLK. That is; the data output from the latch circuit 13 is selected by the selector circuit 12 and is input to the AND gate 47. The AND gate 47 processes this data applied from the latch circuit 13 and the data output clock UPCLK by AND operation, which enables the controlling of the clock externally applied.

Fig. 14 shows a structure which employs, instead of the AND gate 47 in said Fig. 13, an OR gate 48 of which one input terminal is connected to an inverter 49. In this structure, the externally applied data output clock UPCLK can be controlled by the data of the latch circuit 13, similarly to the circuit in Fig. 13.

Although, in the embodiments described hereinabove, level-sensitive circuits using the clocks of two phases are exemplified as the latch circuits, latch circuits employing edge trigger may be used.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A boundary scan semiconductor integrated circuit comprising:

   a circuit block (6);
   a plurality of boundary scan registers (7(7i,7o)) connected serially to form a shift bus, which plurality includes input registers (7i) connected between said circuit block (6) and data input terminal means (9(9i), 9') for inputting system data, and also output registers (7o) connected between said circuit block (6) and data output terminal means (9',9(9o)) for outputting system data; and
   a control circuit (8), which is co-operative with said plurality of boundary scan registers (7), and which is responsive to input test signals

(TDI,TMS,TCK) for generating a selection control signal (LT), non-overlapping two-phase first and second shift clock signals (SCLK1, SCLK2), a capture clock signal (CPCLK), and a data output clock signal (UPCLK), for controlling operation of said plurality of boundary scan registers (7); wherein

each said boundary scan register (7) comprises:

(a) a shift-in latch circuit (13(37-40);45(41-44)) having:

a data input (D2;DI) connected to the shift output (SO) of the adjacent preceding boundary scan register (7) or, if the said boundary scan register (7) is first in series, the shift output (SO) of said control circuit (8);

a clock input (C2;CI) connected to said control circuit (8) to receive said first shift clock signal (SCLK1) to shift-in data applied to the data input (D2;DI) of the shift-in latch circuit (13 (37-40);45(41-44)); and
an output (Y);

(b) a selector circuit (12(30-35)) having first and second data inputs (D1,D2), a data output (Y) and a control input (SEL), of which the first data input (D1) is connected to either said data input terminal means (9 (9i), 9') or an output of said circuit block (6), and also said control input (SEL) is connected to said control circuit (8) to receive said selection control signal (LT) to select between data applied respectively to said first and second data inputs (D1,D2) of said selector circuit (12 (30-35));
(c) a capture latch circuit (13(36,38-40); 46 (36,38-40)) having a data input (D1), a data output (Y) and a clock input (C1), of which said data input (D1) is connected to the data output (Y) of said selector circuit (12 (30-35)), and also said clock input (C1) is connected to said control circuit (8) to receive said capture clock signal (CPCLK), to capture data selected by said selector circuit (12(30-35));
(d) a shift-out latch circuit (14(41-44); 46 (37-40)) having a data input (DI;D2), a data output (Y), and a clock input (CI;C2), of which said data input (DI,D2) is connected to the data output (Y) of said shift-in latch circuit (13(37-40); 45(41-44), said data output (Y) is connected to the shift input (SI) of the adjacent succeeding boundary scan register (7), or, if the said boundary scan register (7) is last in series, the shift input (SI) of said control circuit (8), and also said clock input (CI;C2) is connected to said control circuit (8) to receive said second shift-clock signal (SCLK2), to shift out data shifted into said shift-in latch circuit (13 (37-40); 45(41-44)) and
(e) a data output circuit (15(41-44); 47; 48 & 49) having first and second inputs (DI,CI) and a data output (Y) of which the second input (CI) is connected to said control circuit (8) to receive said data output clock signal (UPCLK);

which semiconductor integrated circuit is characterised in that:

(i) the second data input (D2) of said selector circuit (12(30-35)) is connected to the output terminal (Y) of the shift-in latch circuit (13 (37-40); 45(41-44));
(ii) the data output (Y) of said selector circuit (12(30-35)) is also connected to the first input (DI) of said data output circuit (15(41-44); 47; 48 & 49); and
(iii) the data output (Y) of said data output circuit (15(41-44); 47; 48 & 49) is connected to either an input of said circuit block (6) or said data output terminal means (9',9(9o).

2. A semiconductor integrated circuit according to claim 1, wherein

said shift-in latch circuit (13(37-40)) and said capture latch circuit (13(36,38-40)) are comprised by a dual-input latch circuit (13) having: a first data input (D1) connected to the output (Y) of said selector circuit (12); a second data input (D2) connected to the shift output (50) of the adjacent preceding boundary scan register (7) or, if the said boundary scan register (7) is first in series, the shift output (50) of said control circuit (8), a first clock input (C1) connected to said control circuit (8) to receive said captive clock signal (CPCLK); a second clock input (C2) connected to said control circuit (8) to receive said first shift clock signal (SCLK1); and an output (Y) connected to the second data input (D2) of said selector circuit (12) and to the data input of said shift-out latch circuit (14).

3. A semiconductor integrated circuit according to claim 1, wherein:

said capture latch circuit (46(36,38-40)) and said shift-out latch circuit (46,(37-40)) are comprised by a dual-input latch circuit (46) having:

a first data input (D1) connected to the output (Y) of said selector circuit (12); a second data input (D2) connected to the output (Y) of said shift-in latch circuit (45); a first clock input (C1) connected to said control circuit (8) to receive said capture clock signal (CPCLK); a second clock input (C2) connected to said control circuit (8) to receive said second shift-clock signal (SCLK2); and an output (Y) connected to the shift input (SF) of the adjacent succeeding boundary scan register (7), or, if the said boundary scan register (7) is last in series, the shift input (SF) if said control circuit (8).

4. A semiconductor integrated circuit according to any preceding claim, wherein

said control circuit (8) includes and instruction register (8b), decoding means (8e) for decoding the contents of said instruction register (8b), and test access port controlling means (8c) for varying the control signals (LT, CPCLK, SCLK1, SCLK2, UPCLK) to be applied to said plurality of boundary scan registers (7) in response to inputting signals (TDI, TMS, TCK).

5. A semiconductor integrated circuit according to claim 4, wherein

said test access port controlling means (8c) comprises means for generating the selection control signal (LT), the data output clock signal (UPCLK), the capture clock signal (CPCLK) and the non-overlapping two-phase first and second shift clock signals (SCLK1, SCLK2), to apply the selection control signal (LT), the data output clock signal (UPCLK) and the capture clock signal (CPCLK) to said boundary scan registers (7) and then apply the second shift clock signal (SCLK2) to said boundary scan registers (7) in a case (i) where the contents of the input test signals (TDI, TMS, TCK) are a sample test, and to apply only the selection control signal (LT) and said data output clock signal (UPCLK) to all of said plurality of boundary scan registers (7) in a case (ii) where the contents of the input test signals (TD1, TMS, TCK) are a test of a path through which system data is transmitted.

6. A semiconductor integrated circuit according to any preceding claim, wherein

said shift-in latch circuit (13(37-40); 45(41-44)) includes state storing means (38, 39; 42,43) for temporarily storing applied data, and gate means (37;41) responsive to said first shift clock signal (SCLK1) for applying data shifted from the adjacent preceding boundary scan register (7) or control circuit (8) to said state storing means (38,39; 42,43).

7. A semiconductor integrated circuit according to claim 6, wherein

said capture latch circuit (13;46) includes gate means (36) connected to the data output of said selector circuit (12) and responsive to the capture clock signal (CPCLK) for applying data selected by said selector circuit (12) to said state storing means (38,39) of said shift-in latch circuit (13;45).

8. A semiconductor integrated circuit according to any preceding claim, wherein

said shift-out latch circuit (14;46) includes state storing means (42,43;38,39) for temporarily storing applied data, and gate means (41;37) connected to said shift-in latch circuit (13;45) and responsive to said second shift clock signal (SCLK2) for applying data from said shift-in latch circuit (13;45) to said state storing means (42,43;38,39).

9. A semiconductor integrated circuit according to claims 1 or 2, wherein

said shift-in latch circuit (13,(37-40)) and said capture latch circuit (13(36,38-40)) include state storing means (38,39) in common for temporarily storing applied data, first gate means (36) connected to said selector circuit (12) and responsive to said capture clock signal (CPCLK) for applying data selected by said selector circuit (12) to said state storing means (38,39), and second gate means (37) connected to the shift output (50) to the adjacent preceding boundary scan register (7)or, if the said boundary scan register (7) is first in series, the shift output (50) of said control circuit (8) and responsive to said first shift clock signal (SCLK1) for applying data shifted from shift output (50) to said state storing means (38,39).

10. A semiconductor integrated circuit according to claims 1 to 3 wherein

said capture latch circuit (46,(36,38-40)) and said shift-out latch circuit (46,(37-40)) include state storing means (38,39) in common for temporarily storing applied data, first gate means (36) connected to said selector circuit (12) and response to said capture clock signal (CPCLK) for applying data selected by said selector circuit (12) to said state storing means (38,39),

and second gate means (37) connected to said shift-in latch circuit (45) and response to said second shift clock signal (SCLK2) for applying data shifted from said shift-in latch circuit (45) to said state storing means (38,39).

11. A semiconductor integrated circuit according to any preceding claim, wherein

said data output circuit (15) includes state storing means (42,43) for temporarily storing applied data, and gate means (41) connected to said selector circuit (12) and response to said data output clock signal (UPCLK) for applying data selected by said selector circuit (12) to said state storing means (42,43).

12. A semiconductor integrated circuit according to any preceding claim, wherein

said selector circuit (12) includes first signal inversion means (30) connected to said data input terminal means (9',9(9i)) or output of said circuit block (6), second signal inversion means (31) connected to the data output (Y) of said shift-in latch circuit (13), third signal inversion means (34) to receive the selection control signal (LT), respective gate means (32,33) responsive to an output of said third signal inversion means (34) for passing one of an output of said first signal inversion means (30) and an output of said second signal inversion means (31), and fourth signal inversion means (35) connected to the respective outputs of said respective gate means (32,33).

13. A semiconductor integrated circuit according to claim 2 or any claim depending directly or indirectly therefrom, wherein

said data output circuit (47) comprises means (47) for ANDing said data output clock signal (UPCLK) and data selected by said selector circuit (12).

14. A semiconductor integrated circuit according to claim 2 or any claim depending directly or indirectly therefrom, wherein

said data output circuit (48,49) comprises signal inversion means (49) to receive said data output clock signal (UPCLK), and means (48) for ORing an output of said signal inversion means (49) and data selected by said selector circuit (12).

15. A circuit board comprising:

a mounting board (1);
a plurality of semiconductor integrated circuits (5) each according to any preceding claim, surface mounted on said mounting board (1);
input/output terminals (2) for transmitting system data to and from said semiconductor integrated circuits (5);
system signal lines (10) connecting the input/output terminals (2) to the data input terminal means (9i) and data output terminal means (9o) of said plurality of semiconductor integrated circuits (5), and interconnecting the data output and input terminal means (9o,9i) of respective ones of said semiconductor integrated circuits (5);
scan input and output terminals (3,4); and
test signal lines (11) interconnecting the scan input terminal (3), the respective control circuit (8) of each said semiconductor integrated circuit (5), and the scan output terminal (4).

16. A method of testing the internal circuit integrity of the semiconductor integrated circuit of any preceding claim 1 to 14, which method comprises the following successive operations:

(a) a SHIFT operation in which test date is shifted into and held by the shift-in latch circuit (13;45) of a first boundary scan register (7i) on the input side of the circuit block (6);
(b) an UPDATE operation in which the test data held in said shift-in latch circuit (13;45) is input to said circuit block (6) via the data output circuit (15) of said first boundary scan register (7i);
(c) a CAPTURE operation in which result data, output by said circuit block (6) in response to input of said test data, is input into and captured by the capture latch circuit (13;46) of a second boundary scan register (7o) on the output side of the circuit block (6) and held in the shift-output latch circuit (14,46) of said second boundary scan register (7o); and
(d) a SHIFT operation in which the captured result data is shifted from said shift-out latch circuit (14;46) of said second boundary scan register (7o) onto the shift bus; which method is characterised in that:

in said UPDATE operation (b) the test data is routed from the shift-in latch circuit (13; 45) to the data output circuit (15) via the selector circuit (12) of said first boundary scan register (7i); and in said CAPTURE operation (c) the result data is routed from said circuit block (6) to said capture latch circuit (13;46) and said shift-out latch circuit (14;46) via the selector circuit (12) of said secondary boundary scan register

(7o) while transmission of the result data to data terminal output means (9',9(90)) is inhibited by operation of the data output circuit (15) of said second boundary scan register (7o) which is interposed in a path between the output (Y) of said selector circuit (12) of said second boundary scan register (7o) and said data output terminal means (9',9(90)).

17. A method of testing the external circuit integrity of the circuit board of claim 15, which method comprises the following successive operations:

(a) a SHIFT operation in which test data is shifted into and held by the shift-in latch circuit (13;45) of a first boundary scan register (7o) on the output side of a first semiconductor integrated circuit (5);
(b) an UPDATE operation in which the test data held in said shift-in latch circuit (13;45) is output to the data output terminal means (9',9(90)) of said first semiconductor integrated circuit (5) via the data output circuit (15) of said first boundary scan register (7o);
(c) a CAPTURE operation in which the test data output from said first semiconductor integrated circuit (5) is input via a system signal line (10) to the data input terminal means (9(9i),9') of a second boundary scan register (7i) on the input side of a second semiconductor integrated circuit (5), captured by the capture latch circuit (13;46) of said second boundary scan register (7i), and held in the shift-out latch circuit (14;46) thereof; and
(d) a SHIFT operation in which the test data is shifted from said shift-out latch circuit (14;46) of said second boundary scan register (7i) onto the shift bus thereof,

which method is characterised in that:

in said UPDATE operation (b) the test data is routed from the shift-in latch circuit (13;45) to the data output circuit (15) via the selector circuit (12) of said first boundary scan register (7o); and in said CAPTURE operation (c) the test data is routed from said data input terminal means (9(9i),9') to said capture latch circuit (13;46) and said shift-out latch circuit (14;46) via the selector circuit (12) of said second boundary scan register (7o) while transmission of the test data to the circuit block (6) of said second semiconductor integrated circuit (5) is inhibited by operation of the data output circuit (15) of said secondary boundary scan (7i) which is interposed in a path between the output (Y) of said selector circuit (12) of said second boundary scan register (7i) and said circuit block (6).

Patentansprüche

1. Integrierte Rand-Abtast-Halbleiterschaltung mit:

einem Schaltungsblock (6);
einer Mehrzahl von Rand-Abtastregistern (7 (7i,7o)), die zur Ausbildung eines Schiebebusses in Reihe geschaltet sind, wobei die Mehrzahl Eingaberegister (7i), die zwischen den Schaltungsblock (6) und eine Dateneingabe-Anschlußeinrichtung (9(9i), 9') geschaltet sind, zum Eingeben von Systemdaten und außerdem Ausgaberegister (7o), die zwischen den Schaltungsblock (6) und
eine Datenausgabe-Anschlußeinrichtung (9', 9 (9o)) geschaltet sind, zum Ausgeben von Systemdaten aufweist; und
einer Steuerschaltung (8), die mit der Mehrzahl von Rand-Abtastregistern (7) zusammenarbeitet, und die zum Erzeugen eines Auswahlsteuersignals (LT), nicht-überlappender zwei-phasiger erster und zweier Schiebetaktsignale (SCLK1, SCLK2), eines Erfassungstaktsignals (CPCLK) und eines Datenausgabetaktsignals (UPCLK) auf Eingabetestsignale (TDI, TMS, TCK) reagiert, zum Steuern eines Betriebes der Mehrzahl der Rand-Abtastregister (7); wobei

jedes der Rand-Abtastregister (7) aufweist:

(a) eine Schiebe-Ein-Verriegelungsschaltung (13(37-40); 45(41-44)) mit:

einem Dateneingang (D2; DI), der mit dem Schiebeausgang (SO) des benachbarten vorhergehenden Rand-Abtastregisters (7) oder, falls das Rand-Abtastregister (7) das erste in der Reihe ist, mit dem Schiebeausgang (SO) der Steuerschaltung (8) verbunden ist;
einem Takteingang (C2; CI), der mit der Steuerschaltung (8) zum Empfangen des ersten Schiebetaktsignals (SCLK1) zum Einschieben von an den Dateneingang (D2; DI) der Schiebe-Ein-Verriegelungsschaltung (13(37-40); 45(41-44)) angelegten Daten verbunden ist; und
einem Ausgang (Y);

(b) eine Auswahlschaltung (12(30-35)), die einen ersten und

einen zweiten Dateneingang (D1, D2) einen Datenausgang (Y) und

einen Steuereingang (SEL) aufweist, von denen der erste Dateneingang (D1) entweder mit der Dateneingang-Anschlußeinrichtung (9(9i), 9') oder einem Ausgang des Schaltungsblocks (6) verbunden ist, und von denen außerdem der Steuereingang (SEL) mit der Steuerschaltung (8) zum Empfangen des Auswahlsteuersignals (LT) zum Wählen zwischen den an den ersten bzw. den zweiten Dateneingang (D1, D2) der Auswahlschaltung (12 (30-35)) angelegten Daten verbunden ist;

(c) eine Erfassungs-Verriegelungsschaltung (13(36, 38-40); 46(36, 38-40)), die einen Dateneingang (D1), einen Datenausgang (Y) und einen Takteingang (C1) aufweist, von denen der Dateneingang (D1) mit dem Datenausgang (Y) der Auswahlschaltung (12(30-35)) verbunden ist, und von denen außerdem der Takteingang (C1) mit der Steuerschaltung (8) zum Empfangen des Erfassungstaktsignals (CPCLK) verbunden ist, zum Erfassen der Daten, die durch die Auswahlschaltung (12 (30-35)) ausgewählt sind;
(d) eine Schiebe-Aus-Verriegelungsschaltung (14(41-44); 46(37-40)), die einen Dateneingang (DI; D2), einen Datenausgang (Y) und einen Takteingang (CI; C2) aufweist, von denen der Dateneingang (DI, D2) mit dem Datenausgang (Y) der Schiebe-Ein-Verriegelungsschaltung (13(37-40); 45(41-44) verbunden, von denen der Datenausgang (Y) mit dem Schiebeeingang (SI) des benachbarten nachfolgenden Rand-Abtastregisters (7) oder, falls das Rand-Abtastregister (7) das letzte in der Reihe ist, mit dem Schiebeeingang (SI) der Steuerschaltung (8) verbunden ist, und von denen außerdem der Takteingang (CI; C2) mit der Steuerschaltung (8) zum Empfangen des zweiten Schiebetaktsignals (SCLK2) verbunden ist, zum Ausschieben der in die Schiebe-Ein-Verriegelungsschaltung (13(37-40); 45(41-44)) geschobenen Daten; und
(e) eine Daten-Ausgabeschaltung (15(41-44); 47; 48 & 49), die einen ersten und einen zweiten Eingang (DI, CI) und einen Datenausgang (Y) aufweist, von denen der zweite Eingang (CI) mit der Steuerschaltung (8) zum Empfangen des Datenausgabetaktsignals (UPCLK) verbunden ist;

wobei die integrierte Halbleiterschaltung dadurch gekennzeichnet ist, daß

(i) der zweite Dateneingang (D2) der Auswahlschaltung (12(30-35)) mit dem Ausgangsanschluß (Y) der Schiebe-Ein-Verriegelungsschaltung (13(37-40; 45 (41-44)) verbunden ist;

(ii) der Datenausgang (Y) der Auswahlschaltung (12(30-35)) außerdem mit dem ersten Eingang (DI) der Daten-Ausgabeschaltung (15(41-44); 47; 48 & 49) verbunden ist; und

(iii) der Datenausgang (Y) der Daten-Ausgabeschaltung (15(41-44); 47; 48 & 49) mit entweder einem Eingang des Schaltungsblockes (6) oder der Datenausgabe-Anschlußeinrichtung (9', 9(9o)) verbunden ist.

2. Integrierte Halbleiterschaltung nach Anspruch 1, bei der die Schiebe-Ein-Verriegelungsschaltung (13(37-40) und die Erfassungs-Verriegelungsschaltung (13(36, 38-40)) von einer Zwei-Eingänge-Verriegelungsschaltung (13) aufgewiesen werden, die aufweist:

einen ersten Dateneingang (D1), der mit dem Ausgang (Y) der Auswahlschaltung (12) verbunden ist; einen zweiten Dateneingang (D2), der mit dem Schiebeausgang (50) des benachbarten vorhergehenden Rand-Abtastregisters (7) oder, falls das Rand-Abtastregister (7) das erste in der Reihe ist, mit dem Schiebeausgang (50) der Steuerschaltung (8) verbunden ist, einen ersten Takteingang (C1), der mit der Steuerschaltung (8) zum Empfangen des Erfassungstaktsignals (CPCLK) verbunden ist; einen zweiten Takteingang (C2), der mit der Steuerschaltung (8) zum Empfangen des ersten Schiebetaktsignals (SCLK1) verbunden ist; und einen Ausgang (Y), der mit dem zweiten Dateneingang (D2) der Auswahlschaltung (12) und mit dem Dateneingang der Schiebe-Aus-Verriegelungsschaltung (14) verbunden ist.

3. Integrierte Halbleiterschaltung nach Anspruch 1, bei der: die Erfassungs-Verriegelungsschaltung (46 (36, 38-40)) und die Schiebe-Aus-Verriegelungsschaltung (46, (37-40)) von einer Zwei-Eingangs-Verriegelungsschaltung (46) aufgewiesen werden, die aufweist:

einen ersten Dateneingang (D1), der mit dem Ausgang (Y) der Auswahlschaltung (12) verbunden ist; einen zweiten Dateneingang (D2), der mit dem Ausgang (Y) der Schiebe-Ein-Verriegelungsschaltung (45) verbunden ist; einen ersten Takteingang (C1), der mit der Steuerschaltung (8) zum Empfangen des Erfassungstaktsignals (CPCLK) verbunden ist; einen zweiten Takteingang (C2), der mit der Steuerschaltung (8) zum Empfangen des zweiten Schiebetaktsignals (SCLK2) verbunden ist; und einen

Ausgang (Y), der mit dem Schiebeeingang (SF) des benachbarten vorhergehenden Rand-Abtastregisters (7) oder, falls das Rand-Abtastregister (7) das letzte in der Reihe ist, mit dem Schiebeeingang (SF) der Steuerschaltung (8) verbunden ist.

4. Integrierte Halbleiterschaltung nach irgendeinem vorhergehenden Anspruch, bei der

die Steuerschaltung (8) ein Befehlsregister (8b), eine Dekodiereinrichtung (8e) zum Dekodieren der Inhalte des Befehlsregisters (8b) und eine Testzugriffs-Eingabe/Ausgabe-Schnittstellen-Steuereinrichtung (8c) zum Varieren der Steuersignale (LT, CPCLK, SCLK1, SCLK2, UPCLK), die an die Mehrzahl der Rand-Abtastregister (7) anzulegen sind, als Reaktion auf die eingegebenen Signale (TDI, TMS, TCK) aufweist.

5. Integrierte Halbleiterschaltung nach Anspruch 4, bei der die Testzugriffs-Eingabe/Ausgabe-Schnittstellen-Steuereinrichtung (8c) eine Einrichtung zum Erzeugen des Auswahlsteuersignals (LT), des Datenausgabetaktsignales (UPCLK), des Erfassungstaktsignals (CPCLK) und der nicht-überlappenden zwei-phasigen ersten und zweiten Schiebetaktsignale (SCLK1, SCLK2) aufweist, zum Anlegen des Auswahlsteuersignals (LT), des Datenausgabetaktsignals (UPCLK) und des Erfassungstaktsignals (CPCLK) an die Rand-Abtastregister (7) und dann zum Anlegen des zweiten Schiebetaktsignals (SCLK2) an die Rand-Abtastregister (7) in einem Fall (i), in dem die Inhalte der Eingabetestsignale (TDI, TMS, TCK) ein Mustertest sind, und zum Anlegen von nur dem Auswahlsteuersignal (LT) und dem Datenausgabetaktsignal (UPCLK) an alle aus der Mehrzahl der Rand-Abtastregister (7) in einem Fall (ii), in dem die Inhalte der Eingabetestsignale (TDI, TMS, TCK) ein Test eines Pfades sind, durch welchen Systemdaten übertragen werden.

6. Integrierte Halbleiterschaltung nach irgendeinem vorhergehenden Anspruch, bei der

die Schiebe-Ein-Verriegelungsschaltung (13 (37-40); 45(41-44)) eine Zustandsspeichereinrichtung (38, 39; 42, 43) zum zeitweiligen Speichern angelegter Daten und eine Gattereinrichtung (37; 41), die auf das erste Schiebetaktsignal (SCLK1) reagiert, zum Anlegen der von dem benachbarten vorhergehenden Rand-Abtastregister (7) oder der Steuerschaltung (8) geschobenen Daten an die Zustandsspeichereinrichtung (38, 39; 42, 43) aufweist.

7. Integrierte Halbleiterschaltung nach Anspruch 6, bei der die Erfassungs-Verriegelungsschaltung (13; 46) eine Gattereinrichtung (36) aufweist, die mit dem Datenausgang der Auswahlschaltung (12) verbunden ist und auf das Erfassungstaktsignal (CPCLK) reagiert, zum Anlegen der durch die Auswahlschaltung (12) ausgewählten Daten an die Zustandsspeichereinrichtung (38, 39) der Schiebe-Ein-Verriegelungsschaltung (13; 45).

8. Integrierte Halbleiterschaltung nach irgendeinem vorhergehenden Anspruch, bei der

die Schiebe-Aus-Verriegelungsschaltung (14; 46) eine Zustandsspeichereinrichtung (42, 43; 38, 39) zum zeitweiligen Speichern angelegter Daten und eine Gattereinrichtung (41; 37), die mit der Schiebe-Ein-Verriegelungsschaltung (13; 45) verbunden ist und auf das zweite Schiebetaktsignal (SCLK2) reagiert, zum Anlegen von Daten von der Schiebe-Ein-Verriegelungsschaltung (13; 45) an die Zustandsspeichereinrichtung (42, 43; 38, 39) aufweist.

9. Integrierte Halbleiterschaltung nach Anspruch 1 oder 2, bei der

die Schiebe-Ein-Verriegelungsschaltung (13, (37-40)) und die Erfassungs-Verriegelungsschaltung (13 (36, 38-40)) eine Zustandsspeichereinrichtung (38, 39) gemeinsam zum zeitweiligen Speichern angelegter Daten, eine erste Gattereinrichtung (36), die mit der Auswahlschaltung (12) verbunden ist und die auf das Erfassungstaktsignal (CPCLK) reagiert, zum Anlegen von durch die Auswahlschaltung (12) ausgewählten Daten an die Zustandsspeichereinrichtung (38, 39) und eine zweite Gattereinrichtung (37) aufweist, die mit dem Schiebeausgang (50) des benachbarten vorhergehenden Rand-Abtastregisters (7) oder, falls das Rand-Abtastregister (7) das erste in der Reihe ist, mit dem Schiebeausgang (50) der Steuerschaltung (8) verbunden ist und die auf das erste Schiebetaktsignal (SLCK1) reagiert, zum Anlegen der von dem Schiebeausgang (50) geschobenen Daten an die Zustandsspeichereinrichtung (38, 39).

10. Integrierte Halbleiterschaltung nach den Ansprüchen 1 bis 3, bei der

die Erfassungs-Verriegelungsschaltung (46, (36, 38-40)) und die Schiebe-Aus-Verriegelungsschaltung (46, (37-40)) eine Zustandsspeichereinrichtung (38, 39) gemeinsam zum zeitweiligen Speichern angelegter Daten, eine erste Gattereinrichtung (36), die mit der Aus-

wahlschaltung (12) verbunden ist und auf das Erfassungstaktsignal (CPCLK) reagiert, zum Anlegen der durch die Auswahlschaltung (12) ausgewählten Daten an die Zustandsspeichereinrichtung (38, 39) und eine zweite Gattereinrichtung (37), die mit der Schiebe-Ein-Verriegelungsschaltung (45) verbunden ist und auf das zweite Schiebetaktsignal (SCLK2) reagiert, zum Anlegen der von der Schiebe-Ein-Verriegelungsschaltung geschobenen Daten an die Zustandsspeichereinrichtung (38, 39) aufweisen.

11. Integrierte Halbleiterschaltung nach irgendeinem vorhergehenden Anspruch, bei der

die Datenausgabeschaltung (15) eine Zustandsspeichereinrichtung (42, 43) zum zeitweiligen Speichern angelegter Daten und eine Gattereinrichtung (41), die mit der Auswahlschaltung (12) verbunden ist und auf das Datenausgabetaktsignal (UPCLK) reagiert, zum Anlegen der durch die Auswahlschaltung (12) ausgewählten Daten an die Zustandsspeichereinrichtung (42, 43) aufweist.

12. Integrierte Halbleiterschaltung nach irgendeinem vorhergehenden Anspruch, bei der

die Auswahlschaltung (12) eine erste Signalumkehrungseinrichtung (30), die mit der Daten-Eingang-Anschlußeinrichtung (9', 9(9i)) oder einem Ausgang des Schaltungsblocks (6) verbunden ist, eine zweite Signalumkehrungseinrichtung (31), die mit dem Datenausgang (Y) der Schiebe-Ein-Verriegelungsschaltung (13) verbunden ist, eine dritte Signalumkehrungseinrichtung (34) zum Empfangen des Auswahlsteuersignals (LT), entsprechende Gattereinrichtungen (32, 33), die auf eine Ausgabe der dritten Signalumkehrungseinrichtung (34) reagieren, zum Durchgeben entweder einer Ausgabe der ersten Signalumkehrungseinrichtung (30) oder einer Ausgabe der zweiten Signalumkehrungseinrichtung (31) und eine vierte Signalumkehrungseinrichtung (35), die mit den entsprechenden Ausgängen der entsprechenden Gattereinrichtungen (32, 33) verbunden ist, aufweist.

13. Integrierte Halbleiterschaltung nach Anspruch 2 oder irgendeinem Anspruch, der direkt oder indirekt von diesem abhängt, bei der

die Datenausgabeschaltung (47) eine Einrichtung (47) zum Ausführen eines UND des Datenausgabetaktsignals (UPCLK) und des durch die Auswahlschaltung (12) ausgewählten Wertes aufweist.

14. Integrierte Halbleiterschaltung nach Anspruch 2 oder irgendeinem Anspruch, der direkt oder indirekt von diesem abhängt, bei der

die Datenausgabeschaltung (48, 49) eine Signalumkehrungseinrichtung (49) zum Empfangen des Datenausgabetaktsignals (UPCLK) und eine Einrichtung zum Ausführen eines ODER einer Ausgabe der Signalumkehrungseinrichtung (49) und des durch die Auswahlschaltung (12) ausgewählten Wertes aufweist.

15. Platine, die aufweist:

eine Montageplatte (1);
eine Mehrzahl von integrierten Halbleiterschaltungen (5) nach irgendeinem vorhergehenden Anspruch, die auf der Montageplatte (1) oberflächenmontiert sind;
Eingabe/Ausgabe-Anschlüsse (2) zum Übertragen von Systemdaten zu den und von den integrierten Halbleiterschaltungen (5);
System-Signalleitungen (10), die die Eingabe/Ausgabe-Anschlüsse (2) mit den Dateneingabe-Anschlußeinrichtungen (9i) und den Datenausgabe-Anschlußeinrichtungen (9o) der Mehrzahl der integrierten Halbleiterschaltungen (5) verbinden, und die die Datenausgabe- und die Dateneingabe-Anschlußeinrichtungen (9o, 9i) von entsprechenden der integrierten Halbleiterschaltungen (5) verbinden;
einen Abtast-Eingabeanschluß und einen Abtast-Ausgabeanschluß (3, 4); und
Test-Signalleitungen (11), die den Abtast-Eingabeanschluß (3), die entsprechende Steuerschaltung (8) von jeder integrierten Halbleiterschaltung (5) und den Abtast-Ausgabeanschluß (4) verbinden.

16. Verfahren zum Testen der internen Schaltungsintegrität der integrierten Halbleiterschaltung nach einem der vorhergehenden Ansprüche 1 bis 14, wobei das Verfahren die folgenden aufeinanderfolgenden Betriebsabläufe aufweist:

(a) einen VERSCHIEBEN-Betriebsablauf, bei dem ein Testwert in die Schiebe-Ein-Verriegelungsschaltung (13; 45) eines ersten Rand-Abtastregisters (7i) auf der Eingangsseite des Schaltungsblockes (6) geschoben und durch dieses gehalten wird;
(b) einen AKTUALISIEREN-Betriebsablauf, bei dem der in der Schiebe-Ein-Verriegelungsschaltung (13; 45) gehaltene Testwert in den Schaltungsblock (6) über die Daten-Ausgabeschaltung (15) des ersten Rand-Abtastregi-

sters (7i) eingegeben wird;
(c) einen ERFASSEN-Betriebsablauf, bei dem ein Ergebniswert, der durch den Schaltungsblock (6) als Reaktion auf die Eingabe des Testwertes ausgegeben wird, in die Erfassungs-Verriegelungsschaltung (13; 46) eines zweiten Rand-Abtastregisters (7o) auf der Ausgangsseite des Schaltungsblocks (6) eingegeben und von diesem erfaßt und in der Schiebe-Ausgabe-Verriegelungsschaltung (14, 46) des zweiten Rand-Abtastregisters (7o) gehalten wird; und
(d) einen VERSCHIEBEN-Betriebsablauf, bei dem der erfaßte Ergebniswert von der Schiebe-Aus-Verriegelungsschaltung (14; 46) des zweiten Rand-Abtastregisters (7o) auf den Schiebebus geschoben wird; wobei das Verfahren dadurch gekennzeichnet ist, daß:

bei dem AKTUALISIEREN-Betriebsablauf (b) der Testwert von der Schiebe-Ein-Verriegelungsschaltung (13; 45) zu der Daten-Ausgabeschaltung (15) über die Auswahlschaltung (12) des ersten Rand-Abtastregisters (7i) geführt wird; und in dem ERFASSEN-Betriebsablauf (c) der Ergebniswert von dem Schaltungsblock (6) zu der Erfassungs-Verriegelungsschaltung (13; 46) und der Schiebe-Aus-Verriegelungsschaltung (14; 46) über die Auswahlschaltung (12) des zweiten Rand-Abtastregisters (7o) geführt wird, während die Übertragung des Ergebniswertes zu der Datenausgabe-Anschlußeinrichtung (9', 9 (90)) durch einen Betrieb der Daten-Ausgabeschaltung (15) des zweiten Rand-Abtastregisters (7o), die in einem Pfad zwischen dem Ausgang (Y) der Auswahlschaltung (12) des zweiten Rand-Abtastregisters (7o) und der Datenausgabe-Anschlußeinrichtung (9', 9(90)) dazwischengesetzt ist, unterbunden wird.

17. Verfahren zum Testen der externen Schaltungsintegrität der Platine nach Anspruch 15, wobei das Verfahren die folgenden aufeinanderfolgenden Betriebsabläufe aufweist:

(a) einen VERSCHIEBEN-Betriebsablauf, bei dem ein Testwert in die Schiebe-Ein-Verriegelungsschaltung (13; 45) eines ersten Rand-Abtastregisters (7o) auf der Ausgangsseite einer ersten integrierten Halbleiterschaltung (5) geschoben und darin gehalten wird;
(b) einen AKTUALISIEREN-Betriebsablauf, bei dem der in der Schiebe-Ein-Verriegelungsschaltung (13; 45) gehaltene Testwert an die Datenausgabe-Anschlußeinrichtung (9', 9(90)) der ersten integrierten Halbleiterschaltung (5) über die Daten-Ausgabeschaltung (15) des ersten Rand-Abtastregisters (7o) ausgegeben wird;
(c) einen ERFASSEN-Betriebsablauf, bei dem der von der ersten integrierten Halbleiterschaltung (5) ausgegebene Testwert über eine System-Signalleitung (10) in die Dateneingabe-Anschlußeinrichtung (9 (9i), 9') eines zweiten Rand-Abtastregisters (7i) auf der Eingangsseite einer zweiten integrierten Halbleiterschaltung (5) eingegeben, durch die Erfassungs-Verriegelungsschaltung (13; 46) des zweiten Rand-Abtastregisters (7i) erfaßt und in der Schiebe-Aus-Verriegelungsschaltung (14; 46) derselben gehalten wird; und
(d) einen VERSCHIEBEN-Betriebsablauf, bei dem der Testwert von der Schiebe-Aus-Verriegelungsschaltung (14; 46) des zweiten Rand-Abtastregisters (7i) auf den Schiebebus desselben geschoben wird;
wobei das Verfahren dadurch gekennzeichnet ist, daß:
bei dem AKTUALISIEREN-Betriebsablauf (b) der Testwert von der Schiebe-Ein-Verriegelungsschaltung (13; 45) zu der Daten-Ausgabeschaltung (15) über die Auswahlschaltung (12) des ersten Rand-Abtastregisters (7o) geführt wird; und bei dem ERFASSEN-Betriebsablauf (c) der Testwert von der Dateneingabe-Anschlußeinrichtung (9 (9i), 9') zu der Erfassungs-Verriegelungsschaltung (13; 46) und der Schiebe-Aus-Verriegelungsschaltung (14; 46) über die Auswahlschaltung (12) des zweiten Rand-Abtastregisters (7o) geführt wird, während die Übertragung des Testwertes zu dem Schaltungsblock (6) der zweiten integrierten Halbleiterschaltung (5) durch einen Betrieb der der Daten-Ausgabeschaltung (15) des zweiten Rand-Abtastregisters (7i), die in einem Pfad zwischen dem Ausgang (Y) der Auswahlschaltung (12) des zweiten Rand-Abtastregisters (7i) und dem Schaltungsblock (6) dazwischengesetzt ist, unterbunden wird.

Revendications

1. Circuit intégré à semiconducteur d'exploration ou de balayage de jonctions comprenant :

un bloc de circuits (6) ;
une pluralité de registres d'exploration ou de balayage de jonctions (7(7i,7o)) reliés en série pour former un bus de décalage, laquelle pluralité comprend des registres d'entrée (7i) montés entre ledit bloc de circuit (6) et des moyens de bornes d'entrée de données (9(9i),9') pour

introduire des données de système, et également des registres de sortie (7o) montés entre ledit bloc de circuits (6) et les moyens de bornes de sortie de données (9',9(9o)) pour fournir des données de système ; et
un circuit de commande (8) qui est coopératif avec ladite pluralité de registres d'exploration de jonctions (7) et qui est sensible aux signaux de test d'entrée (TDI, TMS, TCK) pour engendrer un signal de commande de sélection (LT), des premier et second signaux d'horloge de décalage à deux phases(SCLK1,SCLK2) qui ne se chevauchent pas, un signal d'horloge de saisie ou d'interception (CPCLK) et un signal d'horloge de sortie de données (UPCLK), pour commander le fonctionnement de ladite pluralité de registre de balayage ou d'exploration de jonctions (7) ; dans lequel
chacun desdits registres de balayage ou d'exploration (7) comprend :

(a) un circuit à verrouillage d'introduction par décalage (13(37-40);45(41-44)) comprenant :

une entrée de données (D2;DI) reliée à une sortie de décalage (SO) du registre de balayage de jonctions précédent adjacent (7) ou, si ledit registre de balayage ou d'exploration de jonctions (7) est le premier dans la série, à la sortie de décalage (SO) dudit circuit de commande (8) ;
une entrée d'horloge (C2;CI) reliée audit circuit de commande (8) pour recevoir ledit premier signal d'horloge de décalage (SCLK1) pour introduire par décalage des données appliquées à l'entrée de données (DI;D2) du circuit à verrouillage d'introduction par décalage (13(37-40);45(41-44)); et
une sortie (Y) ;

(b) un circuit sélecteur (12(30-35)) ayant des première et seconde entrées de données (D1,D2), une sortie de données (Y) et une entrée de commande (SEL) parmi lesquelles la première entrée de données (D1) est reliée soit auxdits moyens de bornes d'entrée de données (9(9i),9') soit à une sortie dudit bloc de circuits (6), et ladite entrée de commande (SEL) est également reliée audit circuit de commande (8) pour recevoir ledit signal de commande de sélection (LT) pour sélectionner parmi les données appliquées respectivement auxdites première et seconde d'entrée de données (D1,D2) dudit circuit sélecteur (12(30-35)) ;
(c) un circuit de verrouillage de saisie et d'interception (13(36,38-40); 46(36,38-40)) ayant une entrée de données (D1), une sortie de données (Y) et une sortie d'horloge (C1) parmi lesquelles ladite entrée de données (D1) est reliée à la sortie de donnée (Y) dudit circuit sélecteur (12(30-35)), et également ladite entrée d'horloge (C1) est reliée audit circuit de commande (8) pour recevoir le signal d'horloge d'interception ou de saisie (CPCLK) pour intercepter les données sélectionnées par ledit circuit sélecteur (12(30-35));
(d) un circuit de verrouillage de sortie par décalage (14(41-44); 46(37-40)) comprenant une entrée de données (DI;D2), une sortie de données (Y) et une entrée d'horloge (CI;C2), desquelles ladite entrée de données (DI,D2) est reliée à la sortie de données (Y) dudit circuit à verrouillage d'introduction par décalage (13 (37-40); 45(41-44), ladite sortie de données (Y) est reliée à l'entrée de décalage (SI) du registre d'exploration ou de balayage de jonctions suivant adjacent (7) ou, si ledit registre de balayage de jonctions (7) est le dernier dans la série, à l'entrée de décalage (SI) dudit circuit de commande (8), et également ladite entrée d'horloge (CI;C2) est reliée audit circuit de commande (8) pour recevoir le second signal d'horloge de décalage (SCLK2), pour faire sortir par décalage des données introduites par décalage dans ledit circuit à verrouillage d'introduction par décalage (13(37-40); 45(41-44)) et
(e) un circuit de sortie de données (15(41-44); 47; 48 & 49) comprenant des première et seconde entrées (DI,CI) et une sortie de données (Y), desquelles la seconde entrée (CI) est reliée audit circuit de commande (8) pour recevoir ledit signal d'horloge de sortie de données (UPCLK) ;

lequel circuit intégré à semiconducteur est caractérisé en ce que :

(i) la seconde entrée de données (D2) dudit circuit sélecteur (12(30-35)) est reliée à la borne de sortie (Y) du circuit à verrouillage d'introduction par décalage (13(37-40); 45(41-44));
(ii) la sortie de données (Y) dudit circuit sélecteur (12(30-35)) est également reliée à ladite première entrée (DI) dudit circuit de sortie de données (15(41-44); 47; 48 & 49) ; et
(iii) la sortie de données (Y) dudit circuit de sortie de données (15(41-44); 47; 48 & 49) est reliée soit à une entrée dudit bloc de circuits (6) soit audit moyen de borne de sortie de données (9',9(9o).

2. Circuit intégré à semiconducteur selon la revendication 1, dans lequel

le circuit à verrouillage d'introduction par décalage précité (13(37-40)) et le circuit à ver-

rouillage d'interception précité (13(36,38-40)) sont formés par un circuit à verrouillage d'entrée duale (13) comprenant :
une première entrée de données (D1) reliée à la sortie (Y) du circuit sélecteur précité (12); une seconde entrée de données (D2) reliée à la sortie de décalage (50) du registre de balayage et d'exploration de jonctions précédent adjacent (7) ou, si ledit registre d'exploration de jonctions (7) est le premier dans la série, à la sortie de décalage (50) dudit circuit de commande (8), une première entrée d'horloge (C1) reliée audit circuit de commande (8) pour recevoir le signal d'horloge d'interception (CPCLK) ; une seconde entrée d'horloge (C2) reliée audit circuit de commande (8) pour recevoir ledit premier signal d'horloge de décalage (SCLK1) ; et une sortie (Y) reliée à la seconde entrée de données (D2) dudit circuit sélecteur (12) et à l'entrée de données du circuit à verrouillage de sortie par décalage précité (14).

3. Circuit intégré à semiconducteur selon la revendication 1, dans lequel :

le circuit de verrouillage d'interception précité (46(36,38-40)) et le circuit à verrouillage de sortie par décalage (46,(37-40)) sont formés par un circuit à verrouillage d'entrée duale par décalage (46) ayant :
une première entrée de données (D1) reliée à la sortie (Y) du circuit sélecteur précité (12) ; une seconde entrée de données (D2) reliée la sortie (Y) du circuit à verrouillage par introduction par décalage (45) ; une première entrée d'horloge (C1) reliée au circuit de commande (8) pour recevoir le signal d'horloge d'interception et de saisie précité (CPLCK) ; une seconde entrée d'horloge (C2) reliée audit circuit de commande (8) pour recevoir le second signal d'horloge de décalage précité (SCLK2) ; et une sortie (Y) reliée à l'entrée de décalage (SF) du registre d'exploration de jonctions suivant adjacent (7) ou, si le registre d'exploration de jonctions (7) est le dernier dans la série, à l'entrée de décalage (SF) dudit circuit de commande (8).

4. Circuit intégré à un semiconducteur selon l'une des revendications précédentes, dans lequel

le circuit de commande (8) comprend un registre d'instructions (8b), des moyens décodeurs (8e) pour décoder les contenus dudit registre d'instructions (8b), et des moyens de commande de bornes d'accès de tests (8c) pour faire varier les signaux de commande (LT, CPCLK, SCLK1, SCLK2, UPCLK) devant être appliqués à la pluralité précitée de registres d'exploration de jonctions (7) en réponse à des signaux d'introduction (TD1, TMS, TCK).

5. Circuit intégré à un semiconducteur selon la revendication 4, dans lequel

les moyens de commande de bornes d'accès de tests précités (8c) comprennent des moyens pour engendrer le signal de commande de la sélection (LT), le signal d'horloge de sortie de données (UPCLK), le signal d'horloge d'interférence (CPLCK) et les premier et second signaux d'horloge de décalage (SCLK1, SCLK2) qui ne se chevauchent pas, pour appliquer le signal de commande de sélection (LT), le signal d'horloge de sortie de données (UPCLK) et le signal d'horloge d'interception (CPLK) au registre de balayage ou d'exploration de jonctions (7) précité et appliquer ensuite le second signal d'horloge (SCLK2) auxdits registres de balayage de jonctions (7) dans un cas (i) où les contenus des signaux de test d'entrée (TDI, TMS, TCK) sont un test d'échantillons, et pour appliquer seulement le signal de commande de sélection (LT) et ledit signal d'horloge de sortie de données (UPCLK) à tous les registres de ladite pluralité de registre de balayage de jonctions (7) dans un cas (ii) où les contenus des signaux de test d'entrée (TD1, TMS, TCK) sont un test d'une voie à travers laquelle des données de système sont transmises.

6. Circuit intégré à semiconducteur selon l'une des revendications précédentes, dans lequel

le circuit à verrouillage d'introduction par décalage précité (13(37-40) ; 45(41-44)) comprend des moyens mémoire d'état (38, 39 ; 42,43) pour temporairement mémoriser les données appliquées, et des moyens de porte (37;41) sensibles au premier signal d'horloge de décalage précité (SCLK1) pour appliquer des données décalées du registre de balayage de jonctions précédent adjacent (7) ou du circuit de commande (8) au moyen mémoire d'état (38,39 ; 42,43).

7. Circuit intégré à semiconducteur selon la revendication 6, dans lequel

le circuit à verrouillage d'interception précité (13;46) comprend des moyens de porte (36) reliés à la sortie de données du circuit sélecteur précité (12) et répondant au signal d'horloge d'interception (CPCLK) pour appliquer les données sélectionnées par le circuit sélecteur pré-

cité (12) audit moyen mémoire d'état (38,39) dudit circuit à verrouillage d'introduction d'un décalage (13;45).

8. Circuit intégré à semiconducteur selon l'une des revendications précédentes, dans lequel

le circuit à verrouillage de sortie par décalage précité (14;46) comprend des moyens mémoire d'états (42,43;38,39) pour temporairement mémoriser les données appliquées, et des moyens de porte (41;37) reliés au circuit à verrouillage d'introduction par décalage (13; 45) et répondant audit second signal d'horloge de décalage précité (SCLK2) pour appliquer des données en provenance du circuit à verrouillage d'introduction par décalage précité (13;45) audit moyen de mémorisation d'états (42,43 ; 38,39).

9. Circuit intégré à semiconducteur selon l'une des revendications 1 ou 2, dans lequel

le circuit de verrouillage d'introduction par décalage précité (13(37-40)) et le circuit à verrouillage d'interception précité (13(36,38-40)) comprend des moyens de mémorisation d'états (38,39) en commun pour temporairement mémoriser les données appliquées, les premier moyens de porte (36) reliés au circuit sélecteur précité (12) et sensibles au signal d'horloge d'interception (CPCLK) pour appliquer des données sélectionnées par ledit circuit sélecteur (12) audit moyen de mémorisation d'états (38,39), et des second moyens de porte (37) reliés à la sortie de décalage (50) pour le registre de balayage de jonctions précité adjacent (7) ou, si ledit registre de balayage de jonctions (7) est le premier dans la série, à la sortie de décalage (50) du circuit de commande précité (8) et sensibles au premier signal d'horloge de décalage (SCLK1) pour appliquer les données décalées de la sortie de décalage (50) audit moyen mémoire d'états (38,39).

10. Circuit intégré à semiconducteur selon l'une des revendications 1 à 3, dans lequel

le circuit de verrouillage d'interception précité (46(36,38-40)) et le circuit à verrouillage de sortie par décalage précité (46,(37-40)) comprend des moyens mémoire d'états (38,39) en commun pour temporairement mémoriser les données appliquées, des premier moyens de porte (36) reliés au circuit sélecteur (12) et sensibles au signal d'horloge d'interception précité (CPCLK) pour appliquer les données sélectionnées par ledit circuit sélecteur (12) audit moyen mémoire d'états (38,39) et des second moyens de porte (37) reliés au circuit à verrouillage d'introduction par décalage précité (45) et sensibles au second signal d'horloge de décalage précité (SCLK2) pour appliquer les données décalées du circuit à verrouillage d'introduction par décalage précité (45) audit moyen mémoire d'états (38,39).

11. Circuit intégré à semiconducteur selon l'une des revendications précédentes, dans lequel

le circuit de sortie de données précité (15) comprend des moyens mémoire d'états (42,43) pour temporairement mémoriser les données appliquées, et des moyens de porte (41) reliés au circuit sélecteur précité (12) et sensibles au signal d'horloge de sortie de données (UPCLK) pour appliquer des données sélectionnées par le circuit sélecteur précité (12) au moyen mémoire d'états précité (42,43).

12. Circuit intégré à semiconducteur selon l'une des revendications précédentes, dans lequel

le circuit sélecteur précité (12) comprend des premier moyens d'inversion de signal (30) reliés au moyen de borne d'entrée de données précité (9',9(9i)) ou à la sortie du bloc de circuits précité (6), des second moyens d'inversion de signal (31) reliés à la sortie de données (Y) du circuit à verrouillage d'introduction par décalage précité (13), des troisième moyens d'inversion (34) pour recevoir le signal de commande de la sélection (LT), des moyens de porte respectifs (32,33) sensibles à une sortie desdits troisième moyens d'inversion de signal (34) pour faire passer l'une des sorties des premier moyens d'inversion de signal précités (30) et une sortie des second moyens d'inversion de signal (31), et des quatrième moyens d'inversion de signal (35) reliés aux sorties respectives des moyens de porte respectifs précités (32,33).

13. Circuit intégré à semiconducteur selon la revendication 2 ou une des revendications dépendant de celle-ci directement ou indirectement de celle-ci, dans lequel

le circuit de sortie de données précité (47) comprend des moyens (47) pour soumettre à une opération ET le signal d'horloge de sortie de données précité (UPCLK) et les données sélectionnées par le circuit sélecteur (12).

14. Circuit intégré à semiconducteur selon la revendi-

cation 2 ou l'une des revendications dépendant directement ou indirectement de celle-ci, dans lequel

le circuit de sortie de données (48,49) précité comprend des moyens d'inversion de signal (49) pour recevoir le signal d'horloge de sortie de données précité (UPCLK), et des moyens (48) pour soumettre à une opération OU une sortie desdits moyens d'inversion de signal (49) et les données sélectionnées par le circuit sélecteur précité (12).

15. Carte imprimée comprenant :

une plaque de montage (1);
une pluralité de circuits intégrés à semiconducteur (5) chacun selon l'une des revendications précédentes, et montés en surface sur ladite plaque de montage (1);
des bornes d'entrée/sortie (2) pour transmettre des données de système à et en provenance desdits circuits intégrés semiconducteurs (5);
des lignes de signaux de système (10) reliant les bornes d'entrée/sortie (2) aux moyens de borne d'entrée de sortie (9i) et des moyens de borne de sortie de données (9o) de ladite pluralité de circuits intégrés semiconducteurs (5), et interconnectant les moyens de sortie de données et les bornes d'entrée (9o,9i) de circuits intégrés semiconducteurs respectifs desdits circuits intégrés semiconducteurs (5);
des bornes d'entrée et de sortie d'exploration ou de balayage (3,4); et
des lignes de signaux de test (11) interconnectant la borne d'entrée d'exploration (3), le circuit de commande respectif (8) de chaque circuit intégré semiconducteur précité (5) et la borne de sortie de balayage ou d'exploration (4).

16. Procédé pour tester l'intégrité de circuit interne du circuit intégré à semiconducteur selon l'une des revendications précédentes 1 à 14, lequel procédé comprend les opérations successives suivantes :

(a) une opération de DECALAGE au cours duquel des données de test sont introduites par décalage et maintenues par le circuit à verrouillage d'introduction par décalage (13;45) d'un premier registre d'exploration de jonctions (7i) sur le côté d'entrée du bloc de circuits (6);
(b) une opération de MISE A JOUR au cours duquel les données de test maintenues dans ledit circuit à verrouillage d'introduction par décalage (13;45) sont introduites dans le bloc de circuits (6) via le circuit de sortie de données (15) dudit premier registre d'exploration de jonctions (7i);
(c) une opération de SAISIE au cours de laquelle des données de résultat, fournies par ledit bloc de circuits (6) en réponse à l'entrée des données de test précitées sont introduites dans et saisies par le circuit à verrouillage de saisie (13;46) d'un second registre d'exploration ou de balayage de jonctions (7o) sur le côté de sortie du bloc de circuits (6) et maintenues dans le circuit à verrouillage de sortie par décalage (14,46) dudit second registre d'exploration de jonctions (7o); et
(d) une opération de DECALAGE au cours de laquelle les données de résultat de saisie sont décalées du circuit à verrouillage de la sortie par décalage (14;46) dudit second registre d'exploration de jonctions (7o) sur le bus à décalage; ledit procédé est caractérisé en ce que :

au cours de ladite opération de MISE A JOUR (b) les données de test sont acheminées du circuit à verrouillage d'introduction par décalage (13;45) au circuit de sortie de données (15) via le circuit sélecteur (12) dudit premier registre d'exploration de jonctions (7i); et au cours de ladite opération de SAISIE (c) les données de résultat sont acheminées dudit bloc de circuits (6) audit circuit à verrouillage de saisie (13;46) et audit circuit à verrouillage de sortie par décalage (14;46) via le circuit sélecteur (12) dudit second registre de balayage de jonctions (70) pendant que la transmission de données de résultat au moyen de sortie de borne de données (9',9(90)) est inhibée par l'opération du circuit de sortie de données (15) dudit second registre de balayage de jonctions (7o) qui est interposé dans une voie entre la sortie (Y) dudit circuit sélecteur (12) du second registre de balayage de jonctions (7o) et lesdits moyens de borne de sortie de données (9', 9(90)).

17. Procédé pour tester l'intégrité des circuits externes de la carte imprimée selon la revendication 15, ledit procédé comprenant les opérations successives suivantes :

(a) une opération de DECALAGE au cours de laquelle des données de test sont introduites par décalage et maintenues par le circuit à verrouillage d'introduction par décalage (13;45) d'un premier registre d'exploration de jonctions (7o) sur le côté de sortie d'un premier circuit intégré à semiconducteur (5);
(b) une opération de MISE A JOUR au cours de laquelle les données de test maintenues

dans ledit circuit à verrouillage d'introduction par décalage (13;45) sont fournies aux moyens de borne de sortie de données (9',9(90)) dudit premier circuit intégré à semiconducteur (5) via le circuit de sortie de données (15) dudit premier registre d'exploration de jonctions (7o);

(c) une opération de SAISIE au cours de laquelle les données de test fournies par ledit premier circuit intégré à semiconducteur (5) sont appliquées via une ligne de signaux de système (10) aux moyens de borne d'entrée de données (9(9i),9') d'un second registre d'exploration de jonctions (7i) sur le côté d'entrée d'un second circuit intégré à semiconducteur (5), saisies par le circuit à verrouillage de saisie ou d'interception (13;46) dudit second registre de balayage ou d'exploration de jonctions (7i), et maintenues dans le circuit à verrouillage de sortie par décalage (14;46) de celui-ci; et

(d) une opération de DECALAGE au cours de laquelle les données de test sont décalées dudit circuit à verrouillage de sortie par décalage (14;46) dudit second registre d'exploration ou de balayage de jonctions (7i) sur le bus à décalage de celui-ci,

ledit procédé est caractérisé en ce que :

au cours de ladite opération de MISE A JOUR (b) les données de test sont acheminées du circuit à verrouillage d'introduction par décalage (13;45) au circuit de sortie de données (15) via le circuit sélecteur (12) dudit second registre de balayage ou d'exploration de jonctions (7o); et

au cours de ladite opération de SAISIE (c) les données de test sont acheminées desdits moyens de borne d'entrée de données (9(9i), 9') audit circuit à verrouillage de saisie ou d'interception (13;46) et ledit circuit à verrouillage de sortie par décalage (14;46) via le circuit sélecteur (12) dudit second registre de balayage ou d'exploration de jonctions (7o) pendant que la transmission des données de test au bloc de circuits (6) dudit second circuit intégré à semiconducteur (5) est inhibée par l'opération du circuit de sortie de données (15) dudit second registre de balayage de jonctions (7i) qui est interposé dans une voie entre la sortie (Y) dudit circuit sélecteur (12) dudit second registre de balayage d'exploration de jonctions (7i) et ledit bloc de circuits (6).

FIG.1

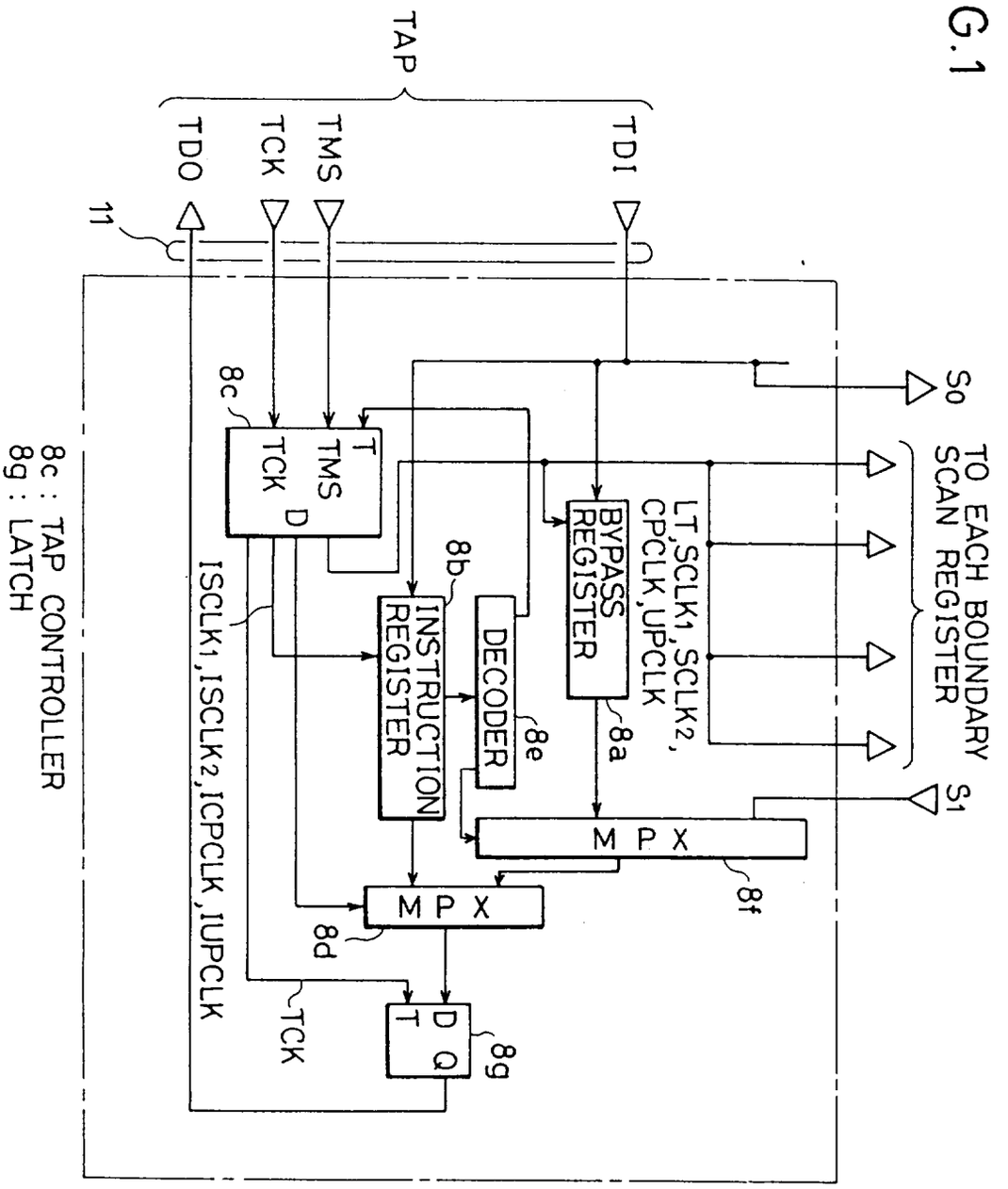
TAP
TDO
TCK
TMS
TDI
11
8c
T
TCK
TMS
D
8b
INSTRUCTION REGISTER
DECODER
8e
BYPASS REGISTER
8a
LT,SCLK1,SCLK2,
CPCLK,UPCLK
So
TO EACH BOUNDARY SCAN REGISTER
S1
M P X
8f
M P X
8d
ISCLK1,ISCLK2,ICPCLK,IUPCLK
TCK
D
T
Q
8g
8c : TAP CONTROLLER
8g : LATCH

FIG.2

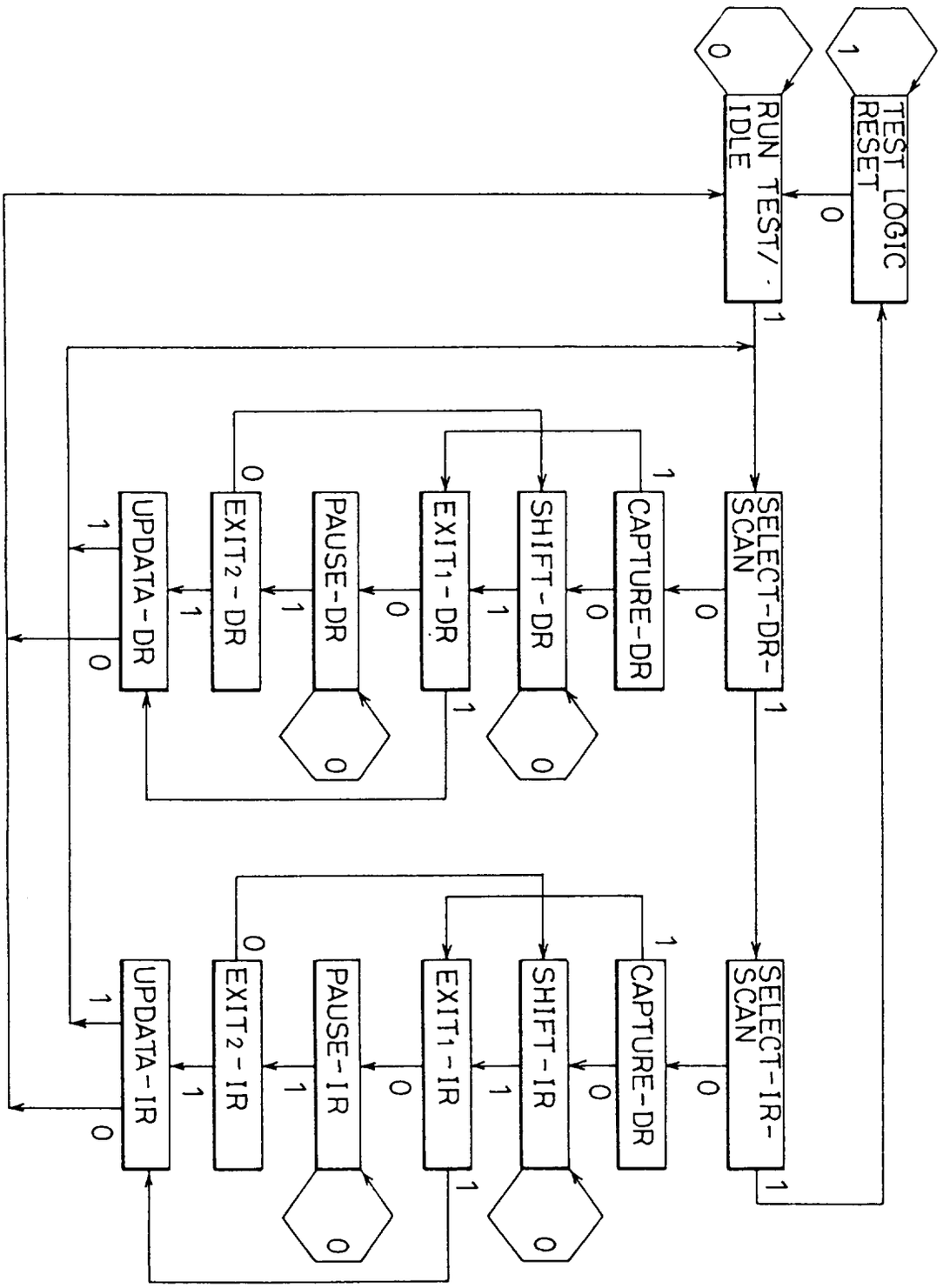
TEST LOGIC RESET
RUN TEST/ IDLE
SELECT-DR-SCAN
CAPTURE-DR
SHIFT-DR
EXIT1-DR
PAUSE-DR
EXIT2-DR
UPDATA-DR
SELECT-IR-SCAN
CAPTURE-DR
SHIFT-IR
EXIT1-IR
PAUSE-IR
EXIT2-IR
UPDATA-IR

FIG.3(a)

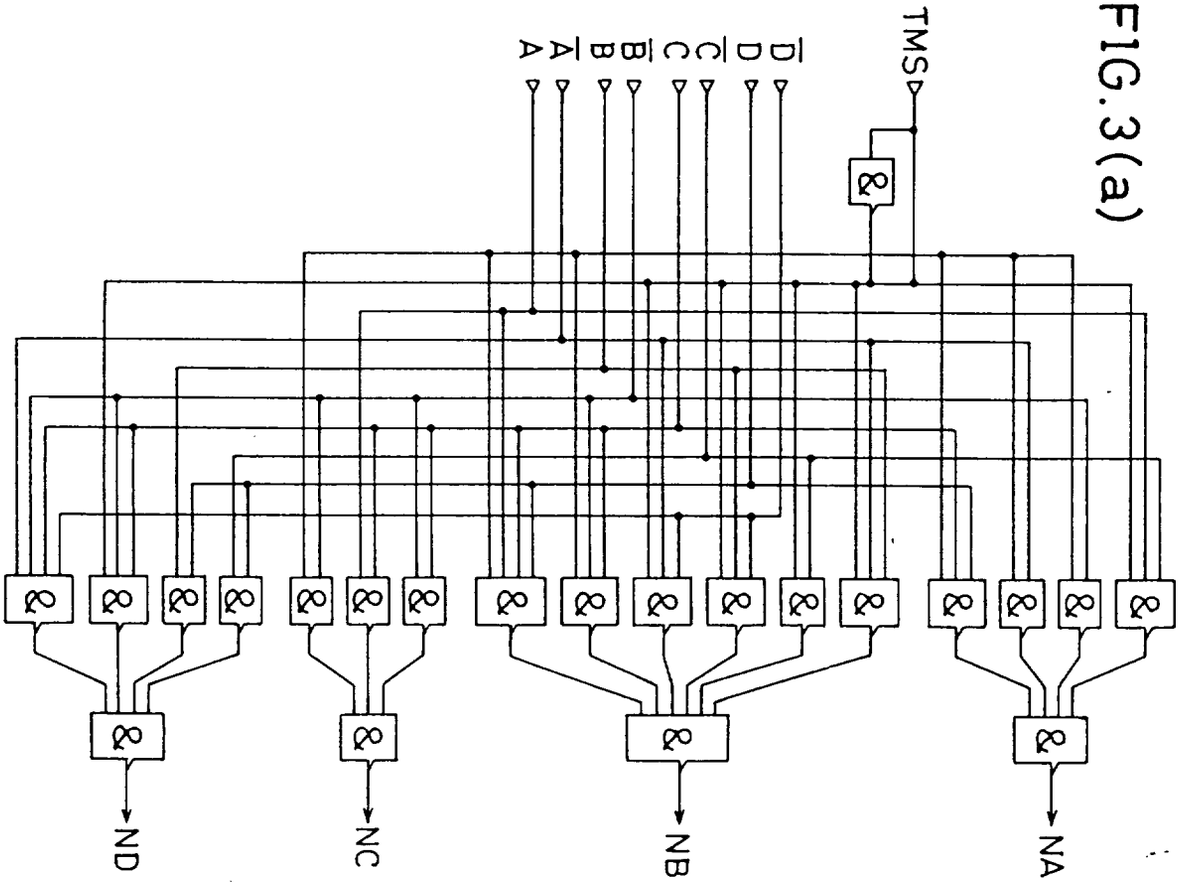

FIG.3(b)

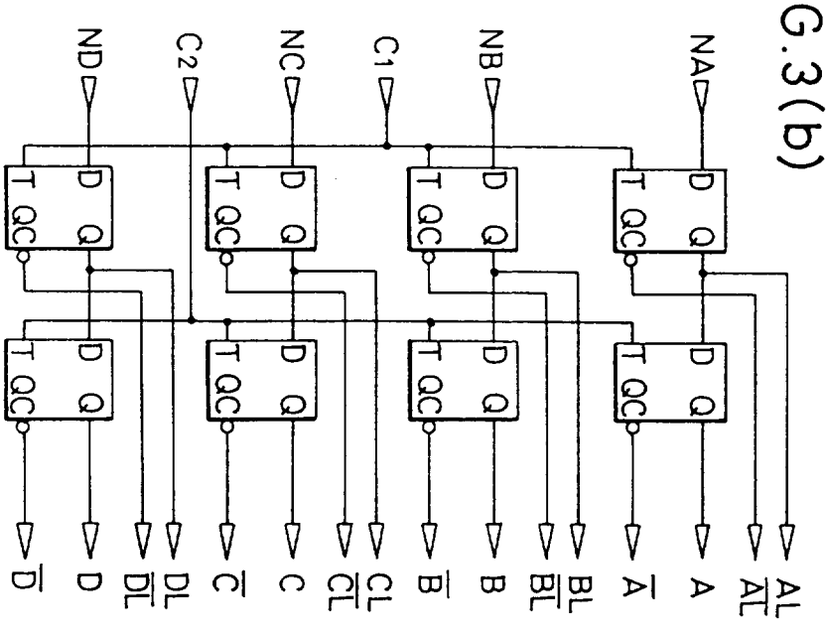

FIG.3(c)

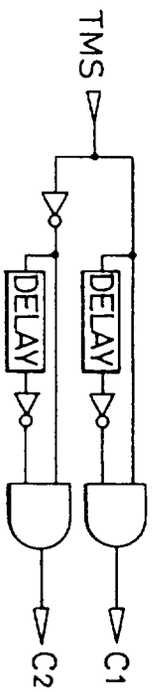

FIG.3(d)

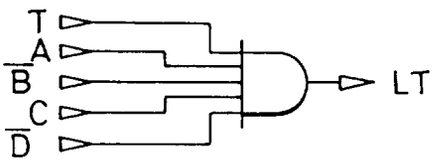

FIG.3(e)

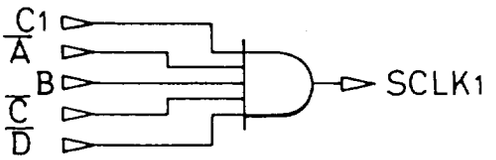

FIG.3(f)

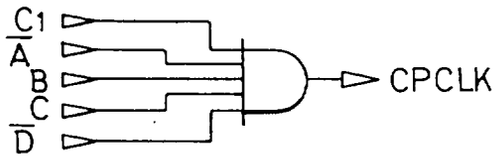

FIG.3(g)

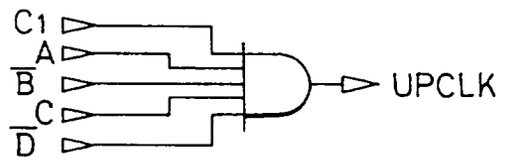

FIG.3(h)

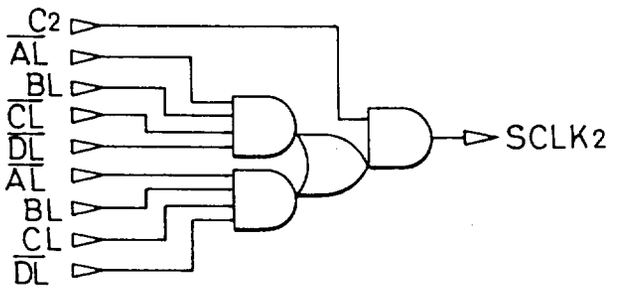

FIG.3(i)

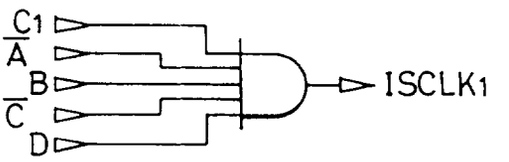

FIG.3(j)

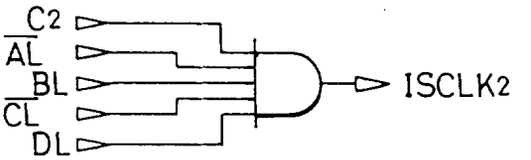

FIG.3(k)

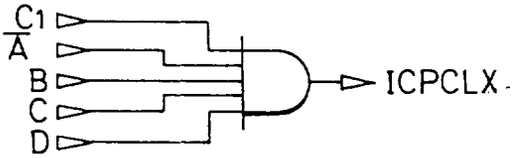

FIG.3(ℓ)

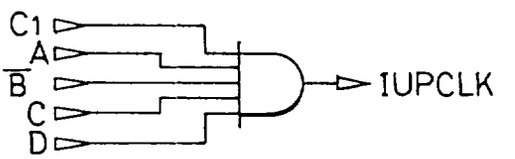

FIG.4

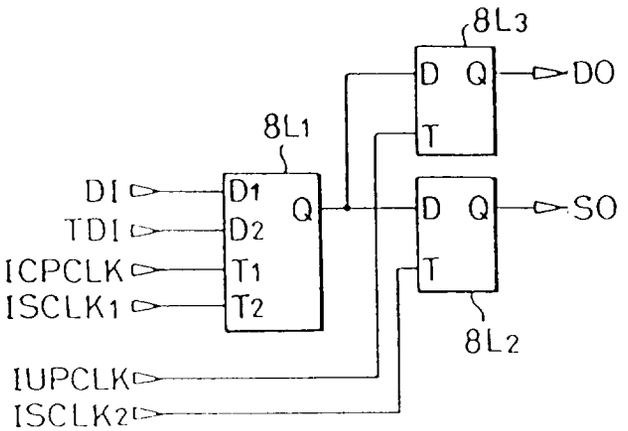

FIG.5

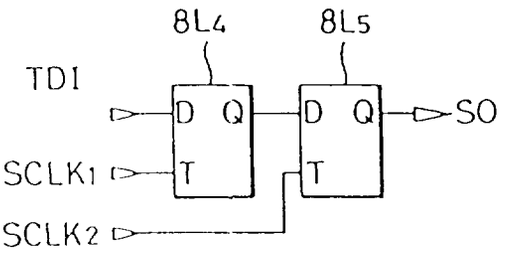

FIG.6A

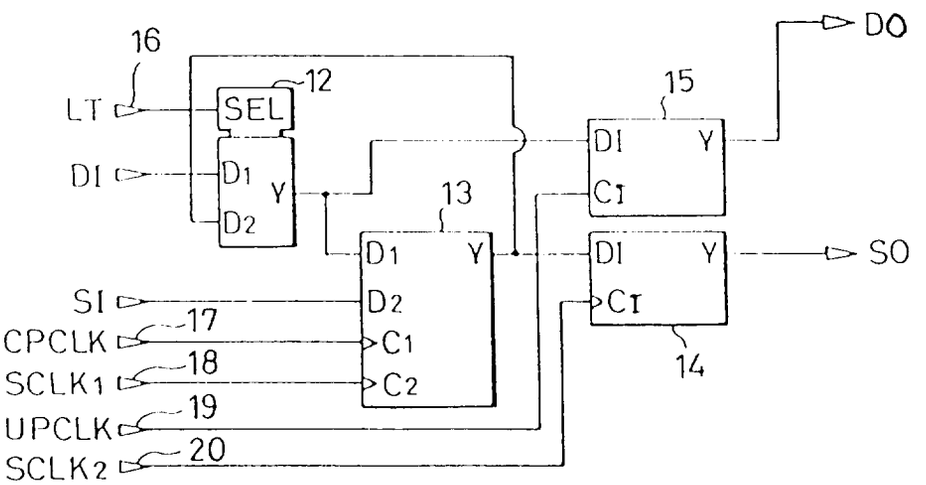

FIG.6B

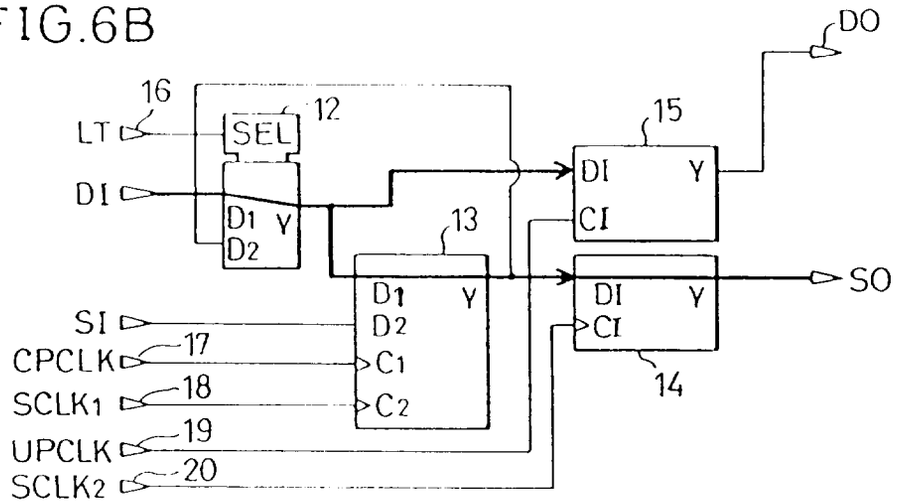

FIG.6C

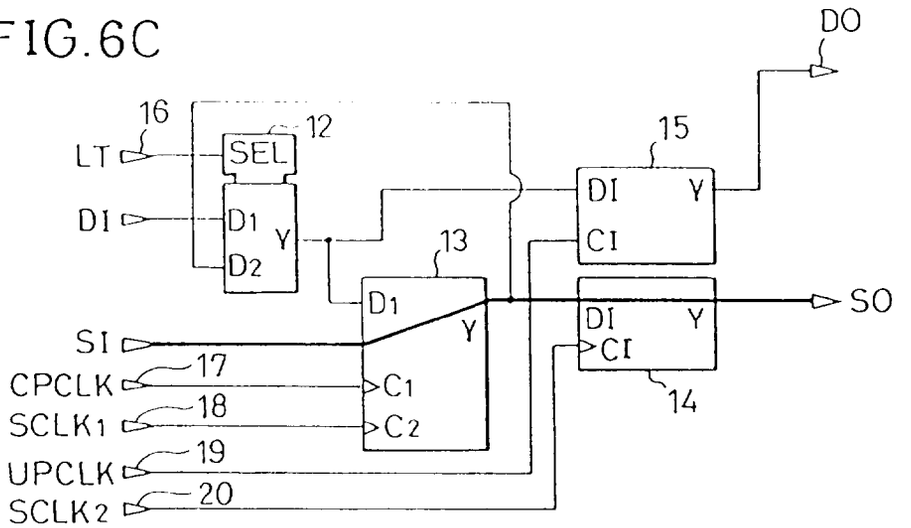

FIG.6D

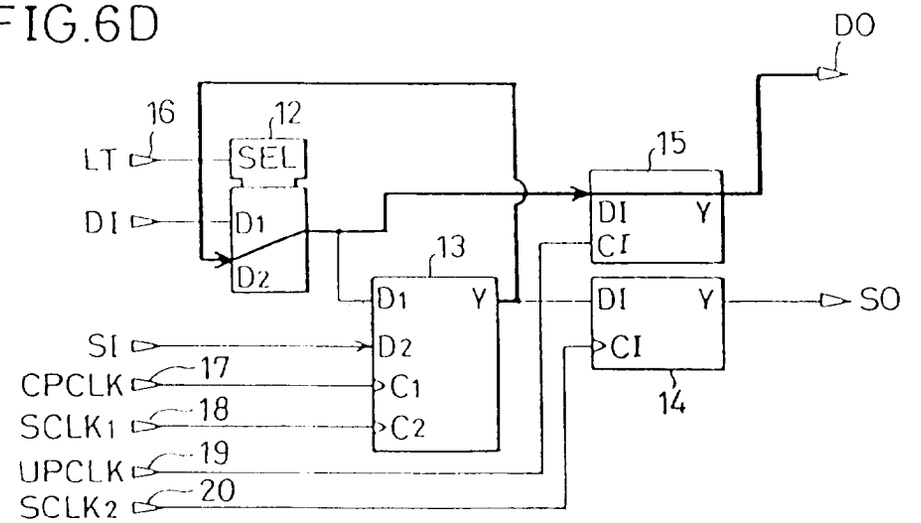

FIG.7

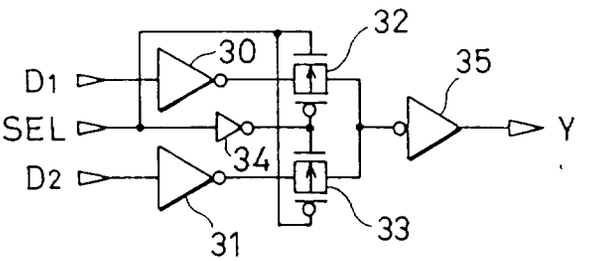

FIG.8

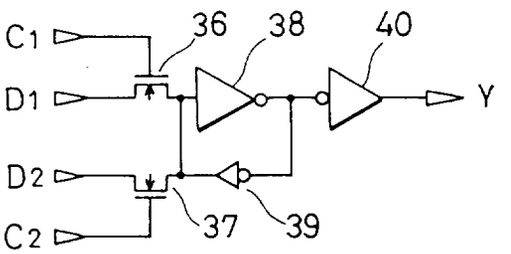

FIG.9

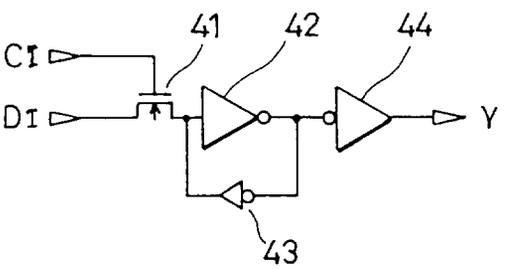

FIG.10

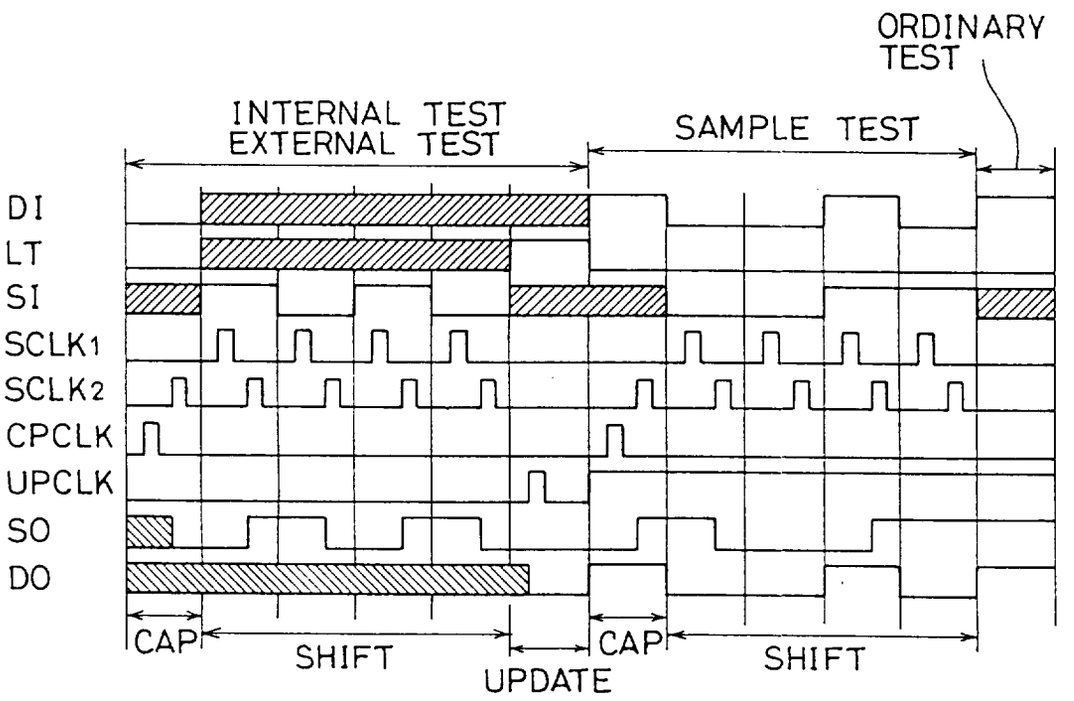
ORDINARY TEST
INTERNAL TEST
EXTERNAL TEST
SAMPLE TEST
DI
LT
SI
SCLK1
SCLK2
CPCLK
UPCLK
SO
DO
CAP
SHIFT
UPDATE
CAP
SHIFT

FIG.11

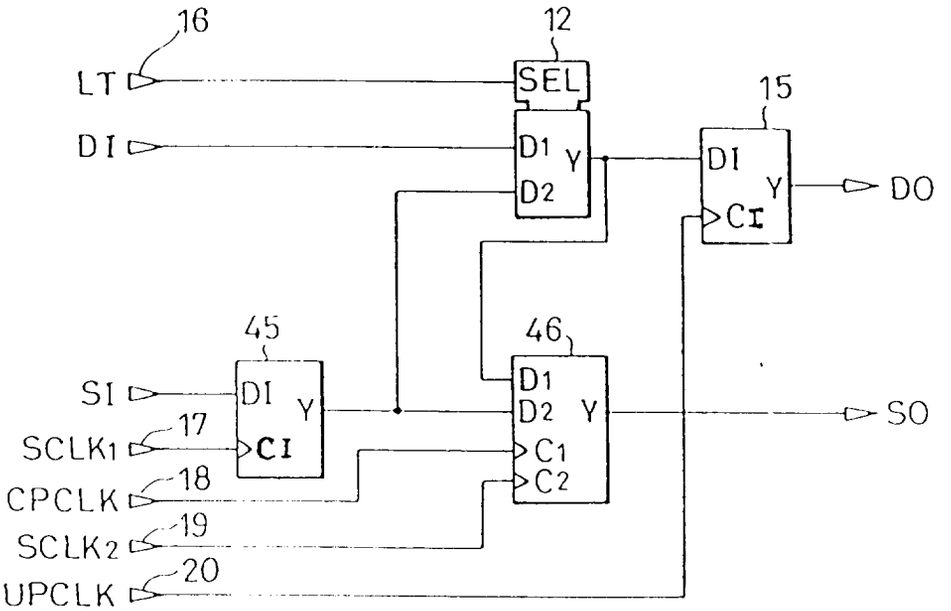
16
12
LT
SEL
15
DI
D1
Y
D2
DI
Y
DO
CI
45
46
SI
DI
Y
D1
D2
Y
SO
17
SCLK1
CI
C1
C2
18
CPCLK
19
SCLK2
20
UPCLK

FIG.12

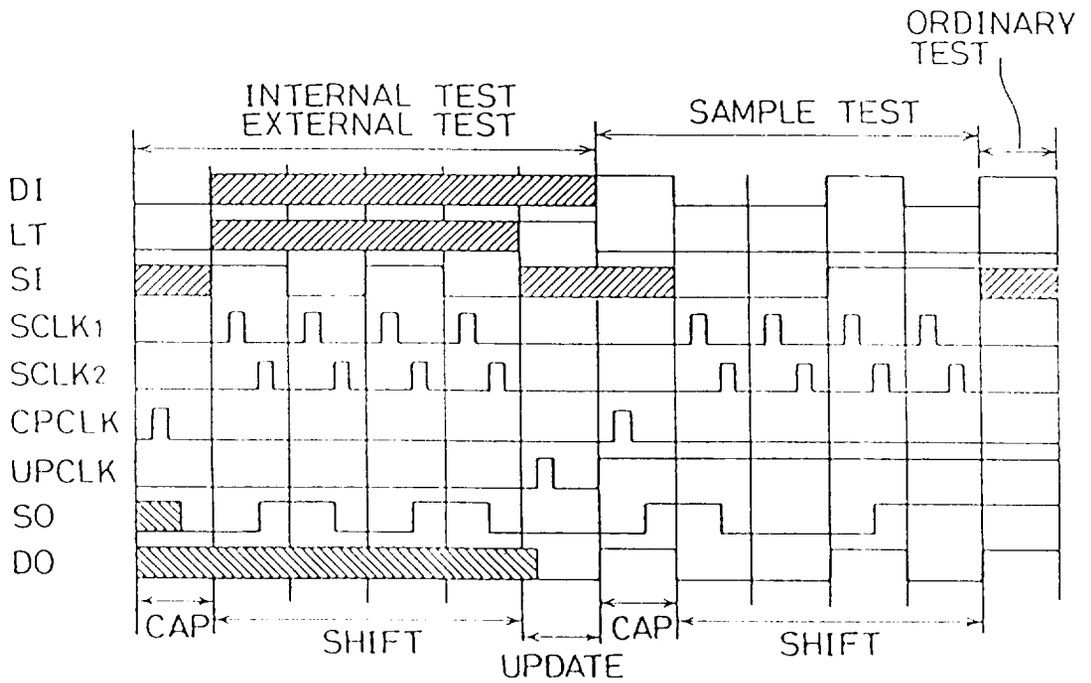
ORDINARY TEST
INTERNAL TEST
EXTERNAL TEST
SAMPLE TEST
DI
LT
SI
SCLK1
SCLK2
CPCLK
UPCLK
SO
DO
CAP
SHIFT
UPDATE
CAP
SHIFT

FIG.13

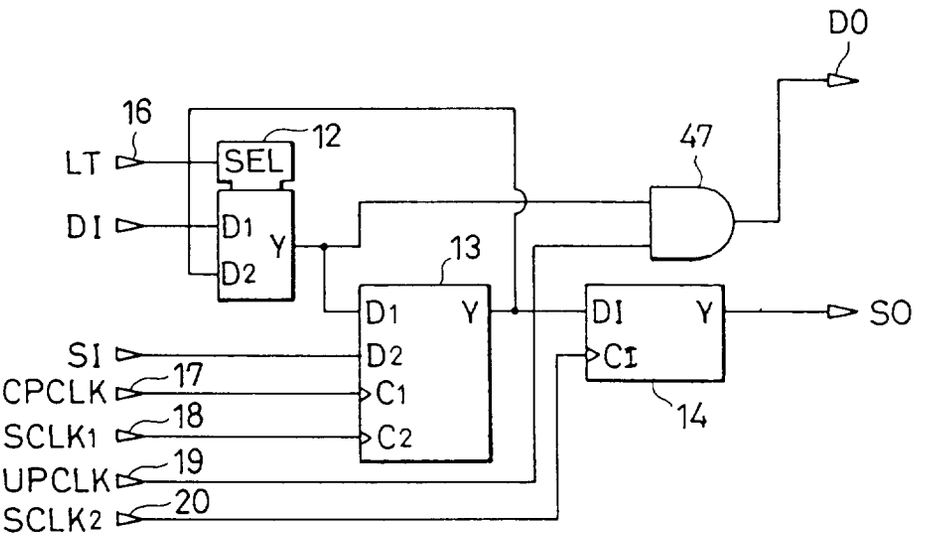
DO
16
12
LT
SEL
DI
D1
Y
D2
47
13
D1
Y
DI
Y
SO
SI
D2
CI
CPCLK
17
C1
SCLK1
18
C2
14
UPCLK
19
SCLK2
20

FIG.14

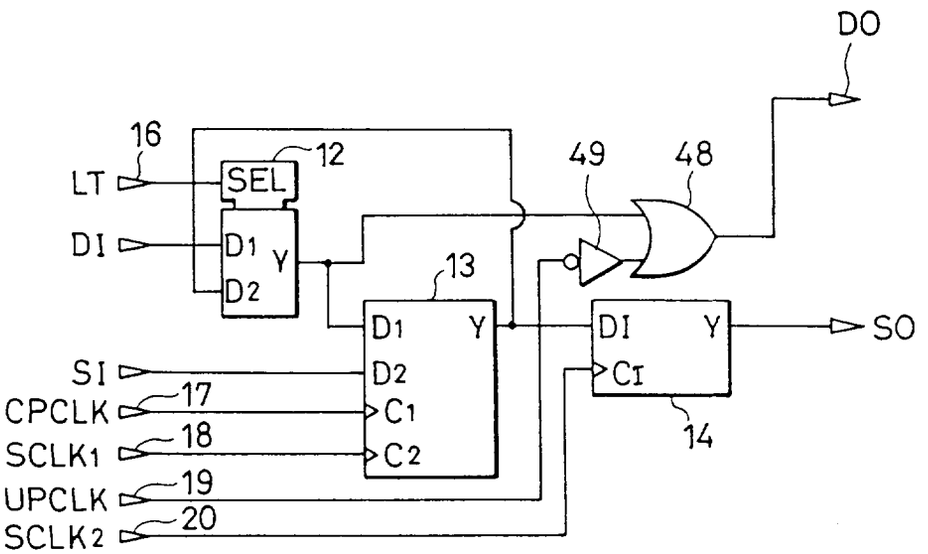
DO
16
12
49
48
LT
SEL
DI
D1
Y
D2
13
D1
Y
DI
Y
SO
SI
D2
CI
CPCLK
17
C1
SCLK1
18
C2
14
UPCLK
19
SCLK2
20

FIG.15

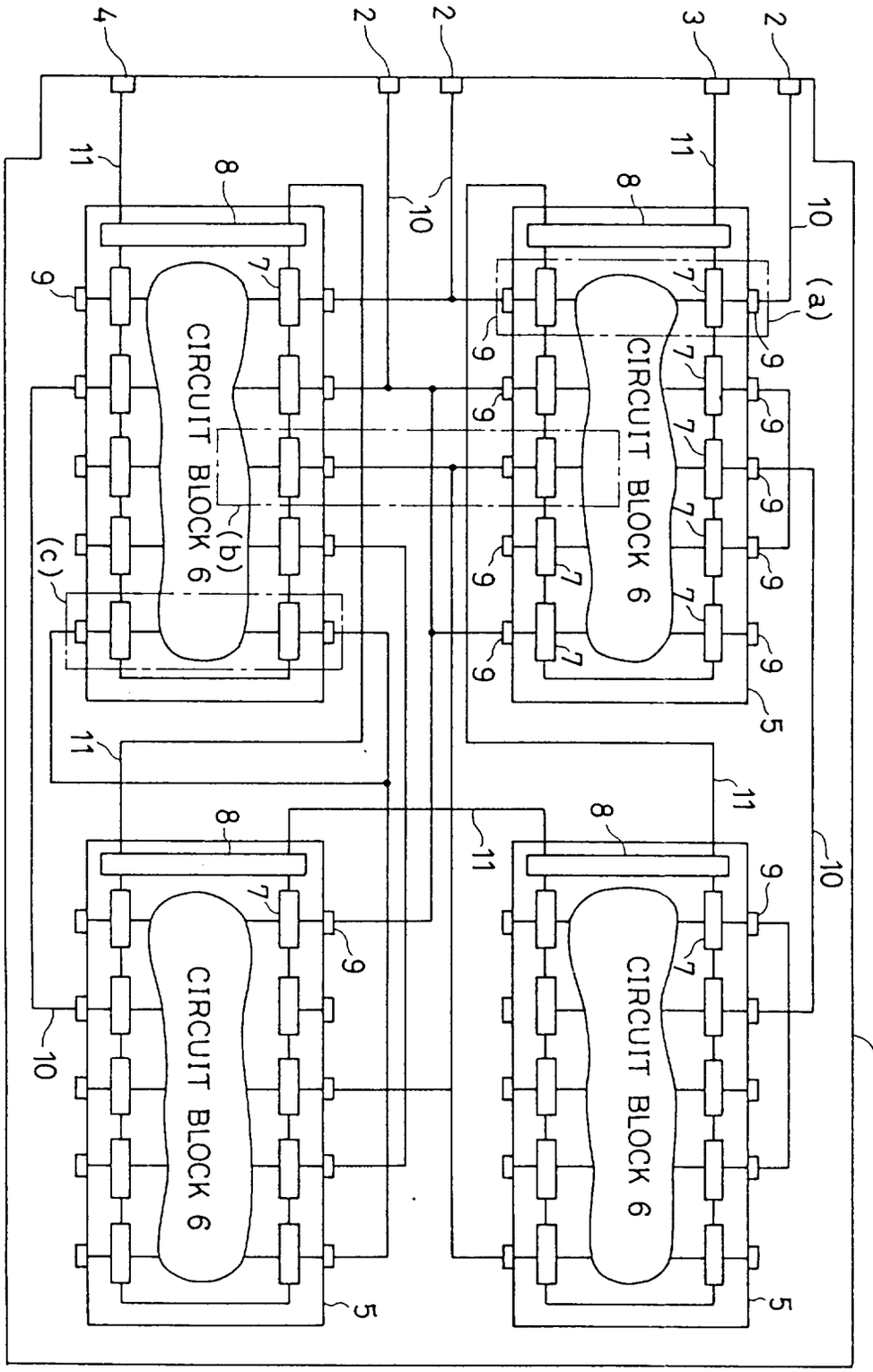
CIRCUIT BLOCK 6
CIRCUIT BLOCK 6
CIRCUIT BLOCK 6
CIRCUIT BLOCK 6
(a)
(b)
(c)
1
2
3
4
5
7
8
9
10
11

FIG.16

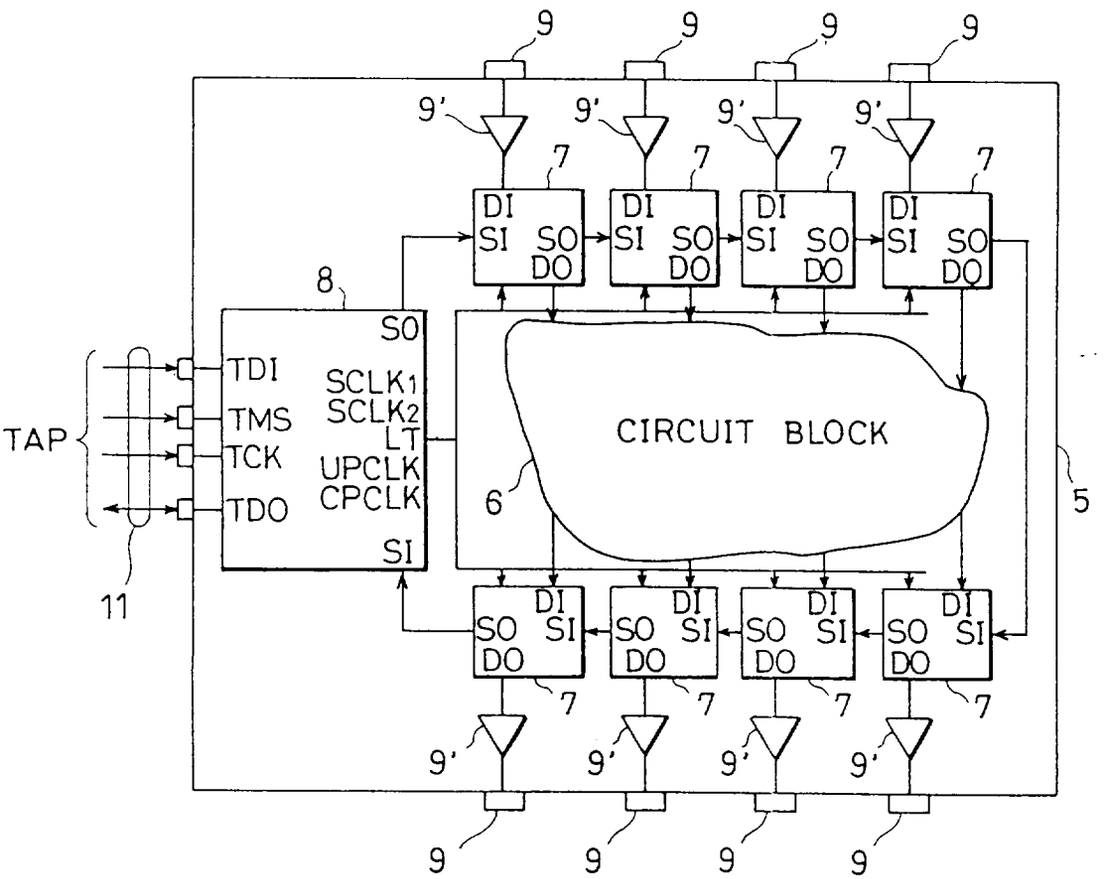
9
9'
7
DI
SI
SO
DO
8
SO
TDI
TMS
TCK
TDO
SCLK1
SCLK2
LT
UPCLK
CPCLK
SI
TAP
11
CIRCUIT BLOCK
6
5

FIG.17A

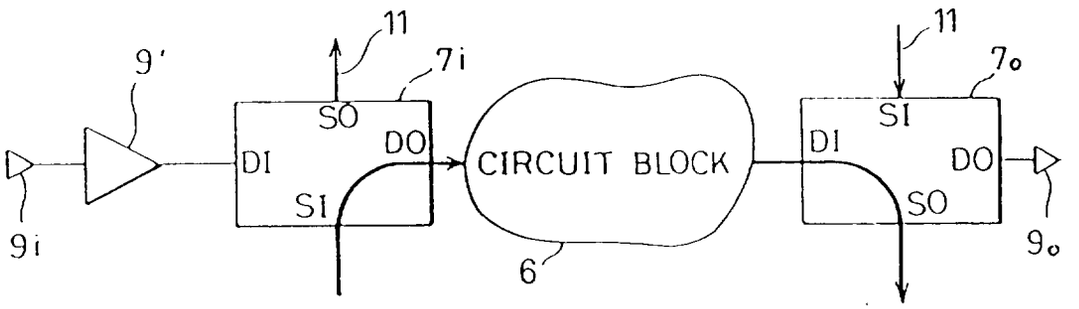

FIG.17B

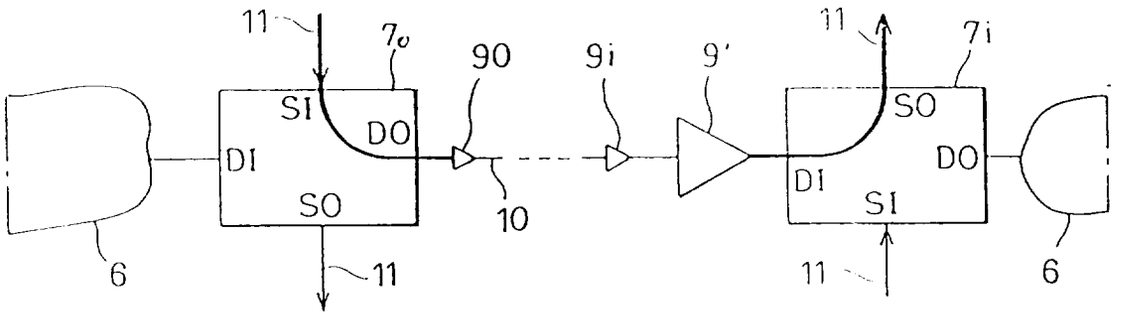

FIG.17C

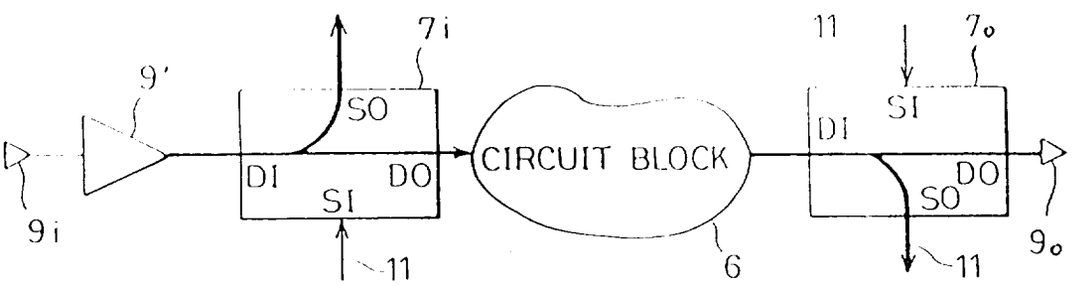

FIG.18A

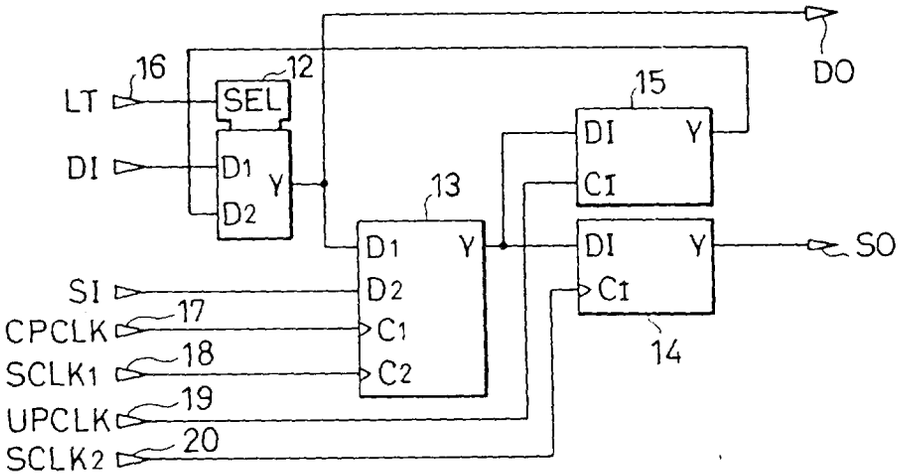

FIG.18B

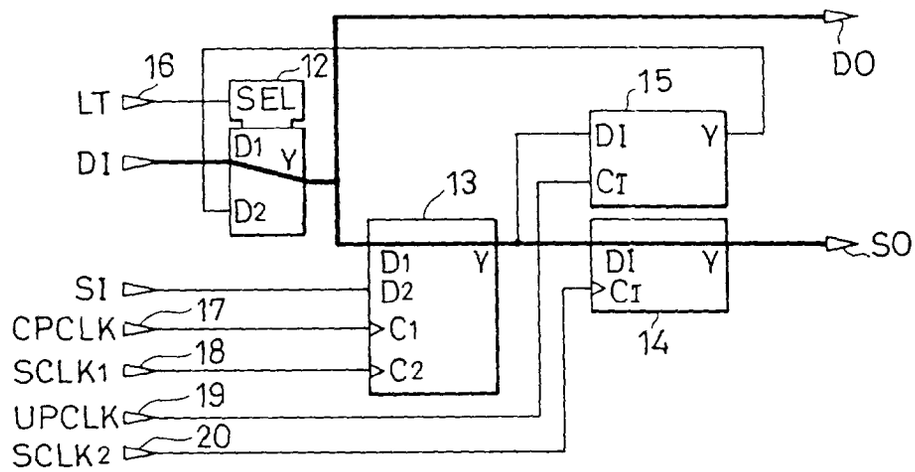

FIG.18C

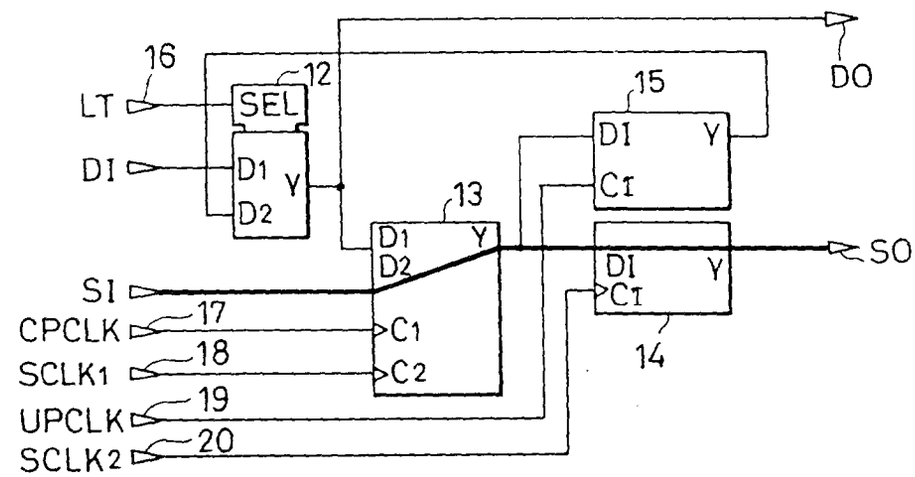

FIG.18D

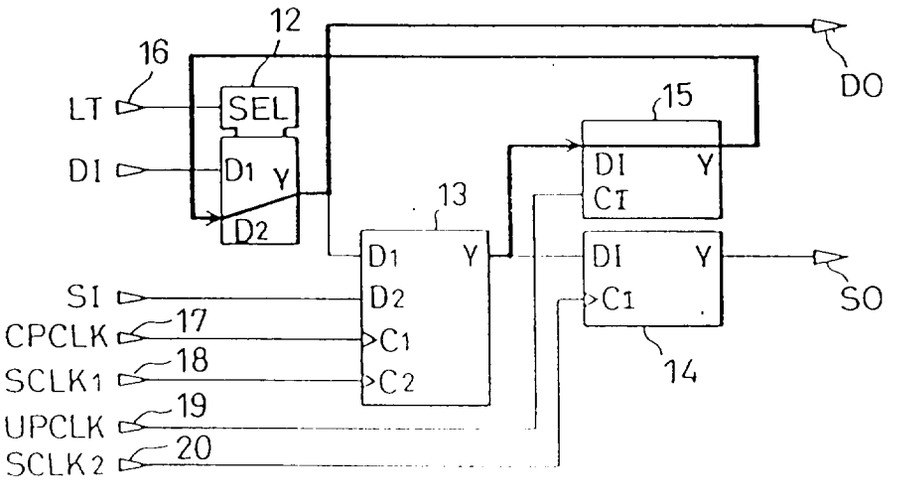

FIG.19

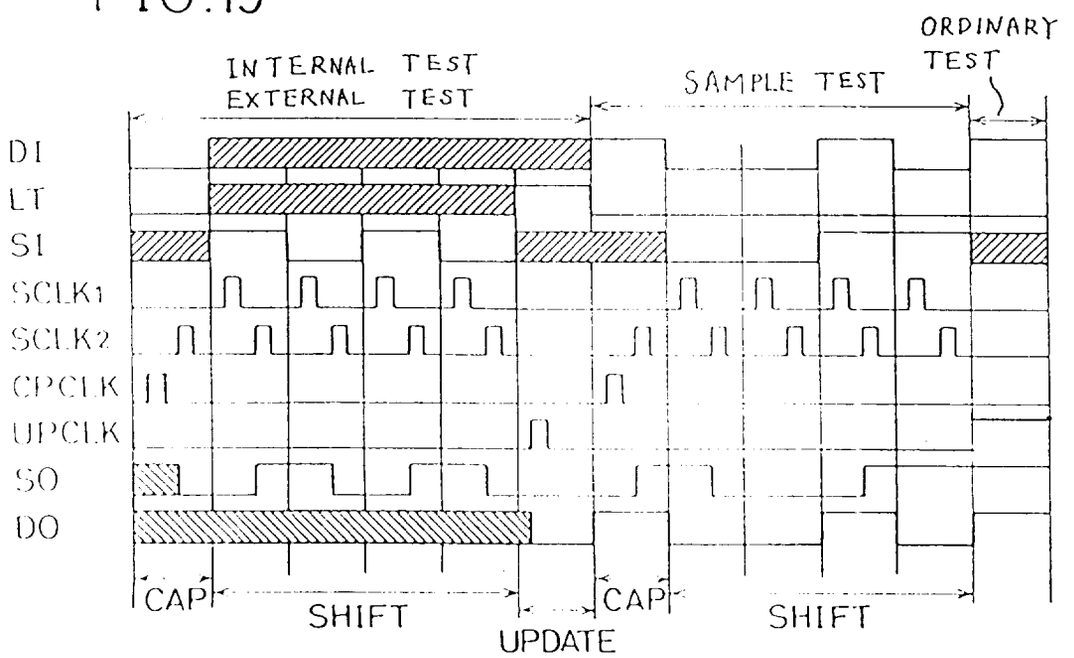

FIG.20A

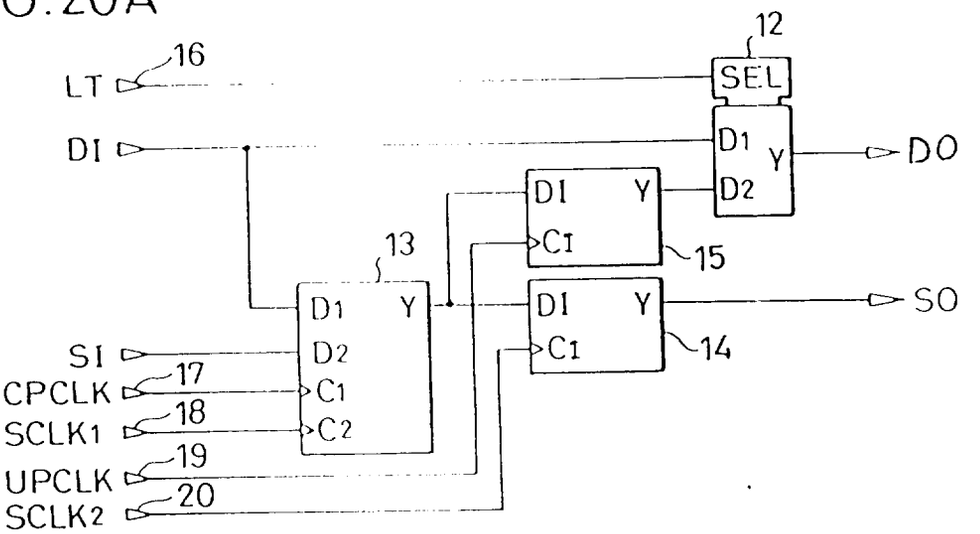

FIG.20B

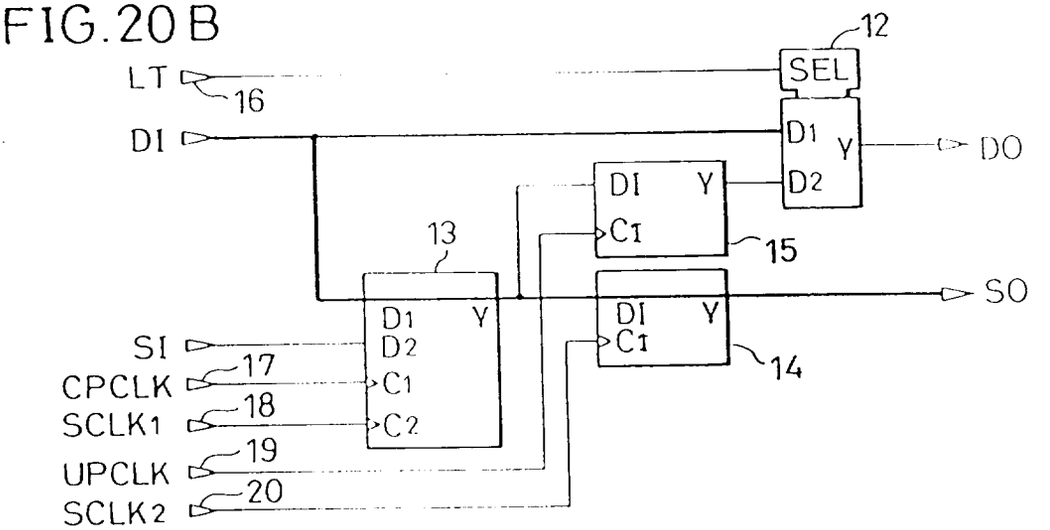

FIG.20C

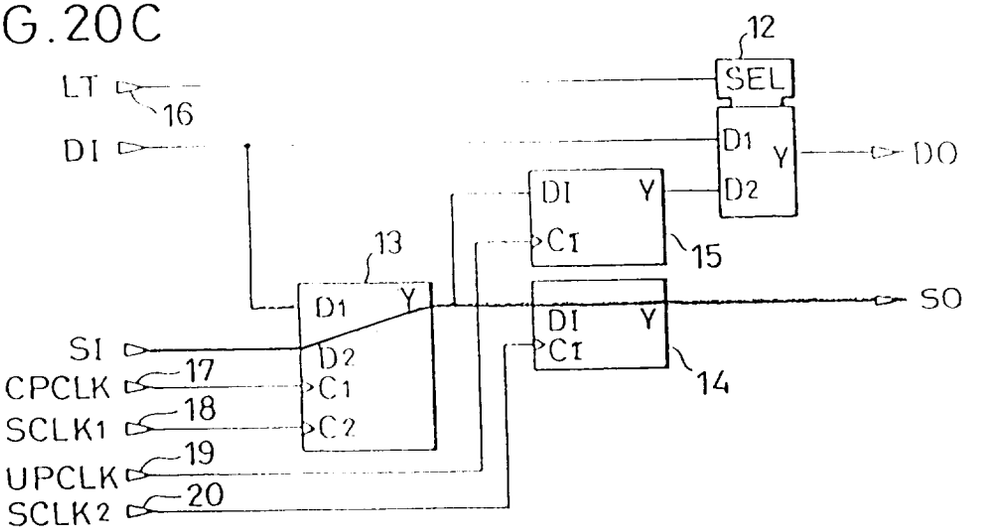

FIG.20D

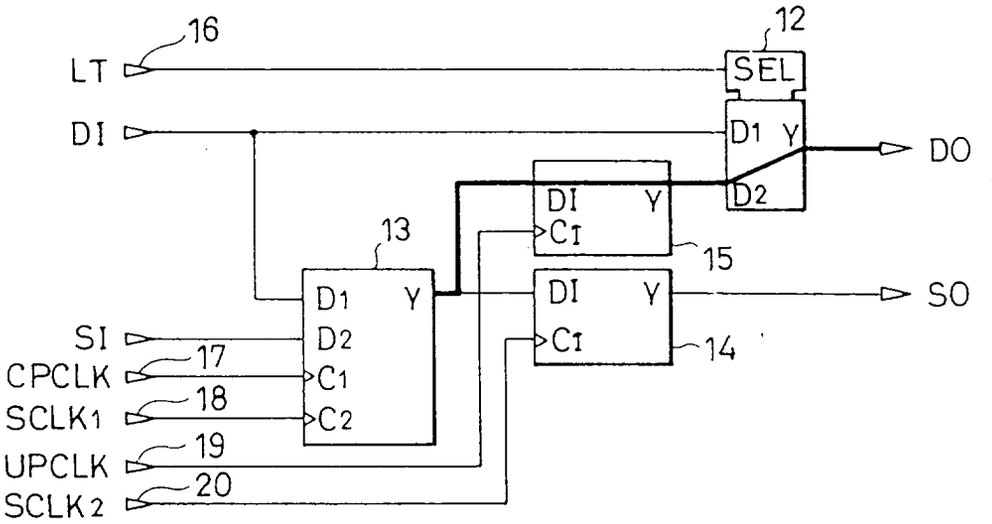

FIG.21