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(54) Drive circuit for dot matrix display.

(57) A drive circuit for a dot matrix liquid crystal display which receives polarity changing drive voltages in different fields, comprising segment drivers for supplying low voltage picture signals and common drivers for supplying a first voltage having a large voltage difference from the picture signal during a selected time and a second voltage having a small voltage difference from the picture signal during non-selected time.

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BACKGROUND OF THE INVENTION

a) Field of the Invention

This invention relates to a dot matrix display, and more particularly to a dot matrix display drive circuit capable of using a low voltage segment driver.

b)Description of Related Art

Description will be made hereinbelow on the conventional dot matrix liquid crystal display (LCD), on several selected items.

Conventional Addressing Mode

A dot matrix LCD is driven by common drivers on row side and by segment (individual) drivers on segment side. In another words, pixels aligned in one direction form a row and are given with a set of display data at a same time. The direction of row may either along x direction or along y direction, but the description hereinbelow will be made assuming that the row is along the x direction (horizontal direction). Fig. 2 shows signals for two successive fields supplied to the matrix from the common driver and from the segment driver in the conventional addressing mode, in part(A) and part(B), respectively.

Also, part (C) of Fig. 2 shows a combined effective voltage which in applied to the pixel (picture element) at each element of the LCD matrix.

The common driver supplies a voltage waveform signal formed of 4 levels of voltage V1, V2, V5 and -VEE as shown in part (A) of Fig. 2, to each row of the matrix. The maximum voltage difference V1 + VEE is of the order of about 25-40 volts.

The segment driver supplies a voltage waveform signal formed of 4 levels of voltage V1, V3, V4 and -VEE as shown in part (B) of Fig. 2, to each column of the matrix. The voltage difference in each field, e.g. V1-V3 is of the order of about 3 volts. Cross-hatched region represents that any voltage in the region may be applied. When the field changes, the voltages are changed widely, for example by about 25-40 volts.

In the first field, voltages of V2 and -VEE are applied to the row and voltages of V1 and V3 are applied to the column depending on the state of display. In the second field, voltages of V1 and V5 are applied to the row and voltages of V4 and -VEE are applied to the column depending on the state of display.

The combined signal VPIXEL which the pixel receives takes the peak amplitude during the selection time τR. The peak amplitude becomes (VSCAN + ϵVDATA) in the first field, and -(VSCAN + ϵVDATA) in the second field. Here, the coefficient ϵ is 1 when the pixel is "on" and is -1 when the pixel is "off". The peak amplitude (VSCAN + VDATA) corresponding to the on state is equal to the maximum voltage difference of the power source.

$$VSCAN + VDATA = V1 - (-VEE) = V1 + VEE$$

The combined signal which the pixel receives is VDATA or -VDATA except the selection frame τR, the absolute value of which is constant.

The absolute value VDATA except the selection time is equal to V1-V2, V2-V3, V4-V5, or V5-(-VEE).

The dot matrix display is driven by the six voltages as described above.

Conditions of Drivers

Both of the common driver and the segment driver should supply signals having a high peak amplitude. Namely, the peak amplitude of the common driver is V1-(-VEE). The peak amplitude of the segment driver is also V1-(-VEE). Therefore, each common driver and each segment driver should have the maximum operable voltage of V1-(-VEE) or above. In the case of highly multiplied dot matrix, the voltage V1-(-VEE) is of the order of 25 to 40 volts.

Both the common driver and the segment driver generate four voltage levels. Each output stage uses one switch for each voltage level, and include four high voltage, heavy current switches in total.

Conditions of Power Source

The power source is simple. The six levels of voltage to be supplied are fixed in an appropriate voltage range from V1 (usually +5 volts) to -VEE (usually 20 to 35 volts).

However, the power source should supply high peak currents at the respective voltages of V1, V2, V3, V4, V5 and -VEE (typically about 1 A in a ten inch display), and the stabilization should be 1 % or less for the respective levels of voltage.

The cost of the driver circuit occupies an important part of the total cost of the display device.

Since both of the segment driver and the common driver require high operation voltages, it is not easy to use conventional low cost CMOS circuits for the dot matrix LCD.

In the case of a color display, the number of drivers increases triple times on the segment side. Therefore, especially in the case of a color dot matrix, conventional circuit become expensive.

SUMMARY OF THE INVENTION

An object of this invention is to provide a drive circuit adapted for dot matrix display of low manufacturing costs.

Ordinary low voltage (of the order of ± 3 volts) CMOS driver is used for the segment driver.

The segment driver is formed of a low voltage circuit and the common driver is formed of a high voltage circuit. The two circuits are coupled logically by photo coupling means, and are isolated in dc sense.

The cost of the circuit is reduced by the following construction.

Ordinary CMOS circuits are used in the segment side, and the manufacturing cost thereof is reduced.

Further, several performances can also be improved. For example, because of the low on-resistance RON, crosstalk is reduced. Because of the high cutoff frequency obtainable in low voltage circuits, serial access of data to the driver line memory becomes possible.

Here, the number of output transistors can be reduced to about a half either in the common driver and the segment driver. For example, the number of transistors required to generate output voltages of one way is reduced from four to two.

By reducing the number of output transistors to about a half, the size of the semiconductor chip can be greatly reduced. Not only the cost can be reduced, mounting by TAB or COG can be made easy.

In accompany with the above, several specifications of the power source can more easily be satisfied. Typically, relatively large current are supplied and accurately controlled only at low voltage levels between +5 V and -5 V. High voltage levels are of lower current and require less stabilization.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a schematic structure of a dot matrix LCD device driven by a floating power source.

Fig. 2 is voltage waveform diagrams showing the addressing mode of the conventional dot matrix LCD by a six-level power source.

Figs. 3A and 3B are circuit diagram of a floating power source of a dot matrix LCD and a voltage waveform diagram produced in the circuit of Fig. 3A.

Figs. 4A, 4B and 4C are circuit diagrams showing a common driver.

Fig. 5 is waveform diagrams for illustrating the operation of the common driver.

Fig. 6A and 6B are circuit diagrams illustrating a segment driver.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows an outline of a matrix LCD drive circuit according to a general embodiment of this invention.

A dot matrix type liquid crystal display 1 has its rows driven by common drivers 2a and 2b and its columns driven by segment drivers 3a and 3b. The common drivers 2a and 2b receive voltage signals from a level converter 5, and also receive control signals from an LCD controller 4 through photo coupling stage 6. The photo coupling stage 6 isolate the LCD controller 4 and the common drivers 2a and 2b in dc sense, and couples them logically. The level converter 5 is connected to a 6 level voltage source 11 which is similar to the conventional one, through a bridge and buffer stage 8. The bridge and buffer stage 8 receives three voltage levels of +VSCAN, ground, and -VSCAN from the 6 level voltage source 11 and supplies five voltage levels of VSCAN, VSCAN-VLOGIC, ground -VLOGIC and -VSCAN. The control signal from the LCD controller 4 are also supplied to the segment drivers 3a and 3b and the level converter 5.

The segment drivers 3a and 3b and the LCD controller 4 are low voltage circuits, and can be formed of low price, low voltage semiconductor circuits. The supply voltages for these circuits are four levels of VDATA, -VDATA, -VLOGIC and ground (VG). These voltage levels are all included in the range from +5 V to - 5 V.

Only the common drivers 2a and 2b operate at high voltages. The voltage source for the common driver is floating. The common driver receives as the source voltage, three signals of F"1", F0LOGIC, and F"0".

The voltage differences between these three signals are kept constant, and are converted periodically and totally by a level converter 5 constructed of high voltage gates of VMOS or DMOS structures.

Several logic signals (DATA IN, CLOCK, PHASE SHIFT, ENABLE) which are supplied from the LCD controller 4 and varies their voltage to or from -VLOGIC are all level-converted by the photo coupling means 6 to form DATAIN*, CLOCK*, PHASE SHIFT*, ENABLE* which change the voltage from F"1" to F0LOGIC. Photo coupling means 6 is used to perform the level conversion of these logic signals supplied to the common drivers 2a and 2b without noise. Such a photo-coupling circuit may be formed of a voltage dividing circuit for establishing desired voltages, F"1" and L0LOGIC, and photo-excited switch means, such as photo-couplers, for extracting desired voltage.

By the above described construction, the voltages which the segment drivers 3a and 3b should treat are only two low level voltages, VDATA and -VDATA, and the LCD controller 4 can be made to operate also at low voltages

The common drivers 2a and 2b have a floating power source, and simultaneously receive the level converted logic signals. Here, the voltage levels which the common driver 2a and 2b should treat are only two, F"1" and F"0".

The outline of this invention is described as above. This invention will further be described in detail along the respective constituent elements.

Power Source Circuit

The power source circuit corresponds, in the structure of Fig. 1, to the combination of the 6-level power source 11, the bridge and buffer stage 8 and the level converter 5, and supplies currents to the common drivers 2a and 2b, the segment drivers 3a and 3b, and the LCD controller 4.

A structure of the power source circuit is shown in Fig. 3A.

First stage: A power source 11 similar to the conventional one supplies six constant voltages, VSCAN, VDATA, ground(VG), -VDATA, -VLOGIC and -VSCAN.

Four low voltages VDATA, VG, -VDATA and -VLOGIC are derived as low voltage levels and directly supplied to the segment drivers 3a and 3b and the LCD controller 4.

Second Stage: The bridge and buffer stage 8, which is formed of a resistance bridge and the associated buffers similar to the conventional one supply two intermediate levels VSCAN-VLOGIC and -VLOGIC. Only the logics of the common driver use these intermediate voltages. Therefore, these levels do not need to be adjusted precisely, and the required currents are very low (of the order of several mA).

Third Stage: A group of level converting elements in the level converter 5 realize the following three signals. Here, VMOS or DMOS switches 13 are periodically activated by the PHASE SHIFT signal supplied from the LCD controller 4.

F"1" = VSCAN or VG (depending on the PHASE SHIFT signal)
F0LOGIC = F"1"-VLOGIC
F"0" = F"1"-VSCAN

These voltage waveforms are shown in Fig. 3B.

The voltage difference among F"1", F0LOGIC and F"0" are maintained constant throughout the level conversion by a group of capacitors CF (in the case of a ten inch LCD, typically CF = 10nF)

Common Driver

The common driver circuit is shown in Figs. 4A, 4B and 4C.

As an example, a diver circuit for driving six rows is shown. Fig. 4A shows a schematic circuit configuration, Fig. 4B shows the relation with the control signal, and Fig. 4C is an enlarged diagram of a portion shown by a broken line in Fig. 4B.

The common driver is constructed of three stages.

The first stage is an ordinary shift register which is operated by two signals, DATA IN* and COMMON CLOCK* (the waveforms on which before level conversion are shown in Fig. 5).

The second stage is an inverter stage controlled by PHASE SHIFT* (the waveform of which before the level conversion is shown in Fig. 5). This stage supplies six signals, Gate rowi* (i is 1 to 6,) which are used in the third stage.

The third stage is constructed of six output blocks, each having a structure as shown in Fig. 4C.

When the enable signal ENABLE* (the waveforms of which before the level conversion is shown in Fig. 5) is "1", the transistor T1 connected to F"1" and the transistor T0 connected to F"0" are respectively driven by Gate row signal and its inverted and converted signal, respectively, and generate the common driver output F"1" or F"0". When the enable signal ENABLE* is "0", transistors T1 and T0 are both open. Therefore, when the signal ENABLE* is "0", the common drivers become of high impedance.

Fig. 5 shows the general relation of all the signals described hereinabove.

The PHASE SHIFT (or PHASE SHIFT*) is shown at the upper most part of Fig. 5. During the first field, the signal PHASE SHIFT is in the state "1", and during the second field, the signal PHASE SHIFT is in the state "0".

The next part shows the signal DATA IN (or DATA IN*). The signal DATA IN is a signal pulse at the beginning of each field. This is a single "1" as the first data which initialize the shift resister.

The third part shows the signal ENABLE (or ENABLE*). The signal ENABLE keeps the state of "0" (corresponding to the high impedance of all the common drivers) from the (N+1)th pulse of COMMON CLOCK to the first pulse of the next COMMON CLOCK.

The fourth part shows the signal COMMON CLOCK (or COMMON CLOCK*). The signal COMMON CLOCK pushes out the signals in the shift register. When the number of rows to be scanned is N, the signal COMMON CLOCK includes N+1 pulses. After the final stage, the single "1"s are pushed out to make all the data in the shift register "0".

The fifth and the sixth parts show the common driver outputs corresponding to the succeeding two rows (for example, the first and the second rows). In the first frame, the driver output becomes F"1" during the selection time and becomes F"0" during the non-selection time. In the second frame, the common driver output becomes F"0" during the selection time and becomes F"1" during the non-selection time.

The table at the lower part of the figure represents the levels of the shift registers, and shows the respective states of the Gate Row signals supplied to the output state. When all the Gate Row signals are in the same state (all "0" or all "1"), the signal ENABLE is "0". Therefore, when the PHASE SHIFT signal is switched from "0" to "1" or from "1" to "0" to activate the total change of the signals F"1", FOLOGIC and F"0" for the common driver power source, all the common drivers become of high impedance. Therefore, the common drivers are protected from the polarity inversion. Namely, we can know an important fact that when the level conversion is being performed, currents are not supplied.

before conversion	after conversion
all the Gate row signals "0"	all the Gate row signals "1"
↓	↓
all the common drivers supply F"0"=VG to all the rows	all the common drivers supply F"1"=VG to all the rows

The effective voltage applied to the cells is not varied, the level conversion does not require much current and the polarity inversion of the drivers has no risk.

Segment Driver

Fig. 6 shows a structure of the segment driver. A segment driver has four stages of low voltage circuits.

First stage: A shift register 15 (date is serial).

Second stage: A line memory 16 (which has parallel access).

Third stage: A polarity inversion stage 17 which is controlled by a phase shift signal PHASE SHIFT.

Fourth stage: An output driver 18.

The block in the output driver 18 for each segment is formed of a pair of CMOS transistors directly driven by the signal GATE SEGMENT supplied in the third stage as shown in Fig. 6B.

Description has been made hereinabove along an embodiment of this invention. This invention is not limited thereto. For example, it will be apparent for those skilled in the art that the various alterations, improvements and combinations are possible within the scope of the appended claims.

As has been described hereinabove, according to this invention, the manufacturing costs of a dot matrix display can be reduced.

A high voltage stage and a low voltage stage are electrically isolated and logically coupled by a photo coupling stage, and hence the low voltage circuit does not require a high withstand voltage.

Claims

1. A drive circuit adapted for a dot matrix display having common drivers and segment drivers, comprising:

a group of common drivers for generating output voltages, adapted for driving rows of a dot matrix display;

a power source for supplying three kinds of signals F"1", F0LOGIC and F"0" to the common drivers, the voltage differences between F"1" and F0LONG and between F"1" and F"0" being constant, the respective signal levels changing periodically by being driven by a signal PHASE SHIFT which changes at the end of each field, with F"0" and F"1" being alternately grounded;

each output voltage of the common driver changing between F"1" and F"0" such that all the non-selected rows are always grounded; and

converter stage having a photo-coupling means, for supplying logic signals between F"1" and F0LOGIC to the common drivers.

2. A drive circuit adapted for a dot matrix display according to claim 1, wherein said power source includes

5-levels power supply for supplying VSCAN, VSCAN-VLOGIC, ground, -VLOGIC and -VSCAN, and

three gates driven by the signal PHASE SHIFT and supplying signals of F"1" = VSCAN or ground, F0LOGIC = F"1"-VLOGIC, and F"0" = F"1"-VSCAN, and

said common drivers have such enable function that all output drivers are driven to high impedance state during all level conversion of F"1", F0LOGIC, and F"0".

3. A drive circuit adapted for a dot matrix display which includes picture elements at cross points of rows and columns, comprising:

signal drivers for supplying picture signals to the columns of the picture elements;

common drivers for supplying a selection signal to a selected row of the picture elements and a non-selected signal to non-selected rows of the picture elements;

a controller circuit for supplying low voltage picture signals to the segment drivers and low voltage control signals;

means for coupling said control signals with at least one of said high voltage signals and supplying them to said common driver.

4. D drive circuit adapted for driving a dot matrix display including picture elements at cross points of rows and columns, the polarity of voltage applied to the picture elements being reversed alternately from field to field, the drive circuit comprising:

a control circuit for suppling picture data signals, and control signals including a phase shift signal synchronized with the field change;

a segment driver circuit for receiving the picture data signal and the phase shift signal and supplying the picture data signal and the inverted picture data signal alternately in succeeding fields;

a high voltage source for supplying a first voltage which changes between a first high voltage of one polarity and a first low reference voltage and a second voltage which changes between a second low reference voltage and a second high voltage of the other polarity, in synchronism with said phase shift signal;

a common driver circuit for applying the first or second high voltage to a selected row during a selection time and the first or second low reference voltage during other periods depending on the field change so that a selected picture cell can be applied with a predetermined high voltage.

5. A drive circuit according to claim 4, further comprising means for level shifting said control signals through photoelectric elements.

6. A drive circuit according to claim 4, wherein said common driver circuit includes a pair of CMOS transistors for driving each row, and enabling means for enabling said pair of CMOS transistors only when there exists a selected row.

7. A drive circuit according to claim 4, wherein said common driver circuit includes a register for receiving a row selecting signal, and means for transmitting said row selecting signal directly and through inverter means.

8. A drive circuit according to claim 4, wherein said segment driver circuit includes a register for receiving said picture data signal, and means for transmitting said picture data signal directly and through inverter means.

9. A drive circuit according to claim 7, wherein said segment driver circuit includes a register for receiving said picture data signal, and means for transmitting said picture data signal directly and through inverter means.

FIG. 1

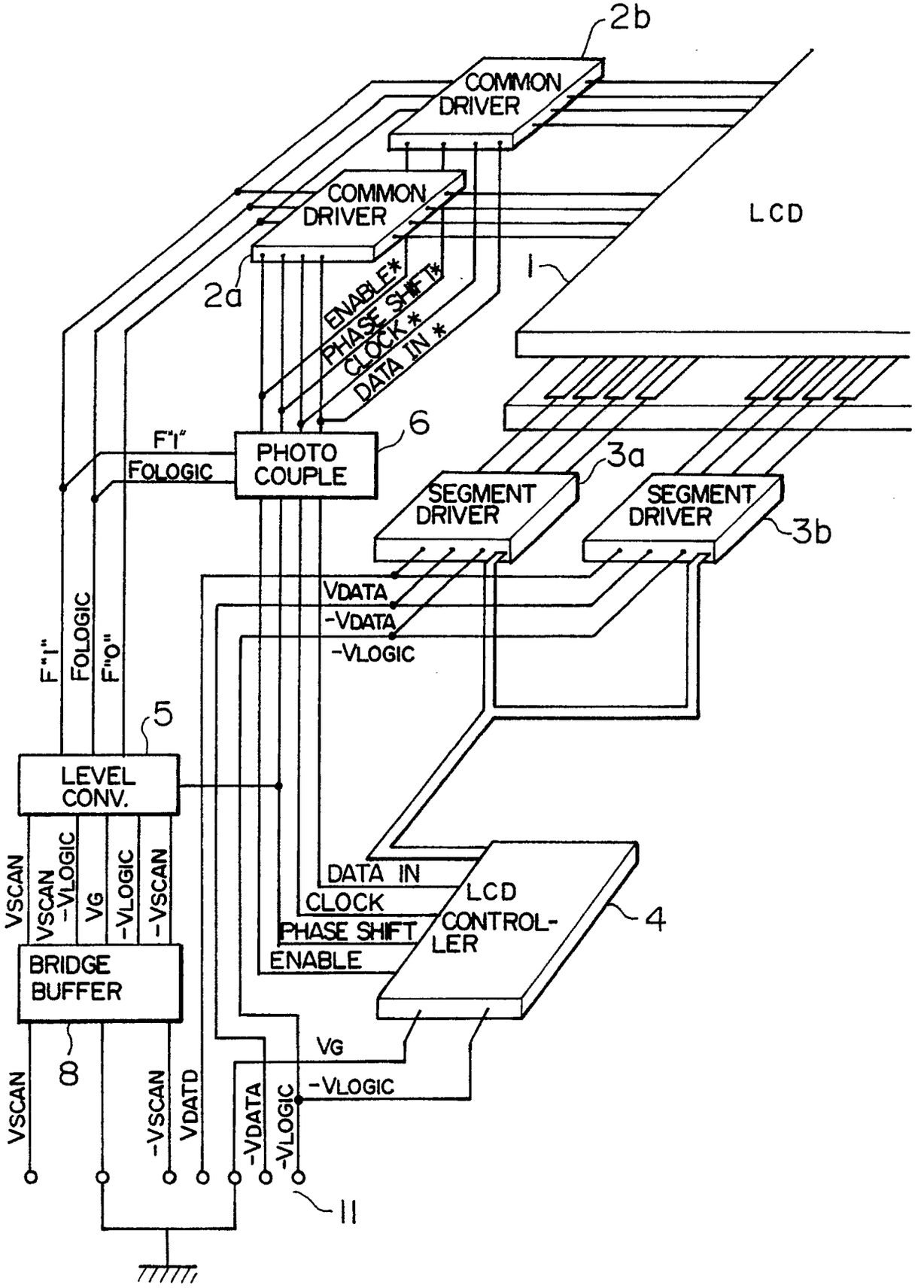
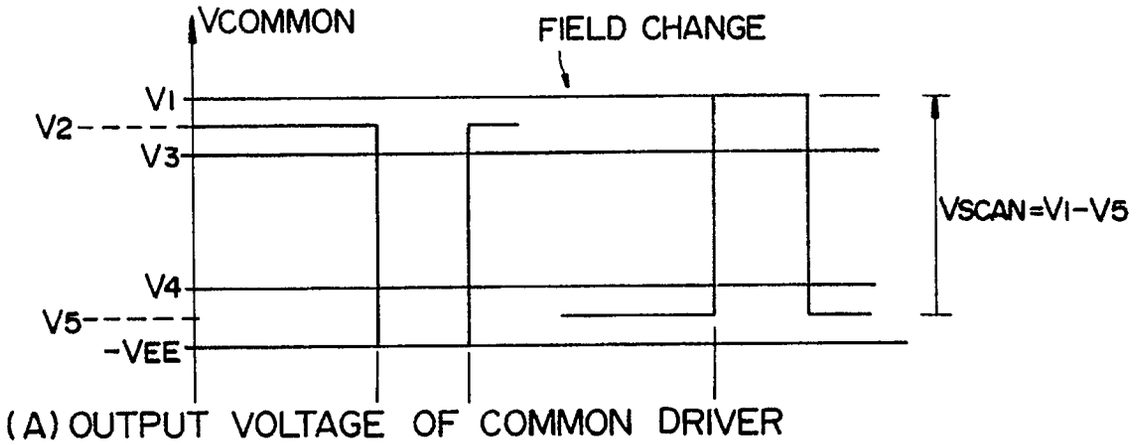
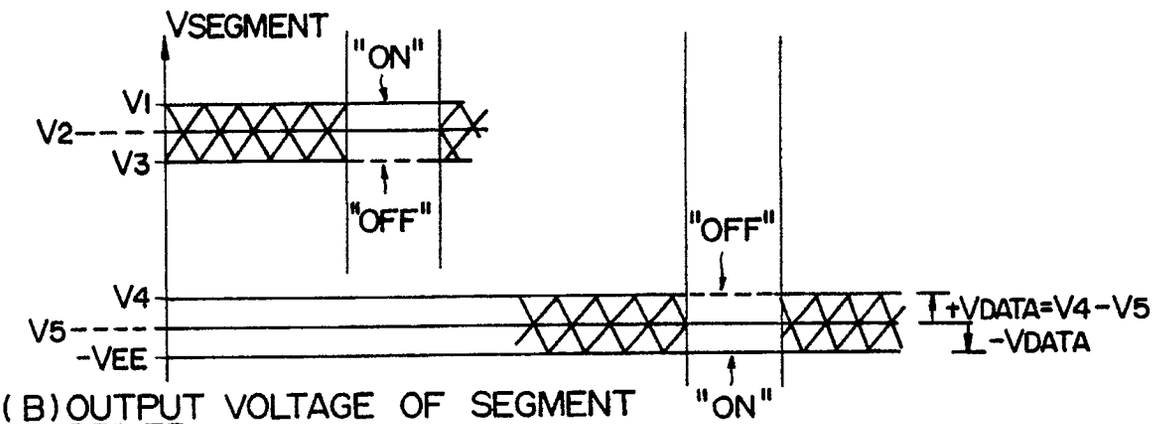

2b
COMMON DRIVER
COMMON DRIVER
LCD
1
2a
ENABLE*
PHASE SHIFT*
CLOCK*
DATA IN*
F"1"
FOLOGIC
PHOTO COUPLE
6
3a
SEGMENT DRIVER
SEGMENT DRIVER
3b
VDATA
-VDATA
-VLOGIC
F"1"
FOLOGIC
F"0"
5
LEVEL CONV.
VSCAN
VSCAN
-VLOGIC
VG
-VLOGIC
-VSCAN
-VSCAN
BRIDGE BUFFER
8
DATA IN
CLOCK
PHASE SHIFT
ENABLE
LCD CONTROL-LER
4
VG
-VLOGIC
VSCAN
-VSCAN
VDATD
-VDATA
-VLOGIC
11

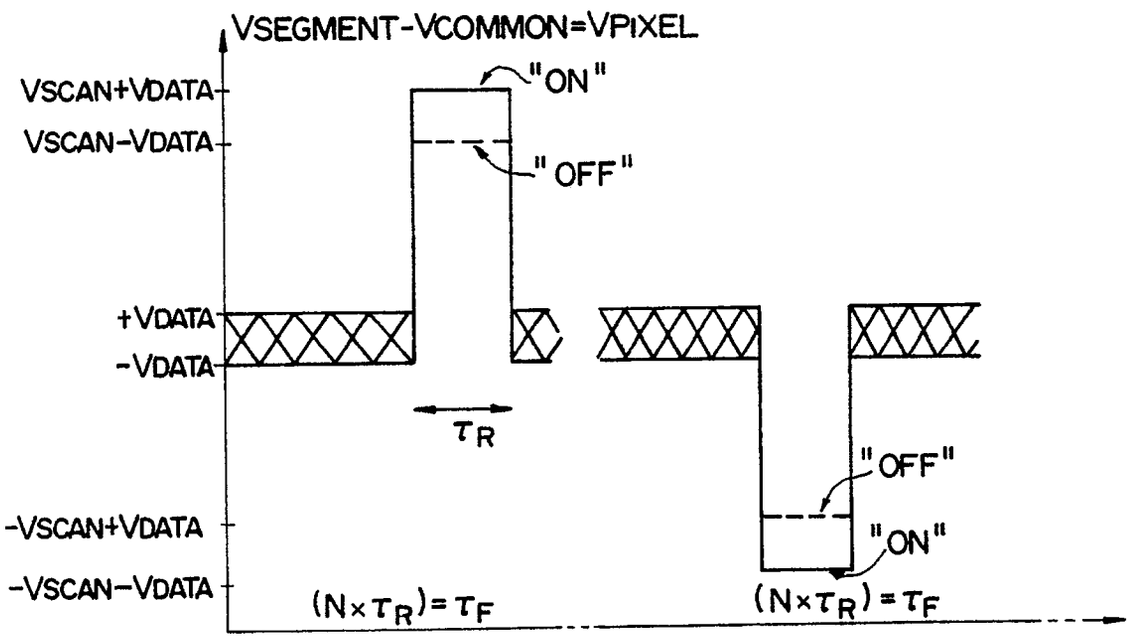
FIG. 2



(A) OUTPUT VOLTAGE OF COMMON DRIVER



(B) OUTPUT VOLTAGE OF SEGMENT DRIVER



(C) VOLTAGE APPLIED TO PIXEL

FIG. 3A

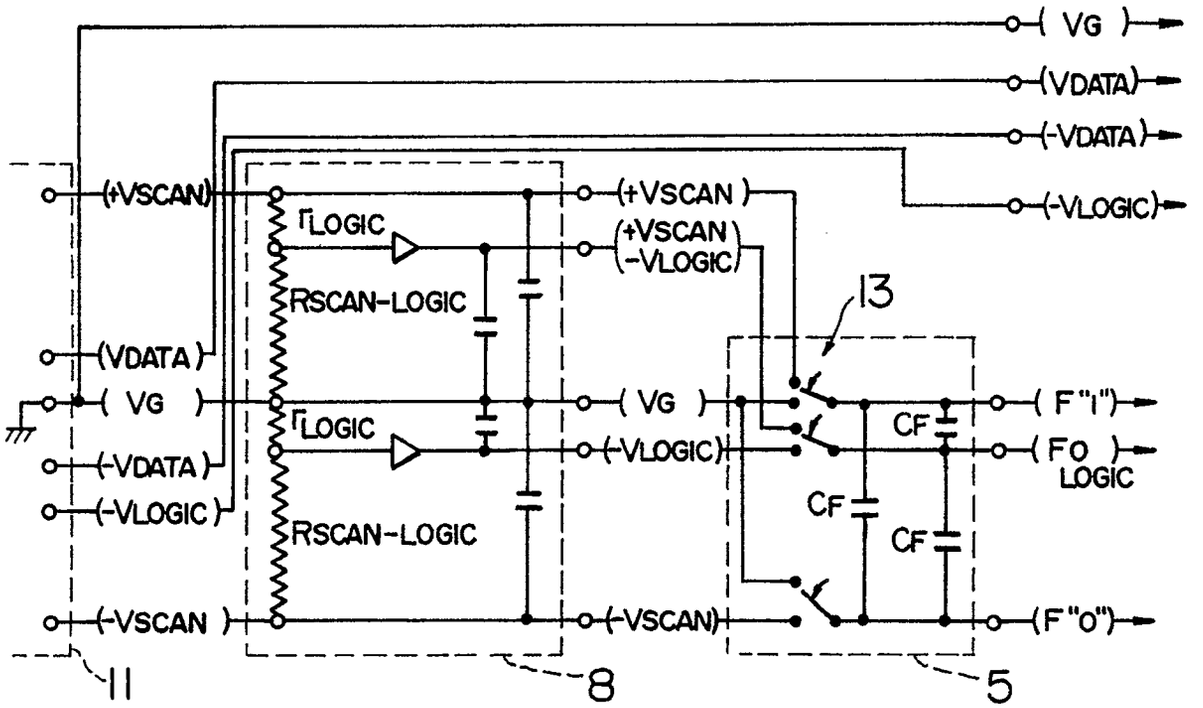

VG
VDATA
-VDATA
-VLOGIC
+VSCAN
VDATA
VG
-VDATA
-VLOGIC
-VSCAN
rLOGIC
RSCAN-LOGIC
rLOGIC
RSCAN-LOGIC
+VSCAN
+VSCAN
-VLOGIC
VG
-VLOGIC
-VSCAN
13
CF
CF
CF
F"1"
Fo
LOGIC
F"0"
11
8
5

FIG. 3B

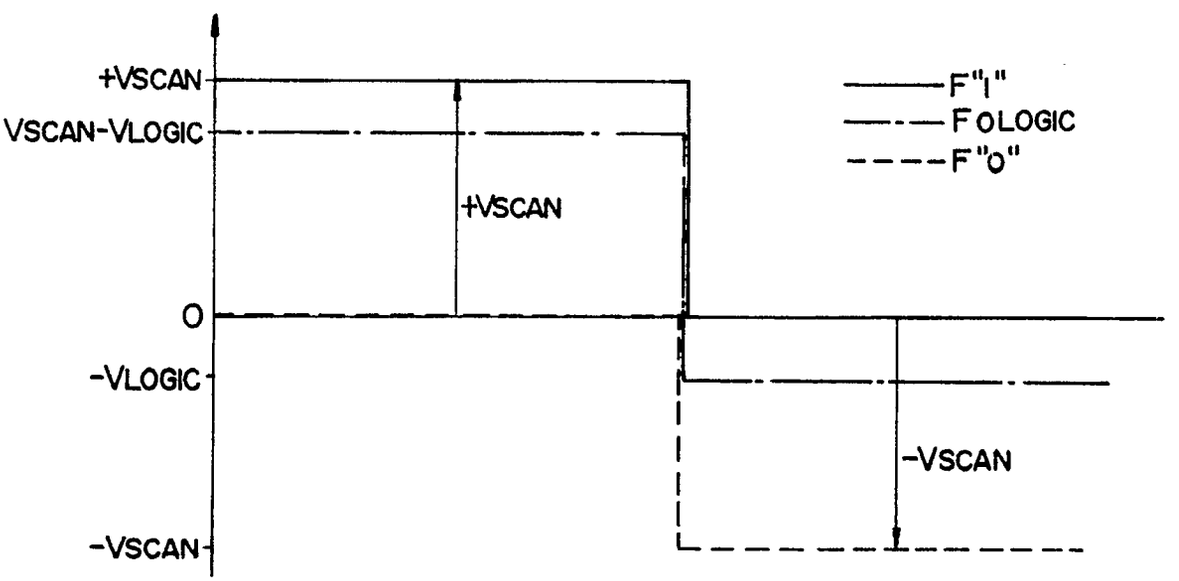

+VSCAN
VSCAN-VLOGIC
0
-VLOGIC
-VSCAN
+VSCAN
-VSCAN
F"1"
F OLOGIC
F"0"

FIG. 4A

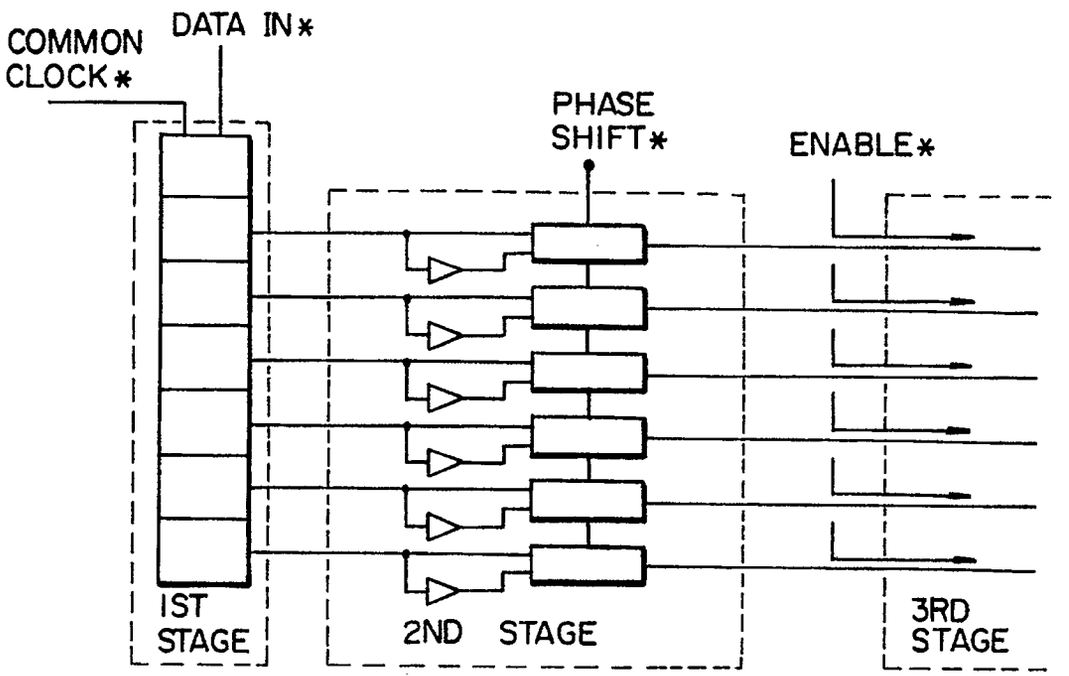

COMMON CLOCK*
DATA IN*
PHASE SHIFT*
ENABLE*
1ST STAGE
2ND STAGE
3RD STAGE

FIG.4B

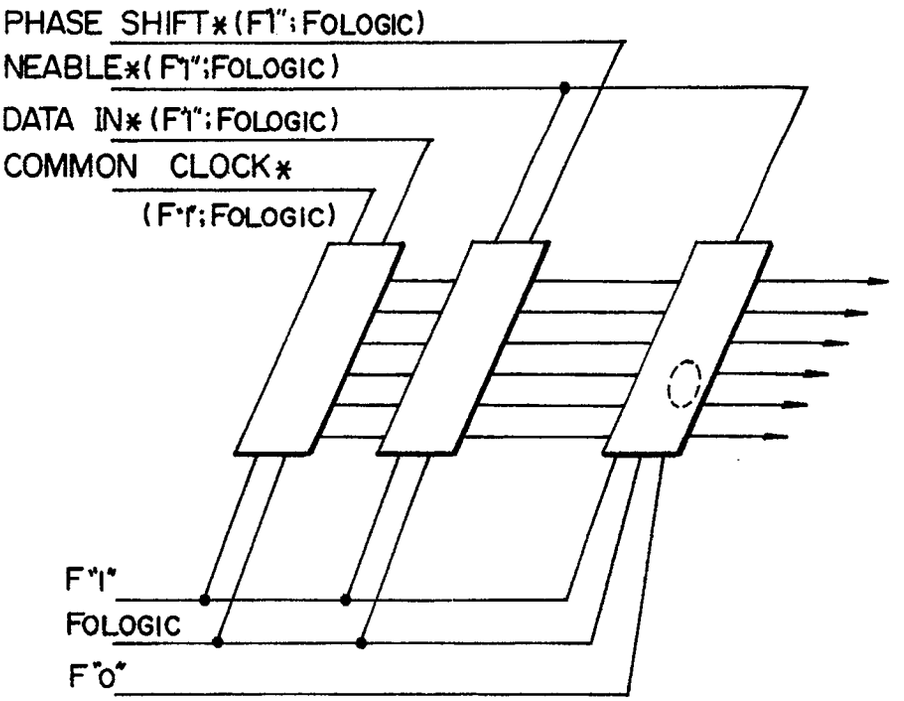

PHASE SHIFT*(F"1";FOLOGIC)
NEABLE*(F"1";FOLOGIC)
DATA IN*(F"1";FOLOGIC)
COMMON CLOCK*
(F"1";FOLOGIC)
F"1"
FOLOGIC
F"0"

FIG.4C

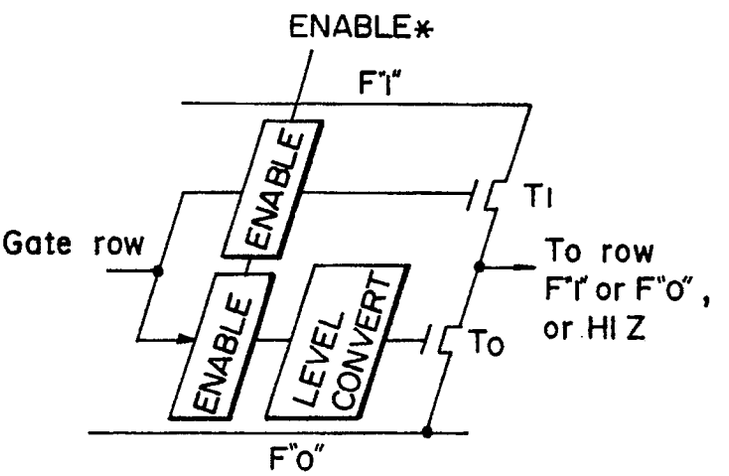

ENABLE*
F"1"
ENABLE
Gate row
ENABLE
LEVEL CONVERT
TI
To row
F"1" or F"0",
or HI Z
To
F"0"

FIG. 5

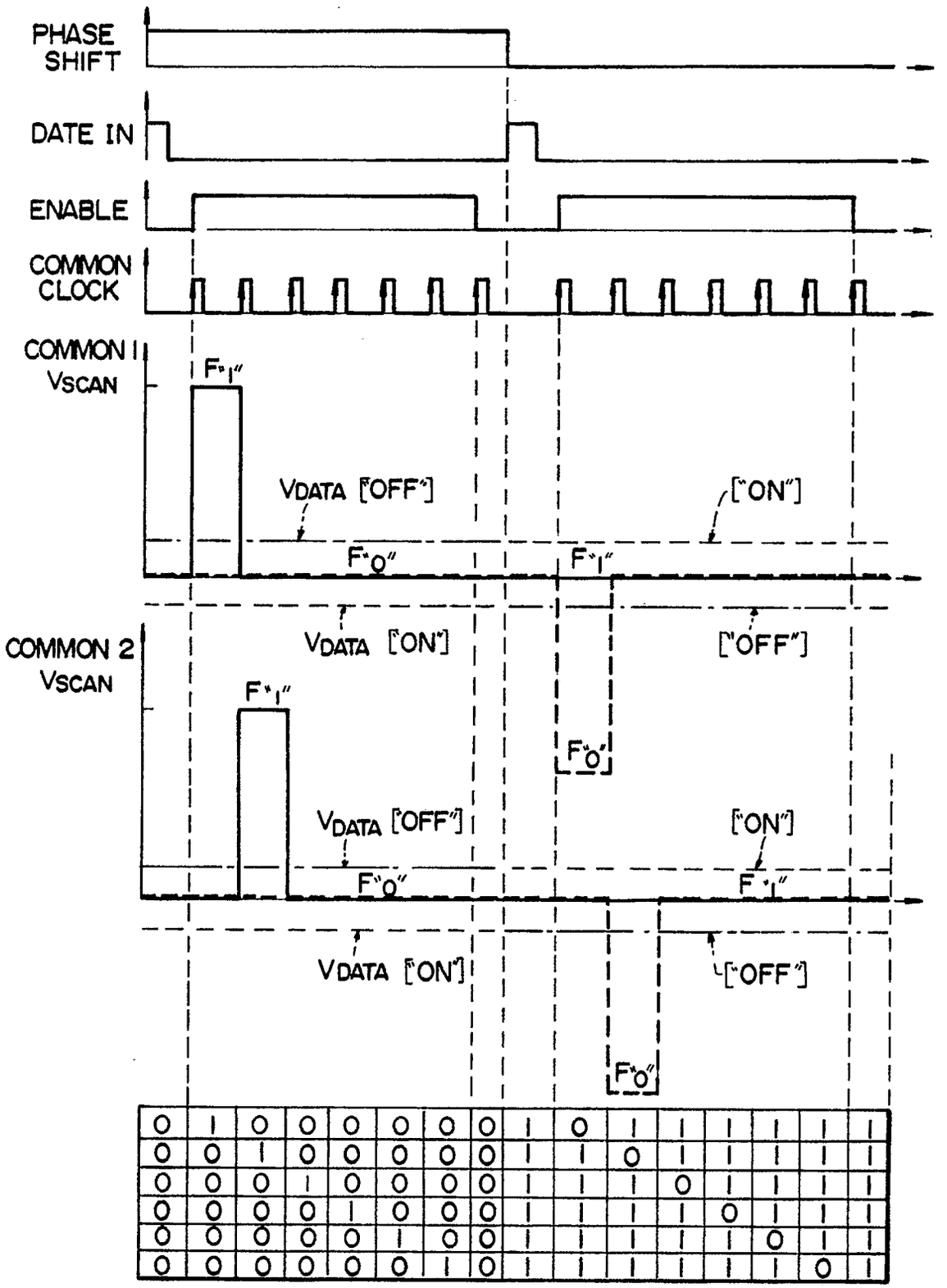

PHASE SHIFT
DATE IN
ENABLE
COMMON CLOCK
COMMON 1 VSCAN
F"1"
VDATA ["OFF"]
["ON"]
F"0"
F"1"
VDATA ["ON"]
["OFF"]
COMMON 2 VSCAN
F"1"
F"0"
VDATA ["OFF"]
["ON"]
F"0"
F"1"
VDATA ["ON"]
["OFF"]
F"0"

FIG. 6A

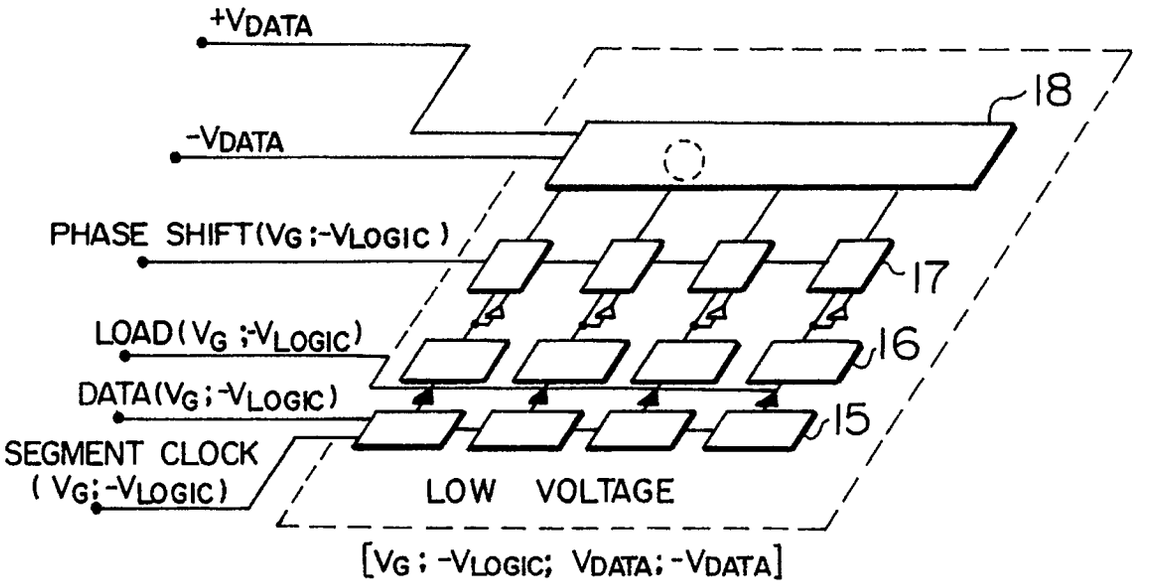
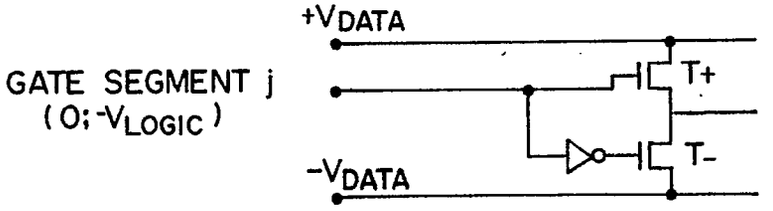

+VDATA
-VDATA
PHASE SHIFT(VG;-VLOGIC)
LOAD(VG;-VLOGIC)
DATA(VG;-VLOGIC)
SEGMENT CLOCK
(VG;-VLOGIC)
18
17
16
15
LOW VOLTAGE
[VG; -VLOGIC; VDATA; -VDATA]

FIG. 6B


+VDATA
GATE SEGMENT j
(O;-VLOGIC)
T+
T-
-VDATA