



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number : **0 453 158 A2**

(12)

EUROPEAN PATENT APPLICATION

(21) Application number : **91303128.2**

(51) Int. Cl.⁵ : **G06G 7/186**

(22) Date of filing : **09.04.91**

(30) Priority : **12.04.90 US 509657**

(43) Date of publication of application :
23.10.91 Bulletin 91/43

(84) Designated Contracting States :
DE FR GB IT

(71) Applicant : **Hewlett-Packard Company**
Mail Stop 20 B-O, 3000 Hanover Street
Palo Alto, California 94304 (US)

(72) Inventor : **Gilsdorf, Michael J.**
2040 NW Elder Street
Corvallis, OR 97330 (US)
Inventor : **Badyal, Rajeev**
172 NE Powderhorn
Corvallis, OR 97330 (US)

(74) Representative : **Colgan, Stephen James et al**
CARPMAELS & RANSFORD 43 Bloomsbury
Square
London WC1A 2RA (GB)

(54) **Switched-current integrator circuit**

(57) A switched-current integrator circuit (50) employs track-and-hold circuits (52,54) in which the gates of the current mirror FET switches (M1,M2) are connected together to form a common gate node (58) to double the effective holding capacitance. Additionally, the common gate node (58) is coupled to the input terminal (16) through a CMOS switch (62,64) so that parasitic clock feed-through is essentially cancelled to minimize DC offset voltages (V1,V3 in FIG. 4).

EP 0 453 158 A2

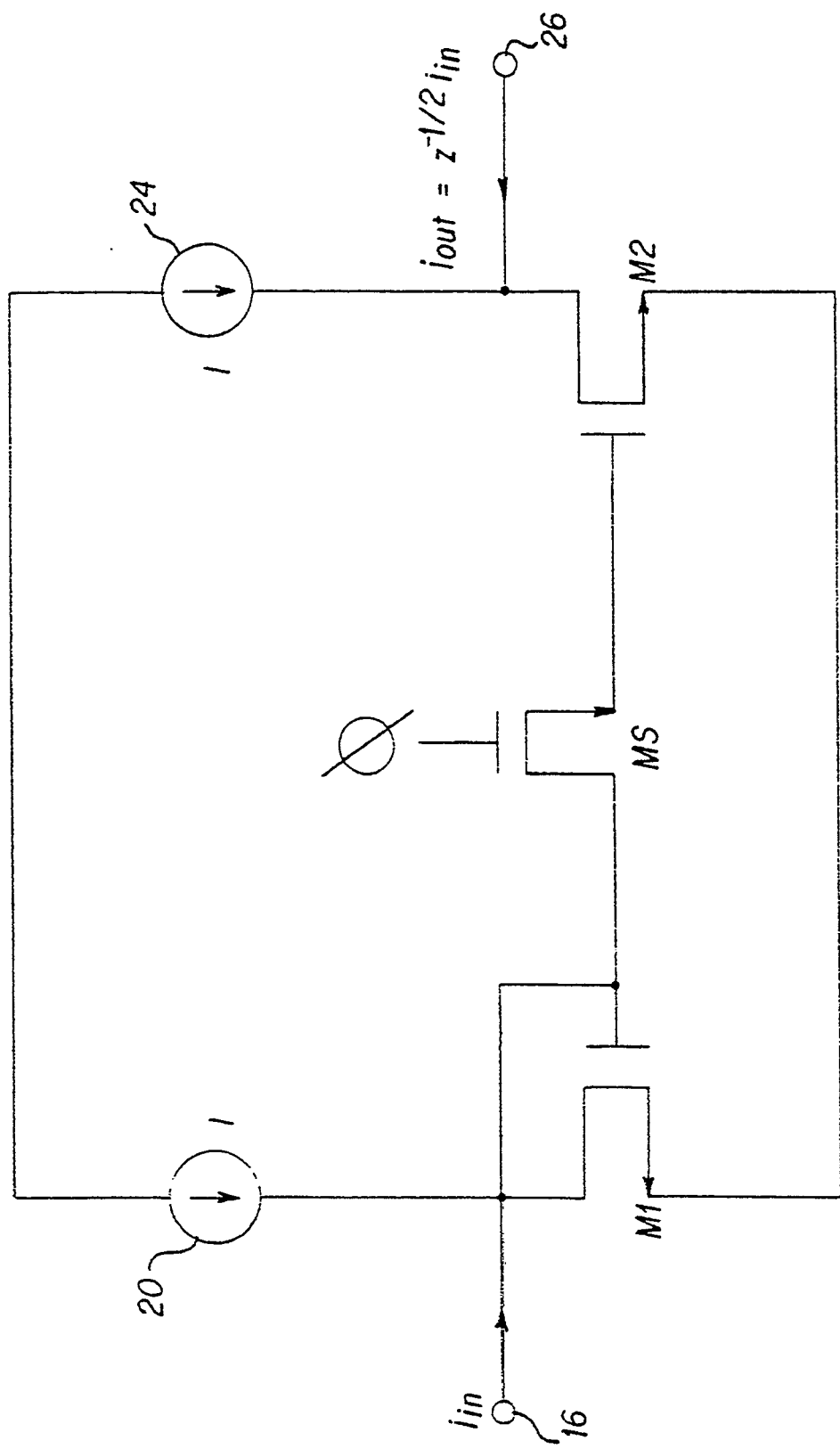


FIG. 1

BACKGROUND OF THE INVENTION

The present invention relates to the field of track-and-hold circuits and integrator circuits such as may be used, for example, in analog sampled-data signal processing applications. In particular, the invention includes improved switched-current track-and-hold circuits and methods.

CMOS switched-capacitor (SC) circuits are widely used in analog sampled-data signal processing applications. Although the SC technique achieves high accuracy, it requires extra processing steps to fabricate precision linear capacitors used in such circuits.

The concept of CMOS switched-current (SI) circuits for analog sampled-data applications was recently introduced. Rather than voltage operational amplifiers and precision capacitors, SI circuits employ wide-band current mirrors and a standard low-voltage digital CMOS process.

CMOS switched-current circuits are useful, for example, in building filters. In the SI technique, a filter coefficient is realized as the gain of a current mirror. To obtain high transconductances for high-frequency SI applications, wide, short-channel MOSFETs are used in the current amplifiers. See Fiez and Allstot, "FAM 12.5: A CMOS Switched-Current Filter Technique", proceedings of the ISSCC, February, 1990.

Known SI circuits, such as those shown by Fiez and Allstot, suffer distortion resulting from DC offset. An object of the present invention is to build track-and-hold circuits for use in integrators, analog filters and the like, using standard CMOS processes while minimizing offset and distortion.

SUMMARY OF THE INVENTION

The invention includes, in a switched-current track-and-hold circuit having a pair of switches arranged to form a current mirror, the steps of connecting the gate terminals of the current mirror switches together to form a common gate node; coupling the input terminal to the common gate node during track mode to accumulate charge on the common gate node responsive to the input current; and, while leaving the gates connected together, decoupling the input terminal from the common gate node to hold the accumulated charge on the common gate node during hold mode. Preferably, a CMOS switch is provided between the input terminal and the common gate node, so that coupling the input terminal includes turning the CMOS switch ON, and decoupling the input terminal includes turning the switch OFF.

A binary clock signal and a complement clock signal complementary to the binary clock signal are provided for driving the track-and-hold. One side (FET transistor) of the CMOS switch is coupled to receive the binary clock signal, and the other side of the

switch receives the complement clock signal. The entire CMOS switch thus turns ON or OFF in accordance with the state of the binary clock signal.

The foregoing method has the advantage of charging both current mirror gates during the track mode, and leaving the gates connected together during the hold mode, thereby doubling the effective holding capacitance of the circuit. Another advantage is that clock feedthrough through the CMOS switch while the clock is going high is essentially cancelled while the complement clock is going low, due to the symmetry of the CMOS device.

Another aspect of the invention is a novel track-and-hold circuit that incorporates the foregoing methods. The circuit includes a pair of FET switches arranged in a current mirror configuration. The two FET gate terminals are connected together to form a common gate node. A CMOS switch is disposed between the signal input terminal and the common gate node for selectively coupling the signal input terminal to the common gate node.

Yet another aspect of the invention is an SI integrator circuit comprising two stages, each stage including a track-and-hold circuit as described above.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment which proceeds with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a known switched-current (SI) track-and-hold circuit.

FIG. 2 is a schematic diagram of a known SI integrator circuit.

FIG. 3 is a schematic diagram of an improved SI integrator circuit according to the present invention.

FIG. 4 is a simulation plot showing settling of the circuits of FIGS. 2 and 3 to steady-state conditions.

FIG. 5 is a simulation plot for the circuits of FIG. 2 and FIG. 3, showing theoretical DC offset voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a schematic diagram of a known switched-current track-and-hold circuit. In the circuit, a pair of switch devices M1 and M2 are arranged in a current mirror configuration. Current sources 20, 24 each provide a predetermined current I to the respective switches M1, M2. A third switch MS is disposed in series between the gates of switches M1 and M2.

Switch MS is controlled by a binary clock signal ϕ .

A signal input terminal 16 receives an input current i_{in} . In operation, when switch MS is ON (track mode), it presents essentially a short circuit between

the gates of switches M1 and M2. A current $I + i_{in}$ flows through device M1. Because V_{GS} (M1) is equal to V_{GS} (M2), an equal current $(I + i_{in})$ flows through switch M2, thus mirroring the first current. An output terminal 26 is connected between current source 24 and M2. Since the two current sources are equal, an output current i_{out} equals i_{in} . The output current thus tracks the input current while MS is ON (track mode).

When $\overline{\Phi}$ changes state, MS is switched OFF, thereby isolating the gate of M2 from the input circuitry. This is the hold mode. An essentially constant voltage V_{GS} (M2) remains on the switch M2, so that the current $(I + i_{in})$ continues to flow through M2. Output current i_{out} thus continues to be equal to the earlier i_{in} , i.e. the value of i_{in} during the track mode, regardless of the present value of i_{in} .

FIG. 2 is a schematic diagram of a known switched-current integrator circuit 10. The circuit comprises generally a first track-and-hold stage 12 coupled to a second track-and-hold stage 14. Each of the stages 12, 14 is similar to the circuit of FIG. 1 described above.

Referring to the first stage 12, a signal input terminal 16 is provided to receive an input current i_1 . A first FET switch M1 and a second FET switch M2 are arranged in a current mirror configuration. A first current source 20 provides a predetermined current I to the first FET input terminal at node 22. A switch MS1 is disposed in series with the gates of FET switches M1 and M2. Switch MS1 is controlled by a binary clock signal Phase 1.

While the clock signal Phase 1 is high, MS1 is ON, and the current through M1 is mirrored in M2. When Phase 1 goes low (hold mode), MS1 is OFF, and the same current as before persists in M2, independent of the current in M1.

The second track-and-hold circuit 14 similarly includes switches M3 and M4, arranged in a current mirror configuration, a switch MS2 disposed in series with the gates of switches M3 and M4, and a second current source 30. Current sources 20 and 30 each provide a stable reference or bias current I . Switch MS2 is controlled by a clock signal $\overline{\text{Phase 2}}$ (complement of Phase 2). Phase 1 and Phase 2 are non-overlapping binary clock signals.

The SI integrator circuit of FIG. 2 operates essentially as follows. From the topology, a current in M2 also flows in M3, assuming i_2 is zero, so the output current of the first stage 12 is the input current to the second stage 14. During clock Phase 1 (time t_1), input current i_1 is tracked so that $i_{M2} = I + i_1$. That current persists in M2, and therefore in M3, after Phase 1 goes low.

When Phase 2 goes high, $\overline{\text{Phase 2}}$ goes low, turning MS2 ON, thereby coupling M3 to M4. The current in M4 is therefore $I + i_1(t_1)$. Current source 30 subtracts current I , so that the feedback current along

path 40 is $i_1(t_1)$. When Phase 2 goes low (Phase 2 goes high), the current in M4 persists, independent of the current in M3.

When Phase 1 next goes high (time t_2), the feedback current is summed in node 22 with the new input current $i_1(t_2)$, so that the current in M1 becomes $I + i_1(t_1) + i_1(t_2)$. The input current thus is integrated over time. The process repeats over subsequent clock cycles in like fashion.

FIG. 3 shows an improved integrator circuit according to the present invention. The circuit elements in FIG. 3 which are common to those shown in FIG. 2 have like reference numbers. Referring to FIG. 3, a first track-and-hold stage 52 is coupled to a second track-and-hold stage 54 in the same fashion as the corresponding circuitry of FIG. 2. The gate of the first switch M1 is connected directly to the gate of the second switch M2 to form a common gate node 58.

A pair of complementary FET devices 62,64 are coupled in parallel to each other between the input terminal 16 and the common gate node 58. Preferably, the FET devices 62,64 comprise a CMOS switch. In much the same manner, the second track-and-hold stage 54 has the gates of switches M3 and M4 connected together to form a common gate node 60. A second pair of complementary FET switches 68,70 are connected in parallel to each other between node 56 and common gate node 60. Node 56 effectively is the input terminal to the second stage. This novel circuitry has several advantages over the prior art. These will be described with respect to track-and-hold circuit 52 with the understanding that the second circuit 54 operates in essentially the same manner.

In the first stage 52, the first FET switch 62 is controlled by a clock signal Phase 1. The complementary FET switch 64 is controlled by a second clock signal $\overline{\text{Phase 1}}$, which is the complement of Phase 1. Accordingly, when clock signal Phase 1 is high, both FET switches 62,64 are ON, thereby coupling the input terminal 16 to the common gate node 58. While Phase 1 is high (track mode), charge accumulates on the gates of M1 and M2, charging the common gate node 58 to a voltage V_{gs} responsive to the current $I + i_1$.

When Phase 1 goes low, both FET switches 62,64 are turned OFF, thus isolating the common gate node 58 from the signal input terminal 16. The resulting holding capacitance is equal to the sum of the gate capacitances of M1 and M2, since the gates are charged in parallel. Assuming that M1 and M2 have the same geometries in FIG. 3 as in FIG. 2, the effective holding capacitance of the new circuit is twice that of the old circuit, in which only the gate capacitance of M2 was available for holding V_{gs} . Increased holding capacitance results in improved accuracy in a track-and-hold circuit. The increased holding capacitance is achieved here without increasing circuit size.

Another advantage of the circuit of FIG. 3 is a

reduction in DC offset voltage. DC offset voltage results, in the circuit of FIG. 2, from parasitic capacitances that couple the gate of MS1 to its source and drain terminals. Because of these parasitic capacitances, the transitions of clock signal Phase 1 give rise to a parasitic current which adds charge to the gate of M2. This results in a corresponding DC offset voltage.

Referring to the new circuit of FIG. 3, the first FET device 62 also has parasitic capacitances which couple the gate to the source and drain terminals. The second FET device 64 similarly has parasitic capacitances. The parasitic capacitances inherent in device 62 are approximately the same as those of device 64 due to the symmetry of construction of such devices.

In operation, when the Phase 1 clock signal makes a low to high transition, a parasitic current flows from the device 62 gate terminal into the common gate terminal 58. However, when Phase 1 makes a high to low transition, an approximately equal current flows out of node 58 through the gate terminal of device 64. The transition of the complement clock effectively cancels the feedthrough effect of the Phase 1 clock. This results, as will be shown below, in substantial reduction in offset voltage as compared to the prior art.

The same principle applies in the second track-and-hold circuit 54 with respect to the complementary FET device 68,70. Preferably, the complementary pairs of FET devices are CMOS devices, though the same principles are applicable to any FET devices such as SOS, Gallium Arsenide, and so on.

Although the improved track-and-hold circuit is shown in the context of an integrator circuit, it may be used advantageously in any application where a improved switched-current track-and-hold circuit with minimum clock feedthrough is desired.

FIG. 4 is a simulation plot of voltage versus time, showing settling of the circuits of FIGS. 2 and 3 to steady state conditions. In the plot, trace number 1 indicates the voltage at the common gate node 58 of FIG. 3, and trace number 3 indicates the voltage at the second stage common gate node 60 of FIG. 3. Trace number 2 indicates the voltage at the gate of M2 in the prior art circuit of FIG. 2. Finally, trace 4 indicates the voltage at the gate of M4 in the circuit of FIG. 2. Dashed trace 5 indicates the theoretical or ideal v_{gs} voltage.

The plot of FIG. 4 thus provides for comparison of v_{gs} offset voltages between the circuits of FIG. 2 and FIG. 3. It may be observed that both the prior art circuit voltages (traces 2 and 4) and the improved circuit voltages (traces 1 and 3) are approximately symmetric about the ideal voltage (trace 5). Comparing the steady-state voltages (time > 14 microseconds), the plot shows a total DC offset voltage for the circuit of FIG. 2 of approximately 210 millivolts (the voltage difference between traces 2 and 4). The offset voltage is

only about 40 millivolts for the circuit of FIG. 3 (the voltage difference between traces 1 and 3).

The traces of FIG. 4 also show that the settling time for the circuit of FIG. 2 is on the order of 8 microseconds, whereas the settling time of the circuit of FIG. 3 is on the order of 2 microseconds, a substantial speed improvement.

FIG. 5 is a simulation plot showing the theoretical v_{gs} steady state voltage for the circuits of FIGS. 2 and 3, approximately 2.23 volts. This is the voltage level of trace 5 in FIG. 4.

Having illustrated and described the principles of our invention in a preferred embodiment thereof, it should be readily apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications coming within the spirit and scope of the accompanying claims.

Claims

1. In a switched-current track-and-hold circuit (12,14) having an input terminal (16) for receiving an input current and having first and second switches (M1,M2) arranged to form a current mirror, each switch having a respective gate terminal, a method of tracking and holding the input current comprising:
 - connecting the gate terminals of the first and second switches (M1,M2) together to form a common gate node (58);
 - coupling the input terminal (16) to the common gate node (58) to accumulate charge on the common gate node responsive to the input current; and
 - decoupling the input terminal from the common gate node while leaving the gate terminals connected together, to hold the accumulated charge on the common gate node.
2. A method according to claim 1 including providing first and second complementary FET switch devices (62,64), coupled in parallel to each other between the input terminal (16) and the common gate node (58), and wherein:
 - coupling the input terminal includes turning the first and second FET switches ON; and
 - decoupling the input terminal includes turning the first and second FET switches OFF.
3. A method according to claim 2 wherein the first and second FET switch devices (62,64) together comprise a CMOS switch.
4. A method according to claim 1 wherein said coupling and decoupling the input terminal includes: providing a binary clock signal (Phase 1)

- and a complement clock signal ($\overline{\text{Phase 1}}$) complementary to the binary clock signal;
 providing first and second complementary FET switch devices (62,64), coupled in parallel to each other between the input terminal (16) and the common gate node (58), each of said FET switch devices having a respective gate terminal (72,74);
 coupling the first FET switch gate terminal (72) to receive the binary clock signal (Phase 1); and
 coupling the second FET switch gate terminal (74) to receive the complement clock signal ($\overline{\text{Phase 1}}$) so that both FET switch devices are ON when the binary clock signal is HIGH and both FET switch devices are OFF when the binary clock signal is LOW.
5. A switched-current track-and-hold circuit comprising:
 a first current source (20) for providing a predetermined current;
 a signal input terminal (16) for receiving an input current;
 a first FET (M1) having an input terminal and a gate terminal, the FET input terminal coupled to the first current source and coupled to the signal input terminal;
 a second current source (24) for providing a second predetermined current;
 a second FET (M2) having an input terminal and a gate terminal, the second FET input terminal coupled to the second current source;
 the first and second FET gate terminals being connected together to form a common gate node (58); and
 switch means (62,64) disposed between the signal input terminal and the common gate node for selectively coupling the signal input terminal to the common gate node.
6. A switched-current track-and-hold circuit according to claim 5, wherein the switch means consists of a CMOS switch.
7. A switched-current integrator circuit comprising:
 first and second track-and-hold stages (52,54), each stage having an input terminal (16,56) and an output terminal (56,80), the first stage output terminal being coupled to the second stage input terminal (56) and the second stage output terminal (80) being coupled to the first stage input terminal (16) for providing a feedback current;
 each stage including a pair of FET devices (M1-M2, M3-M4) arranged in current mirror configuration, each FET having a gate terminal;
 in each stage, the FET gate terminals
- being connected together to form a respective common gate node (58,60); and
 each stage including switch means (62,64,68,70) disposed between the input terminal and the common gate node for selectively coupling the input terminal to the common gate node.
8. A switched-current integrator circuit comprising:
 a first current source (20) for providing a predetermined current;
 an input terminal (16) for receiving an input current;
 a first FET (M1) having an input terminal and a gate terminal, the input terminal coupled to the first current source and coupled to the input terminal;
 a second FET (M2) having an input terminal and a gate terminal;
 the first and second FET gate terminals being fixed together to form a first common gate node (58);
 a first switch means disposed between the input terminal and the first common gate node (62,64) for selectively coupling the input terminal to the first common gate node;
 a third FET (M3) having an output terminal and a gate terminal, the output terminal coupled to the second FET input terminal;
 a second current source (30) for providing a second current equal to the predetermined current;
 a fourth FET (M4) having an output terminal and a gate terminal, the output terminal coupled to the second current source;
 the third and fourth FET gate terminals being connected together to form a second common gate node (60);
 a second switch means (68,70) disposed between the second FET input terminal and the second common gate node for selectively coupling the second FET input terminal to the second common gate node; and
 the fourth FET output terminal (80) being coupled to the input terminal (16) to provide a feedback current.
9. A switched-current integrator circuit according to claim 8, wherein the first and second switch means each consists of a CMOS switch.

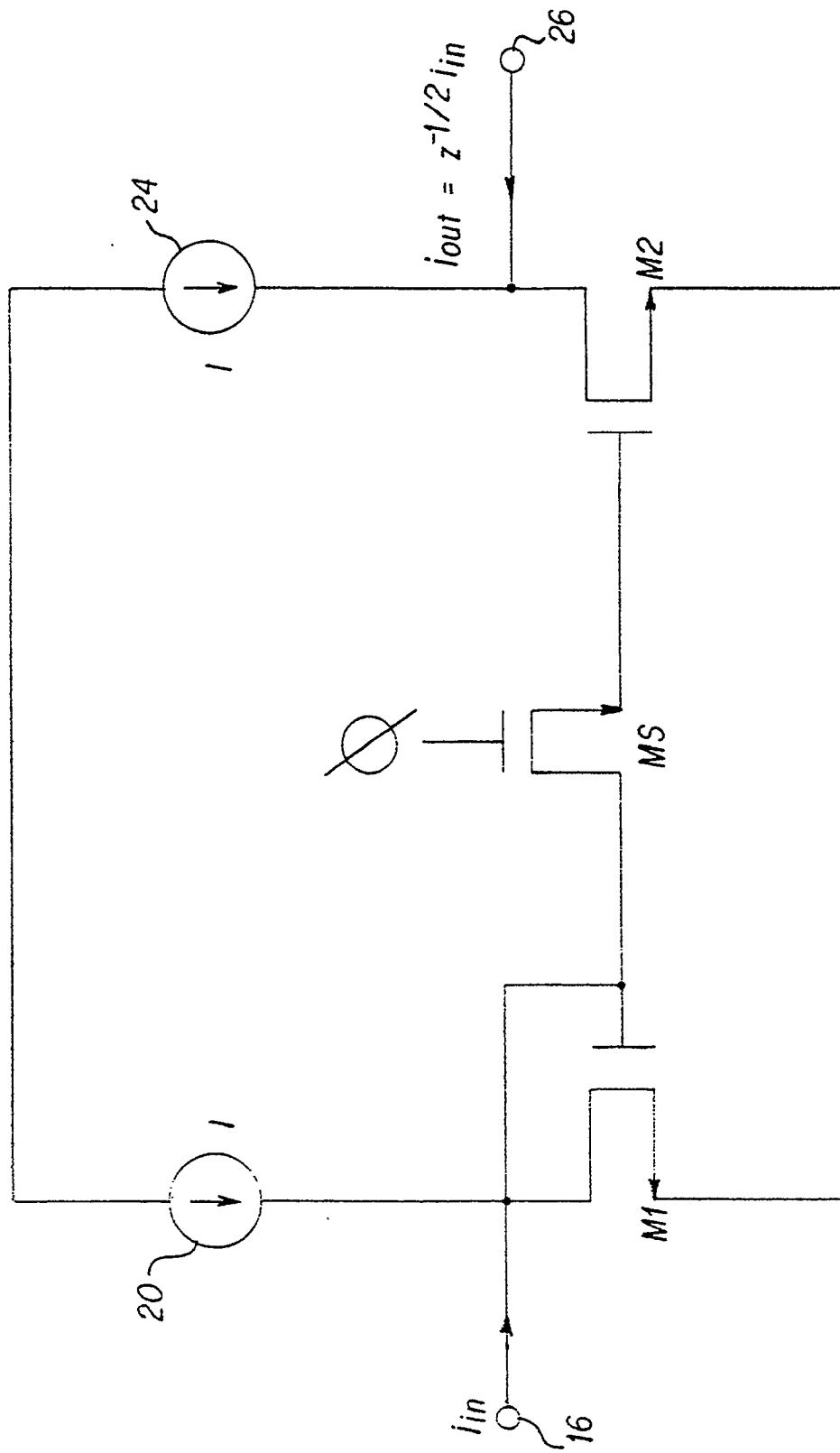


FIG. 1

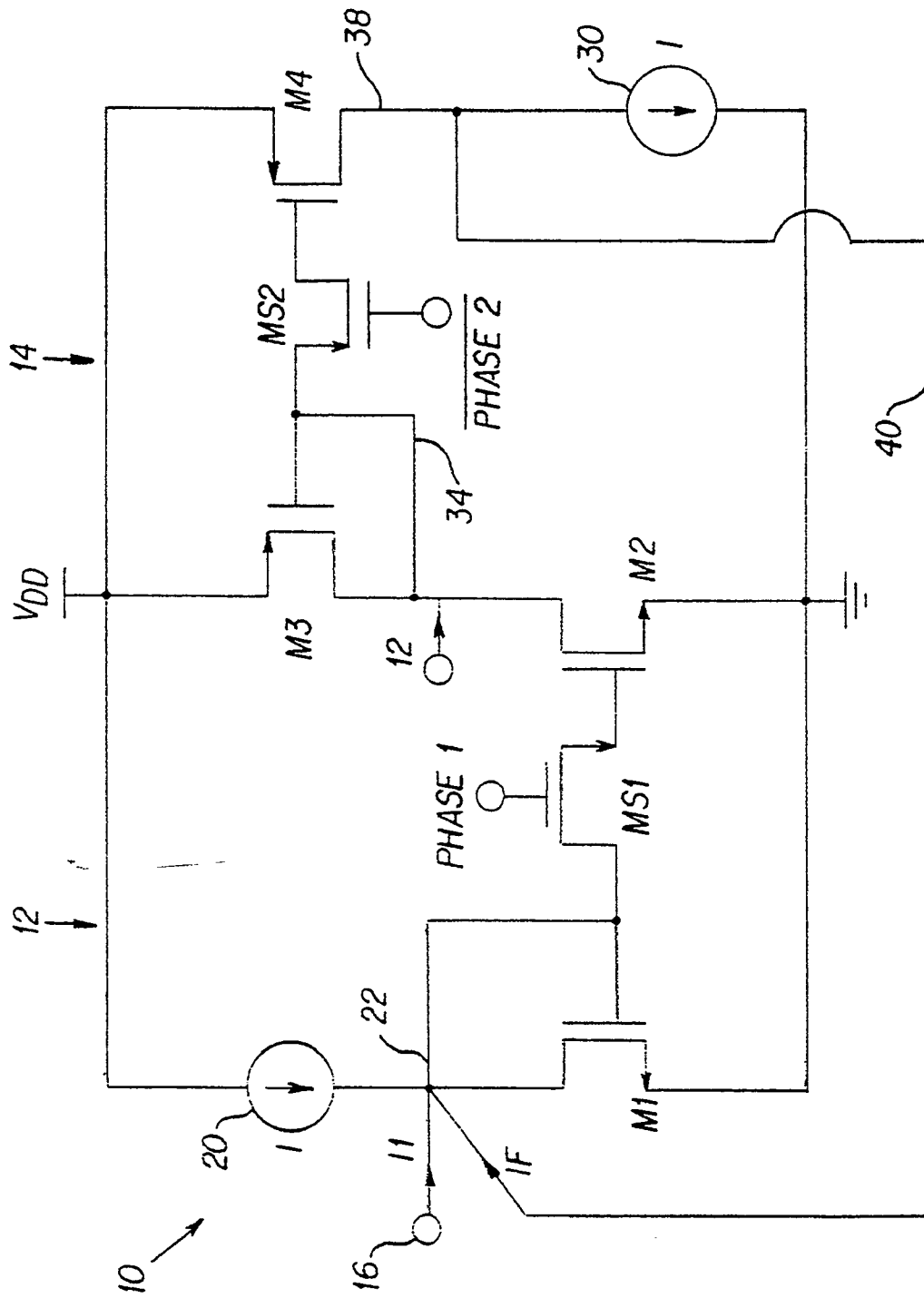
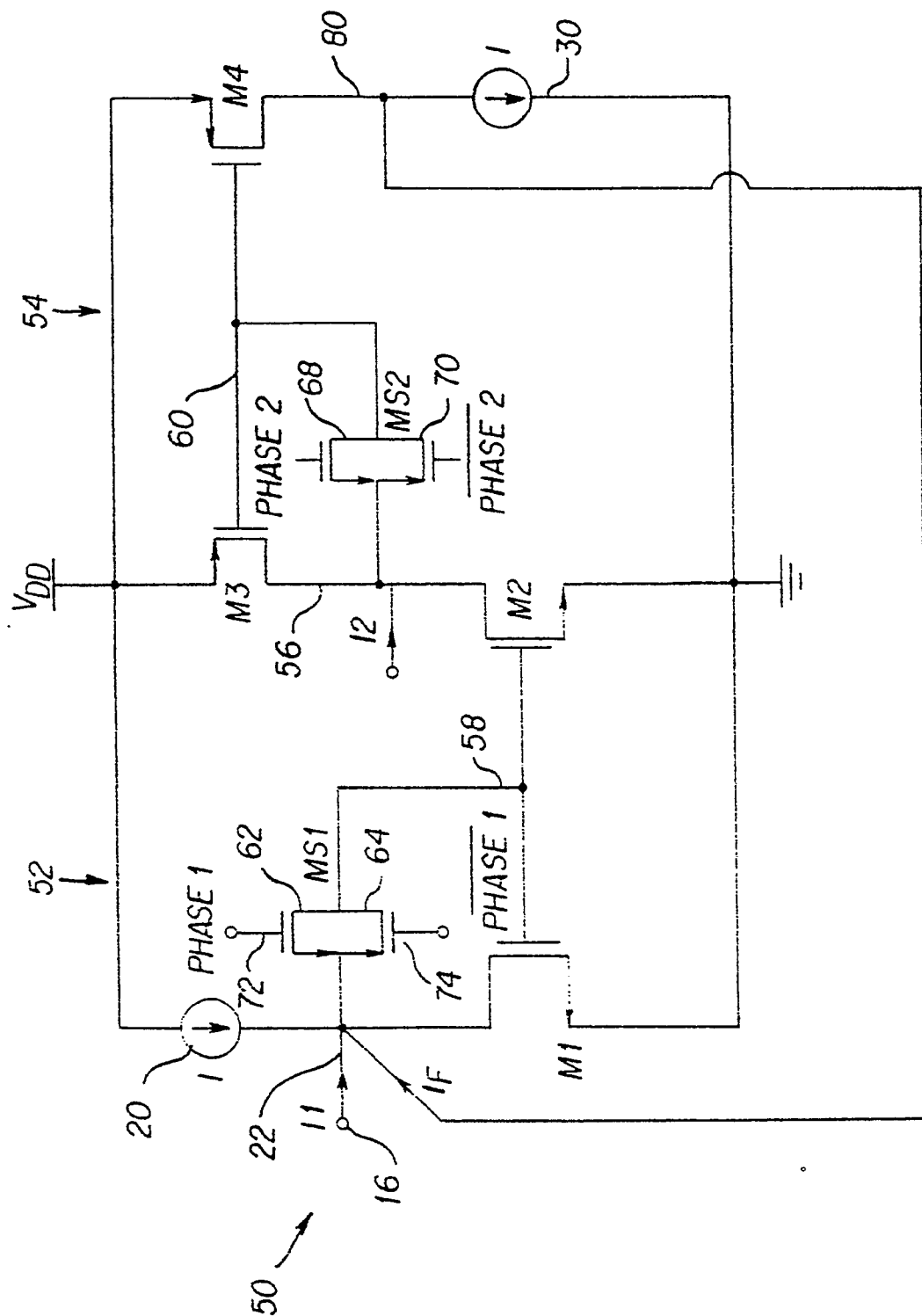


FIG. 2



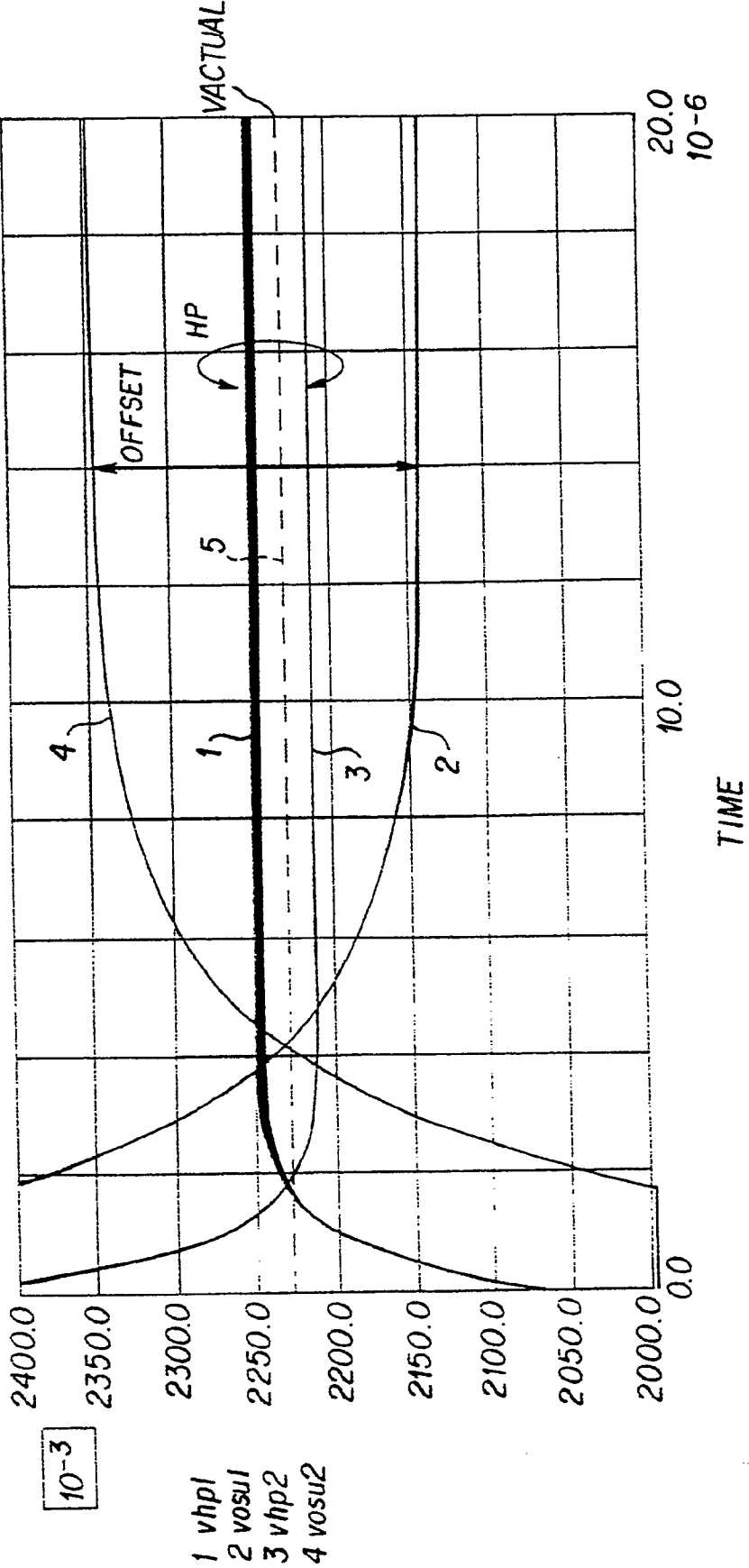


FIG. 4

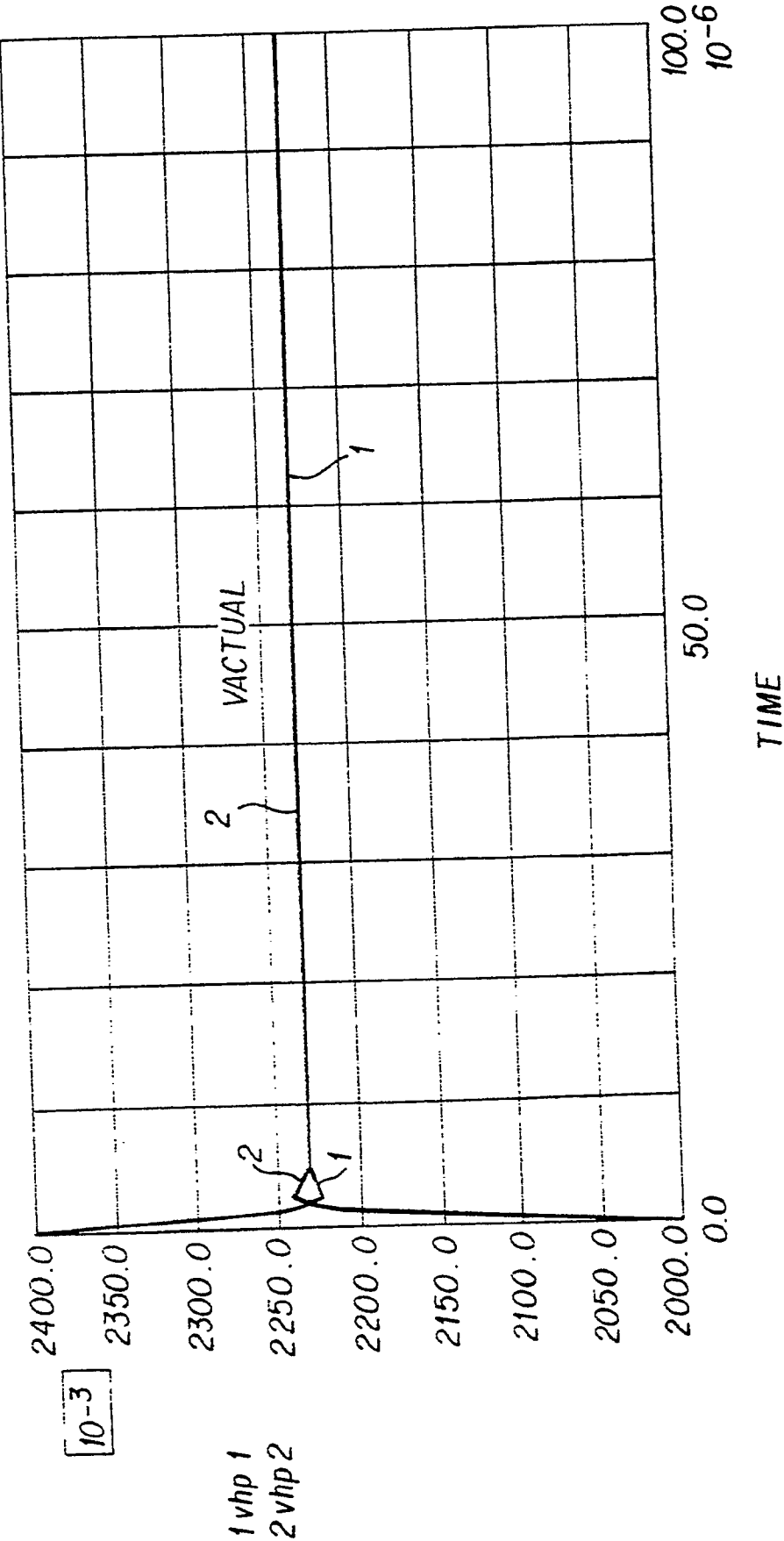


FIG. 5