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(54) **A method and apparatus for scrambling/descrambling a video signal.**

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EP 0 455 405 B1

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Description

The present invention relates to a method and an apparatus for scrambling and descrambling a composite video signal, and more particularly to a method and an apparatus for bit-scrambling and again bit-descrambling a digital signal into which the composite video signal is converted thereby.

There have been various systems for scrambling a composite video signal to prohibit illegally watching TV which is supplied by commercialized system. Among them, there has been used the most generally a line rotation system wherein the scrambled composite video signal is re-scrambled to be descrambled to be the original composite signal. Accordingly, operation principles of a scrambler and a descrambler are basically the same, and thus the operation principle of the descrambler will be described hereinafter only.

The descrambler employed in the above-mentioned conventional line rotation system is shown in Fig. 1. As shown in the drawing, the descrambler comprises an A/D converter 1 adapted to convert a composite video signal Vin inputted therein into 8 bit digital signals; two line memories 2 and 3 adapted to store the digital signals from said converter 1 alternately; a synchronous divider 4 adapted to divide said composite video signal Vin inputted therein into a horizontal synchronous signal H_{sync} and a vertical synchronous signal V_{sync} ; a clock generator 5 adapted to generate a sampling clock in response to said horizontal synchronous signal H_{sync} from said synchronous divider 4 to apply said sampling clock to said A/D converter 1; a D/A converter 6 adapted to receive and convert the digital signals from said line memories 2 and 3 into an analog signal and to receive the sampling clock from said clock generator 5 ; a data slicer 7 adapted to extract from said composite video signal Vin initial data coded during a vertical blanking interval VBI thereof every each field thereof in order togenerate random numbers ; a data RAM 8 adapted to store the coded initial data from said data slicer 7 ; a microprocessor 9 adapted to decode said coded initial data stored in said data RAM 8 ; a 10 bit random number generator 10 adapted to receive said vertical synchronous signal V_{sync} from said synchronous divider 4 and the decoded initial data from said microprocessor 9 and generate 10 bit random numbers ; and an address generator 11 adapted to receive output signals from said 10 bit random number generator 10 and apply address signals to the line memories 2 and 3.

The operation of the descrambler with the above-mentioned construction will now be described.

As shown in Fig. 2A, upon receiving a scrambled composite video signal Vin, the A/D converter 1 converts it into 8 bit digital signals and sends the digital signals out to the line memories 2 and 3 alternately. The line memories 2 and 3 which receive the 8 bit digital signals alternately store them alternately in response to address signals from the address generator 11 and send said stored digital signals out to the D/A converter 6. The D/A converter 6 converts the received digital signals into an analog signal and generates a descrambled composite video signal Vout which is the same as the original composite video signal, as shown in Fig. 2B.

It is noted that address values for the line memories 2 and 3 correspond to a point P shown in Fig. 2B.

A signal of waveform shown in Fig. 2A is scrambled about the point P corresponding to the address values. Accordingly, if a 10 bit random number generator in the scrambler (not shown) which is the same as the 10 bit random number generator 10 generates address values corresponding to the point P on each line randomly, an image from such scrambled video signal can not be recognized at all, like a noise image on screen.

On the other hand, the above-mentioned random number generator of the scrambler as a transmitter transmits the scrambled composite video signal carried with initial data coded during the vertical blanking interval thereof every field thereof. Accordingly, the data slicer 7 receives the scrambled composite video signal Vin and extracts the coded initial data which is in turn stored into the data RAM 8. The microprocessor 9 decodes the coded initial data stored in the data RAM 8 and supplies it to the 10 bit random number generator 10 as a control signal to control it. Therefore, the value of the point P generated in the scrambler as a transmitter is read precisely by the descrambler as a receiver. This is possible because the scrambler as a transmitter and the descrambler as a receiber have the same construction including the 10 bit random number generator 10 so that if initial data values provided for each field are the same in both devices, namely, values of the point P generated at each horizontal scanning line are the same in both devices. The generated value for the point P is supplied to the address generator 11 which in turn supply address signals to the line memories 2 and 3 in order to read a data signal stored in the line memories 2 and 3 as shown in Fig. 2A, as a data signal as shown in Fig. 2B. The reason why two line memories 2 and 3 are used is to perform read and write operations on alternate horizontal lines alternately. Also, the A/D converter 1 and the D/A converter 6 are intended for use of 8 bits and sample of 1024 per horizontal line(10 address lines), although nonlimited thereto.

In the above conventional construction, however, if the address value for the point P is generated by the random number generator, as above-mentioned, a certain point during the video signal interval corresponding to the point P is cut out and then the composite video signal is scrambled about the point P in a line rotation manner. At the cut part of the video signal, high frequency component to be noise is generated. As a result, it results in degrading image quality at the cut part. In addition, there is a disadvantage of expensive manufacture

cost which is coused by the use of expensive two line memories. Furthermore, it can not prohibit the non-subscribers from watching illegally, because the composite video signal is simply scrambled by using two line memories.

Therefore, it is an object of the present invention to provide a method and an apparatus for scrambling and descrambling a digitalized composite video signal by using a transform matrix. It is another object of the present invention to provide a method and an apparatus for scrambling and descrambling the digitalized composite video signal which is capable of avoiding any deterioration of the image quality, increase of cost, and illegally watching of non-subscribers.

In accordance with one aspect of the present invention, there is provided an apparatus for scrambling a video signal comprising an A/D converter for receiving a composite video signal to be bit-scrambled from an external equipment and converting the composite video sinal into a digital signal for bit-scrambling ; a multiplexing means for inputting the digital signal from said A/D converter and outputting the digital signal in a bit order in response to an external select signal ; a D/A converter for receiving the digital signal outputted from said multiplexing means and converting said outputted digital signal into an analog signal; a synchronous divider for receiving said composite video signal and dividing the composite video signal into a vertical synchronous signal and a horizontal synchronous signal ; a clock generator for receiving the horizontal synchronous signal from said synchronous divider to generate a clock signal and supplying the clock signal to said A/D converter and said D/A converter ; an initial data generating means for receiving said composite video signal, extracting from said composite video signal initial data coded during a vertical blanking interval thereof every field thereof, and decoding the extracted coded initial data; a horizontal blanking interval detector for receiving the horizontal synchronous signal from said synchronous divider, detecting a horizontal blanking interval from said horizontal synchronous signal, and outputting a low signal during the detected horizontal blanking interval ; a random number generator for generating random numbers of a predetermined bit number, upon receiving the vertical synchronous signal from said synchronous divider and the decoded initial data from said initial data generating means ; and an AND logic operating means including a plurality of AND gates each having one input terminal for receiving a different bit signal from said random number generator, its other input terminal for receiving an output signal from said horizontal blanking interval detector, its output terminal coupled in common to said multiplexing means for applying said external select signal.

In accordance with another aspect of the present invention, there is provided an apparatus for descrambling a video signal comprising an A/D converter for receiving a scrambled composite video signal to be descrambled and converting the composite video singal into a digital signal for descrambling ; a multiplexing means for inputting the digital signal from said A/D converter and outputting the digital signal in a bit order in response to an external select signal ; a D/A converter for receiving the digital signal outputted from said multiplexing means and converting said outputted digital signal into an analog signal; a synchronous divider for receiving said composite video signal and dividing the composite video signal into a vertical synchronous signal and a horizontal synchronous signal ; a clock generator for receiving the horizontal synchronous signal from said synchronous divider to generate a clock signal and supplying the clock signal to said A/D converter and said D/A converter; an initial data generating means for receiving said composite video signal, extracting from said composite video signal initial data coded during a vertical blanking interval thereof every field thereof, and decoding the extracted coded initial data; a horizontal blanking interval detector for receiving the horizontal synchronous signal from said synchronous divider, detecting a horizontal blanking interval from said horizontal synchronous signal, and outputting a low signal during the detected horizontal blanking interval; a random number generator for generating random numbers of a predetermined bit number, upon receiving the vertical synchronous signal from said synchronous divider and the decoded initial data from said initial data generating means; a 2′S complement converter for complementing each bit signal from said random number generator ; and an AND logic operating means including a plurality of AND gates each having one input terminal for receiving a different complement bit signal from said 2′S complement converter, its other input terminal for receiving an output signal from said horizontal blanking interval detector, its output terminal coupled in common to said multiplexing means for applying said external select signal.

In accordance with still another aspect of the present invention, there is provided a method of scrambling/descrambling a video signal comprising the steps of; converting a composite video signal into digital signals of a predetermined bit number and multiplying the digital signals by a transform matrix of a predetermined format to bit-scramble them; converting said bit-scrambled digital signals to an analog signal and transmitting the analog-converted signal to a user station; re-converting said analog-converted signal into digital signals of said predetermined bit number and multiplying the digital signals by alternative transform matrix of the reverse of said predetermined format to descramble them; and converting said descrambled digital signals to an original composite video signal.

The above and other objects, features and advantages of the present invention will be more clearly un-

derstood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a construction of a conventional descrambler;

Fig. 2A is a waveform diagram of a composite video signal scrambled by a conventional scrambler ;

Fig. 2B is a waveform diagram of the composite video signal descrambled by the conventional descrambler;

Fig. 3 is a block diagram showing a construction of an embodiment of a scrambler according to the present invention ;

Fig. 4 is a block diagram showing a construction of an embodiment of a descrambler according to the present invention;

Fig. 5 is a block digaram showing a construction of alternative embodiment of the scrambler and the descrambler according to the present invention .

Referring now to Fig. 3, a scrambler in accordance with an embodiment of the present invention is shown to comprise an A/D converter 1 which receives a composite video signal Vin from an external equipment and converts the composite video signal into 8 bit digital signals A0-A7. Also, the scrambler comprises a synchronous divider 4, a clock generator 5, a multiplexing means 100, a D/A converter 6, a horizontal blanking interval detector 13, an initial data generating means 200, a 3 bit random number generator 12 and an AND logic operating means 300.

The synchronous divider 4 receives the composite video signal Vin from the external equipment and divides the composite video signal into a vertical synchronous signal V_{sync} and a horizontal synchronous signal H_{sync} which each is to be sent out to the 3 bit random number generator 12, and the clock generator 5 and the horizontal blanking interval detector 13.

The clock generator 5 receives the horizontal synchronous signal H_{sync} from the synchronous divider 4 to generate a clock signal and supplies the clock signal to the A/D converter 1 and D/A converter 6.

The multiplexing means 100 comprises 8 8× 1 multiplexers 21 through 28 which input simultaneously the 8 bit digital signals A0-A7 from the A/D converter 1. Each of the 8× 1 multiplexers 21 through 28 outputs an 1-bit digital signal Y0-Y7 of the 8 bit digital signals A0-A7 to the D/A converter 6 in response to a 3 bit external select signal SEL from the AND logic operating means 300.

The D/A converter 6 receives the 1 bit digital signal from each of the 8× 1 multiplexers 21 through 28, the total 8 bit digital signals and converts the 8 bit digital signals into a scrambled analog signal.

The horizontal blanking interval detector 13 detects a horizontal blanking interval from the horizontal synchronous signal from the synchronous divider 4, so that it outputs a "low" signal during the detected horizontal blanking interval while a "high" signal during the remaining interval.

The initial data generating means 200 receives the composite video signal Vin from the external equipment, extracts from the composite video signal Vin initial data coded during a vertical blanking interval thereof every each field thereof and decodes the extracted coded initial data. Then, the decoded initial data from the initial data generating means 200 is sent out to the 3 bit random number generator 12.

Upon receiving the vertical synchronous signal, V_{sync} from the synchronous divider 4 and the decoded initial data from the initial data generating means 200, the 3 bit random number generator 12 generates 3 bit random numbers.

The AND logic operating means 300 comprises 3 AND gates 14 through 16 which each has its one input terminal receiving 3 bit signals S1-S3 from the 3 bit random number generator 12 and its other input terminal receiving an output signal from the horizontal blanking interval detector 13. An output terminal of each of the AND gates 14 through 16 is coupled in common to the 8× 1 multiplexers 21 through 28 to apply the external select signal SEL.

Also, the initial data generating means 200 comprises a data slicer 7 for extracting from the composite video signal Vin the initial data coded during the vertical blanking interval thereof every each field thereof, a data RAM 8 for storing the coded initial data from the data slicer 7, and a microprocessor 9 for decoding the coded initial data stored in the data RAM 8 and sending the decoded initial data out to the 3 bit random number generator 12.

Fig. 4 is a block diagram showing partially a construction of an embodiment of a descrambler according to the present invention. This drawing is identical to the Fig. 3, except that there is shown a 2′S complement converter 17 connected between the output stage of the 3 bit random number generator 12 and the one input stage of AND gates 14 through 16 in the AND logic operating means 300. For this reason, 3 bit complement signals S1′- S3′ on the 3 bit signals S1-S3 from the 3 bit random number generator 12 are received at the one input stage of AND gates 14 through 16, differently from the scrambler of the present invention.

As described above, the construction of the descrambler in Fig.4 is identical to that of the scrambler in Fig. 3, but that it comprises the 2′S complement converter 17 connected between the output stage of the 3 bit random number generator 12 and the one input stage of AND gates 14 through 16 in the AND logic operating

means 300. The 2'S complement converter 17 performs complementing on the 3 bit signals S1-S3 from the 3 bit random number generator. Therefore, from the 2'S complement converter 17, the 3 bit complement signals S1'- S3' 12 on the 3 bit signals S1-S3 are sent out to the one input stage of AND gates 14 through 16, thereby allowing the external select signal SEL of the 2'S complement from the AND gates 14 through 16 in the AND logic operating means 300 to be applied to the multiplexing means 100.

Therefore, only the operation of the scrambler will be hereinafter described in detail.

First, when the original composite video signal Vin is converted into the 8 bit digital signals by the A/D converter 1, then the 8 bit digital signals from the A/D converter 1 are inputted by the 8 8× 1 multiplexers 21 through 28 simultaneously. Then, each of the 8× 1 multiplexers 21 through 28 outputs the 1 bit digital signal of the 8 bit digital signals to the D/A converter 6 in response to the 3 bit exteranl select signal SEL from the AND logic operating means 300. Finally, D/A converter 6 receives the 1 bit digital signal from each of the 8× 1 multiplexers 21 through 28, the total 8 bit digital signals and converts the 8 bit digital signals into the scrambled analog signal. As a result, the scrambled analog signal can be outputted from the D/A converter 6.

On the other hand, the synchronous divider 4 receives the composite video signal Vin from the external equipment, together with the A/D converter 1, and divides the composite video signal into vertical synchronous signal V_{sync} and horizontal synchronous signal H which then is sent out to the clock generator 5 and the horizontal blanking interval detector 13.

Upon receiving the horizontal synchronous signal H_{sync} from the synchronous divider 4, the clock generator 5 generates a clock signal and applies it to the A/D converter 1 and the D/A converter 6. The horizontal blanking interval detector 13 detects the horizontal blanking interval from the horizontal synchronous signal and applies a low signal to the other input terminals of respective AND gates 14 to 16 in the AND logic operating means 300 during the horizontal blanking interval. This is for the purpose of maintaining all outputs of the AND logic operating means 300 at low level state during the horizontal blanking interval, because this interval contains the horizontal synchronous signal, a color burst signal, a front porch and a back porch and needs no scrambling.

Also, the data slicer 7 in the initial data generating means 200 receives the composite video signal Vin which also is applied to the A/D converter 1 and the synchronous divider 4 and extracts from the composite video signal Vin the initial data coded during the vertical blanking interval thereof every each field thereof in order to store it into the data RAM 8. The microprocessor 9 decodes the coded initial data stored in the data RAM 8 and send the decoded initial data out to the 3 bit random number generator 12. The 3 bit random number generator 12 outputs 3 bit random numbers in response to the inputted initial data and the inputted vertical synchronous signal V_{sync} from the synchronous divider 4. Then, AND gates 14 to 16 in the AND logic operating means 300 receive 3 bit signals S1 to S3 as respective one input signals, respectively, and also receive an output signal from the horizontal blanking interval detector 13 as a common other input signal. The AND gates S1 to S3 AND logic operate the inputted signals and output 3 bit signals to the multiplexing means 100 as an external select signal, respectively.

Now, the operation by the construction of the scrambler as shown in Fig. 3 will be described with reference to the accompanying matrix formats.

The following table 1 shows a transform matrix format when a composite video signal is converted into 8 bit digital signals.

Table 1

$$Tjk = \begin{bmatrix} t11 & t12 & t13 & t14 & t15 & t16 & t17 & t18 \\ t21 & t22 & t23 & t24 & t25 & t26 & t27 & t28 \\ t31 & t32 & t33 & t34 & t35 & t36 & t37 & t38 \\ t41 & t42 & t43 & t44 & t45 & t46 & t47 & t48 \\ t51 & t52 & t53 & t54 & t55 & t56 & t57 & t57 \\ t61 & t62 & t63 & t64 & t65 & t66 & t67 & t68 \\ t71 & t72 & t73 & t74 & t75 & t76 & t77 & t78 \\ t81 & t82 & t83 & t84 & t85 & t86 & t87 & t88 \end{bmatrix}$$

The procedure that the multiplexing means 100 is bit-scrambling digital signals from the A/D converter 1 in response to the external select signal SEL from the AND logic operating means 300 can be defined by the following transform matrix equation 1 :

$$T_n = \begin{cases} Tj\ Ra\ (j+n) = 1 \\ \\ Others = 0 \end{cases} \quad \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

where,

n is a random positive integer including zero,

a is a bit number of the A/D converted composite video signal,

j is a positive integer from 1 to a , and

Ra(j+n) is the remainder when j+n was divided by a (optionally, a when the remainder is zero).

Several examples obtained by applying the matrix equation 1 to the transform matrix format table 1 can be expressed as transform matrix format tables 2 through 4 as follows:

Table 2

$$\begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \end{bmatrix} = \begin{bmatrix} 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \end{bmatrix} \times \begin{bmatrix} A0 \\ A1 \\ A2 \\ A3 \\ A4 \\ A5 \\ A6 \\ A7 \end{bmatrix}$$

Table 3

$$\begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \end{bmatrix} = \begin{bmatrix} 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \end{bmatrix} \times \begin{bmatrix} A0 \\ A1 \\ A2 \\ A3 \\ A4 \\ A5 \\ A6 \\ A7 \end{bmatrix}$$

Table 4

$$\begin{bmatrix} A0 \\ A1 \\ A2 \\ A3 \\ A4 \\ A5 \\ A6 \\ A7 \end{bmatrix} = \begin{bmatrix} 0&0&0&0&0&1&0&0 \\ 0&0&0&0&0&0&1&0 \\ 0&0&0&0&0&0&0&1 \\ 1&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0 \\ 0&0&0&0&1&0&0&0 \end{bmatrix} \times \begin{bmatrix} Y0 \\ Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \end{bmatrix}$$

The table 2 shows a transform matrix format of

$$Y = T_0 \, A$$

where all the bit signals outputted from the 3 bit random number generator 12 are zero (S1=S2=S3=0, that is n=0), the matrix format of the composite video signal digitalized by the A/D converter is indicated as A , the matrix format of the bit-scrambled signals outputted from the multiplexing means 100 is indicated as Y , and the value of a is 8.

The table 3 shows a transform matrix format of

$$Y = T_3 \, A$$

where the random positive integer "n" in the matrix equation 1 is 3.

The table 4 shows a transform matrix format of the descrambled state where the random positive integer in the matrix equation(1) is 3. The external select signal SEL can be obtained by the signals outputted from the 3 bit random number generator 12 and then complemented by the 2'S complement converter 17 as shown in Fig. 4, thus the matrix format of the digitalized composite video signal can be expressed as

$$A = T_n^t \, Y = T_{8-3} \, A$$

The table 4 can be obtained by substituting the above equations

$$A = T_n^t \, Y = T_{8-3} \, A$$

for the matrix equation (1).

In case of n=3,the first term of the scrambled matrix format table 3 can be expressed as :

$$Y0 = 0 \cdot A0 + 0 \cdot A1 + 0 \cdot A2 + 1 \cdot A3 + \ldots\ldots\ldots + 0 \cdot A7 = A3$$

Also, in case of n=3, the fourth term of the descrambled matrix format table 4 can be expressed as:

$$A3 = 1 \cdot Y0 + 0 \cdot Y1 + 0 \cdot Y2 + 0 \cdot Y3 + \ldots\ldots\ldots + 0 \cdot Y7 = Y0$$

Therefore, it is well known that certain signal descrambled by a transform matrix format such as equation (1) can be descrambled by alternative transform matrix of the reverse format of said matrix resulting in its return to its original composite video signal.

On the other hand, the scrambler as a transmitter generally transmits the scrambled composite video signal carried with initial data coded during the vertical blanking interval thereof every each field thereof for preventing the non-subscriber from descrambling the video signal.

In the scrambler, the coded initial data is extracted by the data slicer 7 in the initial data generating means 200, stored in the data RAM 8, then decoded by the microprocessor 9.

Thereafter, the decoded initial data is sent out to the 3 bit random number generator 12 every frame as a signal for controlling the 3 bit random number generator 12.

Accordingly, non-subscriber who is not notified of information about the coded initial data can not descramble the scrambled video signal because he does not recognize the contents of the 3 bit signals S1-S3 from the 3 bit random number generator 12.

Also, it is possible to take a case of n=0,1,7 in the transform matrix equation(1) into consideration in order to simplify the construction of the 8 multiplexers 21 through 28 in the multiplexing means 100. In other words, the scrambler and the descrambler can have such constructions as shown in Fig. 5, in consideration of cases of

$$\pi_0,\ \pi_1,\ \pi_7.$$

In case of π_0, in the scrambler, the 8 8× 1 multiplexers 21 through 28 in Fig. 3 can be replaced by a buffer 32 in Fig. 5A, also in case of π_1, the multiplexers 21 through 28 can be replaced by a first shift register 31 shifting digital signal to the right, 1 bit, and in case of π_7, the multiplexers 21 through 28 can be replaced by a second shift register 33 shifting digital signal to the left, 1 bit.

As above-mentioned, the scrambler and the descrambler in accordance with the present invention can provide advantages as follows:

First, they can cost down because there is no need to provide the two line memories which have been obliged to provide for the conventional apparatus;

Second, they can prevent the image quality from being degraded because the cutting at the random point of the horizontal scanning line for scrambling does not need.

Claims

1. An apparatus for scrambling a video signal comprising an A/D converter (1) for receiving a composite video signal (V_{in}) to be bit-scrambled from an external equipment and converting the composite video signal into a digital signal for bit-scrambling ;

a multiplexing means (100) for inputting the digital signal from said A/D converter (1) and outputting the digital signal in a bit order in response to an external select signal (SEL);

a D/A converter (6) for receiving the digital signal outputted from said multiplexing means (100) and converting said outputted digital signal into an analog signal (V_{out}) ;

a synchronous divider (4) for receiving said composite video signal (V_{in}) and dividing the composite video signal into a vertical synchronous signal (V_{sync}) and a horizontal synchronous signal (H_{sync}) ;

a clock generator (5) for receiving the horizontal synchronous signal (H_{sync}) from said synchronous divider (4) to generate a clock signal and supplying the clock signal to said A/D converter (1) and said D/A converter (6) ;

an initial data generating means (200) for receiving said composite video signal (V_{in}), extracting from said composite video signal (V_{in}) initial data coded during a vertical blanking interval thereof every field thereof, and decoding the extracted coded initial data ;

a horizontal blanking interval detector (13) for receiving the horizontal synchronous signal (H_{sync}) from said synchronous divider (4), detecting a horizontal blanking interval from said horizontal synchronous signal, and outputting a low signal during the detected horizontal blanking interval ;

a random number generator (12) for generating random numbers of a predetermined bit number, upon receiving the vertical synchronous signal from said synchronous divider and the decoded initial data from said initial data generating means (200) ; and

an AND logic operating means (300) including a plurality of AND gates (14-16) each having one input terminal for receiving a different bit signal from said random number generator (12), its other input terminal for receiving an output signal from said horizontal blanking interval detector (13), its output terminal coupled in common to said multiplexing means (100) for applying said external select signal (SEL).

2. An apparatus for descrambling a video signal comprising ;

an A/D converter (1) for receiving a scrambled composite video signal (V_{in}) to be descrambled and converting the composite video signal into a digital signal for descrambling ;

a multiplexing means (100) for inputting the digital signal from said A/D converter (1) and outputting

the digital signal in a bit order in response to an external select signal (SEL) ;

a D/A converter (6) for receiving the digital signal outputted from said multiplexing means (100) and converting said outputted digital signal into an analog signal (V_{out}) ;

a synchronous divider (4) for receiving said composite video signal and dividing the composite video signal into a vertical synchronous signal (V_{sync}) and a horizontal synchronous signal (H_{sync}) ;

a clock generator (5) for receiving the horizontal synchronous signal (H_{sync}) from said synchronous divider (4) to generate a clock signal and supplying the clock signal to said A/D converter (1) and said D/A converter (6) ;

an initial data generating means (200) for receiving said composite video signal (V_{in}), extracting from said composite video signal initial data coded during a vertical blanking interval thereof every field thereof, and decoding the extracted coded initial data ;

a horizontal blanking interval detector (13) for receiving the horizontal synchronous signal (H_{sync}) from said synchronous divider (4), detecting a horizontal blanking interval from said horizontal synchronous signal (H_{sync}), and outputting a low signal during the detected horizontal blanking interval ;

a random number generator (12) for generating random numbers of a predetermined bit number, upon receiving the vertical synchronous signal (V_{sync}) from said synchronous divider (4) and the decoded initial data from said initial data generating means (200) ;

a 2′S complement converter (17) for complementing each bit signal from said random number generator (12) ; and

an AND logic operating means (300) including a plurality of AND gates (14-16) each having one input terminal for receiving a different complement bit signal from said 2′S complement converter (17), its other input terminal for receiving an output signal from said horizontal blanking interval detector (13), its output terminal coupled in common to said multiplexing means (100) for applying said external select signal (SEL).

3. An apparatus for scrambling a video signal as claimed in claim 1, wherein said initial data generating means (200) includes a data slicer (7) for extracting from said composite video signal (V_{in}) said initial data coded during the vertical blanking interval thereof every field thereof, a data RAM (8) for storing said coded initial data from said data slicer (7), and a microprocessor (9) for decoding said coded initial data stored in said data RAM (8) and sending the decoded initial data out to said random number generator (12) to control it.

4. An apparatus for scrambling a video signal as claimed in claim 1, wherein said multiplexing means (100) includes a first shift register (31) for shifting the digital signal from said A/D converter (1) to the right, a buffer (32) for buffering the digital signal from said A/D converter (1), a second shift register (33) for shifting the digital signal signal from said A/D converter (1) to the left, and a switch responsive to said external select signal for selecting one of output from said first and second shift registers (31, 33) and said buffer (32).

5. An apparatus for descrambling a video signal as claimed in claim 2, wherein said initial data generating means (200) includes a data slicer (7) for extracting from said composite video signal (V_{in}) said initial data coded during the vertical blanking interval thereof every field thereof, a data RAM (8) for storing said coded initial data from said data slicer (7), and a microprocessor (9) for decoding said coded initial data stored in said data RAM (8) and sending the decoded initial data out to said random number generator (12) to control it.

6. An apparatus for descrambling a video signal as claimed in claim 2, wherein said multiplexing means (100) includes a first shift register (33) for shifting the digital signal from said A/D converter (1) to the left, a buffer (32) for buffering the digital signal from said A/D converter (1), a second shift register (31) for shifting the digital signal from said A/D converter (1) to the right, and a switch responsive to said external select signal for selecting one of output signals from said first and second shift registers (33, 31) and said buffer (32).

7. A method of scrambling/descrambling a video signal comprising the steps of :

converting a composite video signal into digital signals of a predetermined bit number and multiplying the digital signals by a transform matrix of a predetermined format to bit-scramble them ;

converting said bit-scrambled digital signals to an analog signal and transmitting the analog-converted signal to a user station ;

re-converting said analog-converted signal into digital signals of said predetermined bit number and multiplying the digital signals by alternative transform matrix of the reverse of said predetermined format to descramble them ; and

converting said descrambled digital signals to an original composite video signal.

8. A method for scrambling/descrambling a video signal as claimed in claim 7, wherein said transform matrix is defined by Tn expressed by the equations :

$$T_n = 1 \text{ (in case of } T_n = Tj, Ra(j+n), 0 \text{ (in case of the others)}$$

$$Y = T_n / A ,$$

$$/A = T^{a-n} Y$$

where :

Y =	the matrix of the bit-scrambled composite video signal
/A =	the matrix of the digitalized composite video signal
j =	positive integer from 1 to a, a = bit number of the digitalized composite video signal
n =	random positive integer including zero
x =	j + n
Tj, Ra(j+n) =	the remainder when x are divided by a (but, when the remainder is zero, Tj,Ra(j+n)is regarded as a).

Patentansprüche

1. Vorrichtung zur Verschlüsselung eines Videosignals umfassend einen A/D-Wandler (1) zum Empfang eines von einem externen Gerät kommenden zusammengesetzten Videosignals (V_{in}), das Bit-verschlüsselt werden soll, und zur Umwandlung des zusammengesetzten Videosignals in ein digitales Signal für die Bit-Verschlüsselung;

ein Multiplexmittel (100) zur Eingabe des digitalen Signals des A/D-Wandlers (1) und zur Ausgabe des digitalen Signals in einer Bit-Reihenfolge als Reaktion auf ein externes Auswahlsignal (SEL);

einen D/A-Wandler (6) zum Empfang des digitalen Signals, das von dem Multiplexmittel (100) ausgegeben wird, und zur Umwandlung des ausgegebenen digitalen Signals in ein analoges Signal (V_{out});

einen Synchronteiler (4) zum Empfang des zusammengesetzten Videosignals (V_{in}) und zum Teilen des Videosignals in ein Vertikal-Synchronsignal (V_{sync}) und ein Horizontal-Synchronsignal (H_{sync});

einen Taktgenerator (5) zum Empfang des Horizontal-Synchronsignals (H_{sync}) des Synchronteilers (4), um ein Taktsignal zu erzeugen, und das Taktsignal dem A/D-Wandler (1) und dem D/A-Wandler (6) zuzuführen;

ein Anfangsdaten-erzeugendes Mittel (200) zum Empfang des zusammengesetzten Videosignals (V_{in}), zum Extrahieren aus dem zusammengesetzten Videosignal (V_{in}) der codierten Anfangsdaten während eines Vertikal-Austastintervalls des zusammengesetzten Videosignals mit jedem seiner Felder, und zum Decodieren der extrahierten codierten Anfangsdaten;

einen Horizontal-Austastintervall-Detektor (13) zum Empfang des Horizontal-Synchronsignals (H_{sync}) des Synchronteilers (4), zur Detektierung eines Horizontal-Austastintervalls aus dem Horizontal-Synchronsignal, und zur Ausgabe eines Niedrig-Pegel-Signals während des detektierten Horizontal-Austastintervalls;

einen Zufallszahlgenerator (12) zur Erzeugung von Zufallszahlen einer vorherbestimmten Bit-Zahl nach Empfang des Vertikal-Synchronsignals des Synchronteilers und der decodierten Anfangsdaten des Anfangsdaten-erzeugenden Mittels (200); und

ein UND-Verknüpfungs-logisches-Mittel (300) umfassend eine Vielzahl von UND-Gattern (14 - 16), wobei jedes eine Eingabeklemme zum Empfang eines unterschiedlichen Bit-Signals des Zufallszahlgenerators (12) aufweist, und eine andere Eingabeklemme zum Empfang eines Ausgabesignals des Horizontal-Austastintervall-Detektors (13), wobei deren Ausgabeklemmen zum Multiplexmittel (100) für die Zuführung des externen Auswahlsignals (SEL) zusammengeschaltet sind.

2. Vorrichtung zur Entschlüsselung eines Videosignals umfassend:

einen A/D-Wandler (1) zum Empfang eines verschlüsselten zusammengesetzten Videosignals

(V_{in}), das entschlüsselt werden soll, und zur Umwandlung des zusammengesetzten Videosignals in ein digitales Signal zur Entschlüsselungs;

ein Multiplexmittel (100) zur Eingabe des digitalen Signals des A/D-Wandlers (1) und zur Ausgabe des digitalen Signals in einer Bit-Reihenfolge als Reaktion auf ein externes Auswahlsignal (SEL);

einen D/A-Wandler (6) zum Empfang des digitalen Signals, das vom Multiplexmittel (100) ausgegeben wird und zur Umwandlung des ausgegebenen digitalen Signals in ein analoges Signal (V_{out});

einen Synchronteiler (4) zum Empfang des zusammengesetzten Videosignals und zum Teilen des zusammengesetzten Videosignals in ein Vertikal-Synchronsignal (V_{sync}) und ein Horizontal-Synchronsignal (H_{sync});

einen Taktgenerator (5) zum Empfang des Horizontal-Synchronsignals (H_{sync}) des Synchronteilers (4), um ein Taktsignal zu erzeugen, und das Taktsignal dem A/D-Wandler (1) und dem D/A-Wandler (6) zuzuführen;

ein Anfangsdaten-erzeugendes Mittel (200) zum Empfang des zusammengesetzten Videosignals (V_{in}), zum Extrahieren aus dem zusammengesetzten Videosignal der codierten Anfangsdaten während eines Vertikal-Austastintervalls des zusammengesetzten Videosignals mit jedem seiner Felder, und zum Dekodieren der extrahierten codierten Anfangsdaten;

einen Horizontal-Austastintervall-Detektor (13) zum Empfang des Horizontal-Synchronsignals (H_{sync}) des Synchronteilers (4), zur Detektierung eines Horizontal-Austastintervalls aus dem Horizontal-Synchronsignal (H_{sync}) und zur Ausgabe eines Niedrig-Pegel-Signals während des detektierten Horizontal-Austastintervalls;

einen Zufallszahlgenerator (12) zur Erzeugung von Zufallszahlen einer vorherbestimmten Bit-Zahl, nach Empfang des Vertikal-Synchronsignals (V_{sync}) des Synchronteilers (4) und der decodierten Anfangsdaten des Anfangsdaten-erzeugenden Mittels (200);

einen Zweier-Komplement-Wandler (17) zur Komplementierung jedes Bit-Signals des Zufallszahlgenerators (12); und

ein UND-Verknüpfungs-logisches-Mittel (300) umfassend eine Vielzahl von UND-Gattern (14 - 16), wobei jedes eine Eingabeklemme zum Empfang eines unterschiedlichen Komplement-Bit-Signals des Zweier-Komplement-Wandlers (17) aufweist, und eine andere Eingabeklemme zum Empfang eines Ausgabesignals des Horizontal-Austastintervall-Detektors (13), wobei deren Ausgangsklemmen zum Multiplexmittel (100) für die Zuführung des externen Auswahlsignals (SEL) zusammengeschaltet sind.

3. Vorrichtung zur Verschlüsselung eines Videosignals gemäß Anspruch 1, wobei das Anfangsdaten-erzeugende Mittel (200) ein Datengewinnungsgerät (7) zum Extrahieren aus dem zusammengesetzten Videosignal (V_{in}) der codierten Anfangsdaten während eines Vertikal-Austastintervalls des zusammengesetzten Videosignals mit jedem seiner Felder umfaßt, einen Datenspeicher mit direktem Zugriff (8) zur Speicherung der codierten Anfangsdaten des Datengewinnungs-gerätes (7), und einen Mikroprozessor (9) zur Decodierung der codierten Anfangsdaten, die im Datenspeicher mit direktem Zugriff (8) gespeichert sind, und zur Übertragung der decodierten Anfangsdaten zum Zufallszahlgenerator (12), um diesen anzusteuern.

4. Vorrichtung zur Verschlüsselung eines Videosignals gemäß Anspruch 1, wobei das Multiplexmittel (100) ein erstes Schieberegister (31) zur Rechtsverschiebung des digitalen Signals des A/D-Wandlers (1) umfaßt, einen Puffer (32) zur Pufferung eines digitalen Signals des A/D-Wandlers (1), ein zweites Schieberegister (33) zur Linksverschiebung des digitalen Signals des A/D-Wandlers (1), und einen Schalter, der auf das externe Auswahlsignal reagiert, um eine der Ausgaben vom ersten und zweiten Schieberegister (31, 33) und des Puffers (32) auszuwählen.

5. Vorrichtung zur Entschlüsselung eines Videosignals gemäß Anspruch 2, wobei das Anfangsdaten-erzeugende Mittel (200) ein Datengewinnungsgerät (7) zum Extrahieren aus dem zusammengesetzten Videosignal (V_{in}) der codierten Anfangsdaten während eines Vertikal-Austastintervalls des zusammengesetzten Videosignals mit jedem seiner Felder, einen Datenspeicher mit direktem Zugriff (8) zur Speicherung der codierten Anfangsdaten des Datengewinnungsgerätes (7) und einen Mikroprozessor (9) zur Decodierung der codierten Anfangsdaten umfaßt, die im Datenspeicher mit direktem Zugriff (8) gespeichert sind, und zur Übertragung der decodierten Anfangsdaten zum Zufallszahlgenerator (12), um diesen anzusteuern.

6. Vorrichtung zur Entschlüsselung eines Videosignals gemäß Anspruch 2, wobei das Multiplexmittel (100) ein erstes Schieberegister (33) zur Linksverschiebung des digitalen Signals des A/D-Wandlers (1) umfaßt,

einen Puffer (32) zur Pufferung des digitalen Signals des A/D-Wandlers (1), ein zweites Schieberegister (31) zur Rechtsverschiebung des digitalen Signals des A/D-Wandlers (1), und einen Schalter, der auf das externe Auswahlsignal reagiert, um eines der Ausgabesignale des ersten und zweiten Schieberegisters (33, 31) und des Puffers (32) auszuwählen.

7. Verfahren zur Ver-/Entschlüsselung eines Videosignals folgende Schritte umfassend:

Umwandlung eines zusammengesetzten Videosignals in ein digitales Signal einer vorherbestimmen Bit-Zahl und Multiplizierung des digitalen Signals mit einer Umwandlungsmatrix eines vorherbestimmten Formats zu deren Bit-Verschlüsselung;

Umwandlung des Bit-verschlüsselten digitalen Signals in ein analoges Signal und Übertragung des analog-gewandelten Signals an eine Benutzereinheit;

Rückumwandlung des analog-gewandelten Signals in ein digitales Signal der vorherbestimmten Bit-Zahl und Multiplizierung der digitalen Signale mit einer alternativen Umwandlungsmatrix des Umkehrtyps des vorherbestimmten Formats, um diese zu entschlüsseln; und

Umwandlung der entschlüsselten digitalen Signale in ein ursprüngliches zusammengesetztes Videosignal.

8. Verfahren zur Ver-/Entschlüsselung eines Videosignals gemäß Anspruch 7, wobei die Umwandlungsmatrix durch Tn definiert ist, ausgedrückt durch die Gleichungen:

$$T_n = 1 \text{ (falls } T_n = Tj, Ra(j + n), 0 \text{ (in den anderen Fällen)}$$

$$Y = T_n / A ,$$

$$/A = T a\text{-}n\, Y$$

wobei:

T =	die Matrix des Bit-verschlüsselten zusammen-gesetzten Videosignals
$/A$ =	die Matrix des digitalisierten zusammengesetzten Videosignals
j =	positive ganze Zahl von 1 bis a,
a =	Bit-Zahl des digitalisierten zusammengesetzten Videosignals
n =	ganze positive Zufallszahl einschließlich 0
x =	j + n
Tj, Ra(j+n) =	der Rest, bei x geteilt durch a (wenn jedoch der Rest 0 beträgt, wird Tj, Ra(j+n) als a betrachtet).

Revendications

1. Appareil de brouillage d'un signal vidéo, comprenant un convertisseur Analogique/Numérique (1) pour recevoir un signal vidéo composite (V_{in}) à brouiller en bits, provenant d'un équipement extérieur, et pour convertir le signal vidéo composite en un signal numérique pour le brouillage de bits ;

des moyens de multiplexage (100) pour introduire le signal numérique provenant du convertisseur Analogique/Numérique (1) et pour fournir en sortie le signal numérique dans un ordre de bits en réponse à un signal de sélection extérieur (SEL) ;

un convertisseur Numérique/Analogique (6) pour recevoir le signal numérique de sortie des moyens de multiplexage (100) et pour convertir ce signal numérique de sortie en un signal analogique (V_{out}) ;

un diviseur synchrone (4) pour recevoir le signal vidéo composite (V_{in}) et pour diviser ce signal vidéo composite en un signal synchrone vertical (V_{sync}) et un signal synchrone horizontal (H_{sync}) ;

un générateur d'horloge (5) pour recevoir le signal synchrone horizontal (H_{sync}) provenant du diviseur synchrone (4) afin de générer un signal d'horloge et de fournir ce signal d'horloge au convertisseur Analogique/Numérique (1) et au convertisseur Numérique/Analogique (6) ;

des moyens de génération de données initiales (200) pour recevoir le signal vidéo composite (Vin), pour extraire de ce signal vidéo composite (V_{in}) des données initiales codées pendant un intervalle d'effacement vertical de celui-ci dans chaque champ de celui-ci, et pour décoder les données initiales codées extraites ;

un détecteur d'intervalle d'effacement horizontal (13) pour recevoir le signal synchrone horizontal

(H_{sync}) provenant du diviseur synchrone (4), pour détecter un intervalle d'effacement horizontal dans ce signal synchrone horizontal, et pour fournir en sortie un signal bas pendant l'intervalle d'effacement horizontal détecté ;

un générateur de nombres aléatoires (12) pour générer des nombres aléatoires d'un nombre de bits prédéterminé, à la réception du signal synchrone vertical provenant du diviseur synchrone, et les données initiales décodées provenant des moyens de génération de données initiales (200) ; et

des moyens de fonctionnement logique ET (300) comprenant une pluralité de portes ET (14-16) comportant chacune une borne d'entrée pour recevoir un signal de bits différent du générateur de nombres aléatoires (12), son autre borne d'entrée étant destinée à recevoir un signal de sortie du détecteur d'intervalle d'effacement horizontal (13), et sa borne de sortie étant couplée en commun aux moyens de multiplexage (100) pour appliquer le signal de sélection extérieur (SEL).

2. Appareil de désembrouillage d'un signal vidéo, comprenant :

un convertisseur Analogique/Numérique (1) pour recevoir un signal vidéo composite brouillé (V_{in}) à désembrouiller, et pour convertir ce signal vidéo composite en un signal numérique pour désembrouillage ;

des moyens de multiplexage (100) pour introduire le signal numérique provenant du convertisseur Analogique/Numérique (1) et pour fournir en sortie le signal numérique dans un ordre de bits en réponse à un signal de sélection extérieur (SEL) ;

un convertisseur Numérique/Analogique (6) pour recevoir le signal numérique fourni en sortie par les moyens de multiplexage (100), et pour convertir ce signal numérique de sortie en un signal analogique (V_{out}) ;

un diviseur synchrone (4) pour recevoir le signal vidéo composite et pour diviser ce signal vidéo composite en un signal synchrone vertical (V_{sync}) et un signal synchrone horizontal (H_{sync}) ;

un générateur d'horloge (5) pour recevoir le signal synchrone horizontal (H_{sync}) provenant du diviseur synchrone (4) afin de générer un signal d'horloge, et pour fournir ce signal d'horloge au convertisseur Analogique/Numérique (1) et au convertisseur Numérique/Analogique (6) ;

des moyens de génération de données initiales (200) pour recevoir le signal vidéo composite (V_{in}), pour extraire de ce signal vidéo composite les données initiales codées pendant un intervalle d'effacement vertical de celui-ci dans chaque champ de celui-ci, et pour décoder les données initiales codées extraites ;

un détecteur d'intervalle d'effacement horizontal (13) pour recevoir le signal synchrone horizontal (H_{sync}) du diviseur synchrone (4), pour détecter un intervalle d'effacement horizontal dans ce signal synchrone horizontal (H_{sync}), et pour fournir en sortie un signal bas pendant l'intervalle d'effacement horizontal détecté ;

un générateur de nombres aléatoires (12) pour générer des nombres aléatoires d'un nombre de bits prédéterminé à la réception du signal synchrone vertical (V_{sync}) provenant du diviseur synchrone (4), et des données initiales décodées provenant des moyens de génération de données initiales (200) ;

un convertisseur de complément 2'S (17) pour compléter chaque signal de bits provenant du générateur de nombres aléatoires (12) ; et

des moyens de fonctionnement logique ET (300) comprenant une pluralité de portes ET (14-16) comportant chacune une borne d'entrée pour recevoir un signal de bits de complément différent provenant du convertisseur de complément 2'S (17), son autre borne d'entrée étant destinée à recevoir un signal de sortie provenant du détecteur d'intervalle d'effacement horizontal (13), et sa borne de sortie étant couplée en commun aux moyens de multiplexage (100) pour appliquer le signal de sélection extérieur (SEL).

3. Appareil de brouillage d'un signal vidéo selon la revendication 1, caractérisé en ce que les moyens de génération de données initiales (200) comprennent un découpeur de données (7) pour extraire du signal vidéo composite (V_{in}) les données initiales codées pendant l'intervalle d'effacement vertical de celui-ci dans chaque champ de celui-ci, une mémoire vive de données (8) pour stocker les données initiales codées provenant du découpeur de données (7), et un microprocesseur (9) pour décoder ces données initiales codées stockées dans la mémoire vive de données (8) et pour émettre ces données initiales décodées vers le générateur de nombres aléatoires (12) afin de le commander.

4. Appareil de brouillage d'un signal vidéo selon la revendication 1, caractérisé en ce que les moyens de multiplexage (100) comprennent un premier registre à décalage (31) pour décaler vers la droite le signal numérique provenant du convertisseur Analogique/Numérique (1), une mémoire tampon (32) pour conser-

ver en mémoire le signal numérique provenant du convertisseur Analogique/Numérique (1), un second registre à décalage (33) pour décaler vers la gauche le signal numérique provenant du convertisseur Analogique/Numérique (1), et un commutateur répondant au signal de sélection extérieur pour sélectionner l'une des sorties du premier et second registre à décalage (31, 33) et de la mémoire tampon (32).

5. Appareil de désembrouillage d'un signal vidéo selon la revendication 2, caractérisé en ce que les moyens de génération de données initiales (200) comprennent un découpeur de données (7) pour extraire du signal vidéo composite (V_{in}) les données initiales codées pendant l'intervalle d'effacement vertical de celui-ci dans chaque champ de celui-ci, une mémoire vive de données (8) pour stocker les données initiales codées provenant du découpeur de données (7), et un microprocesseur (9) pour décoder les données initiales codées stockées dans la mémoire vive de données (8) et pour émettre les données initiales décodées vers le générateur de nombres aléatoires (12) afin de le commander.

6. Appareil de désembrouillage d'un signal vidéo selon la revendication 2, caractérisé en ce que les moyens de multiplexage (100) comprennent un premier registre à décalage (33) pour décaler vers la gauche le signal numérique provenant du convertisseur Analogique/Numérique (1), une mémoire tampon (32) pour conserver en mémoire le signal numérique provenant du convertisseur Analogique/Numérique (1), un second registre à décalage (31) pour décaler vers la droite le signal numérique provenant du convertisseur Analogique/Numérique (1), et un commutateur répondant au signal de sélection extérieur pour sélectionner l'un des signaux de sortie des premier et second registres à décalage (33, 31) et de la mémoire tampon (32).

7. Procédé de brouillage/désembrouillage d'un signal vidéo, comprenant les étapes consistant à :

convertir un signal vidéo composite en signaux numériques d'un nombre de bits prédéterminé et multiplier les signaux numériques par une matrice de transformation d'un format prédéterminé pour les embrouiller en bits ;

convertir en un signal analogique les signaux numériques embrouillés en bits et transmettre le signal de conversion analogique à un poste d'utilisateur ;

reconvertir le signal de conversion analogique en signaux numériques du nombre de bits prédéterminé et multiplier les signaux numériques par une autre matrice de transformation de format inverse du format prédéterminé, afin de les désembrouiller ; et

convertir en le signal vidéo composite initial les signaux numériques désembrouillés.

8. Procédé de brouillage/désembrouillage d'un signal vidéo selon la revendication 7, caractérisé en ce que la matrice de transformation est définie par Tn exprimant par les équations :

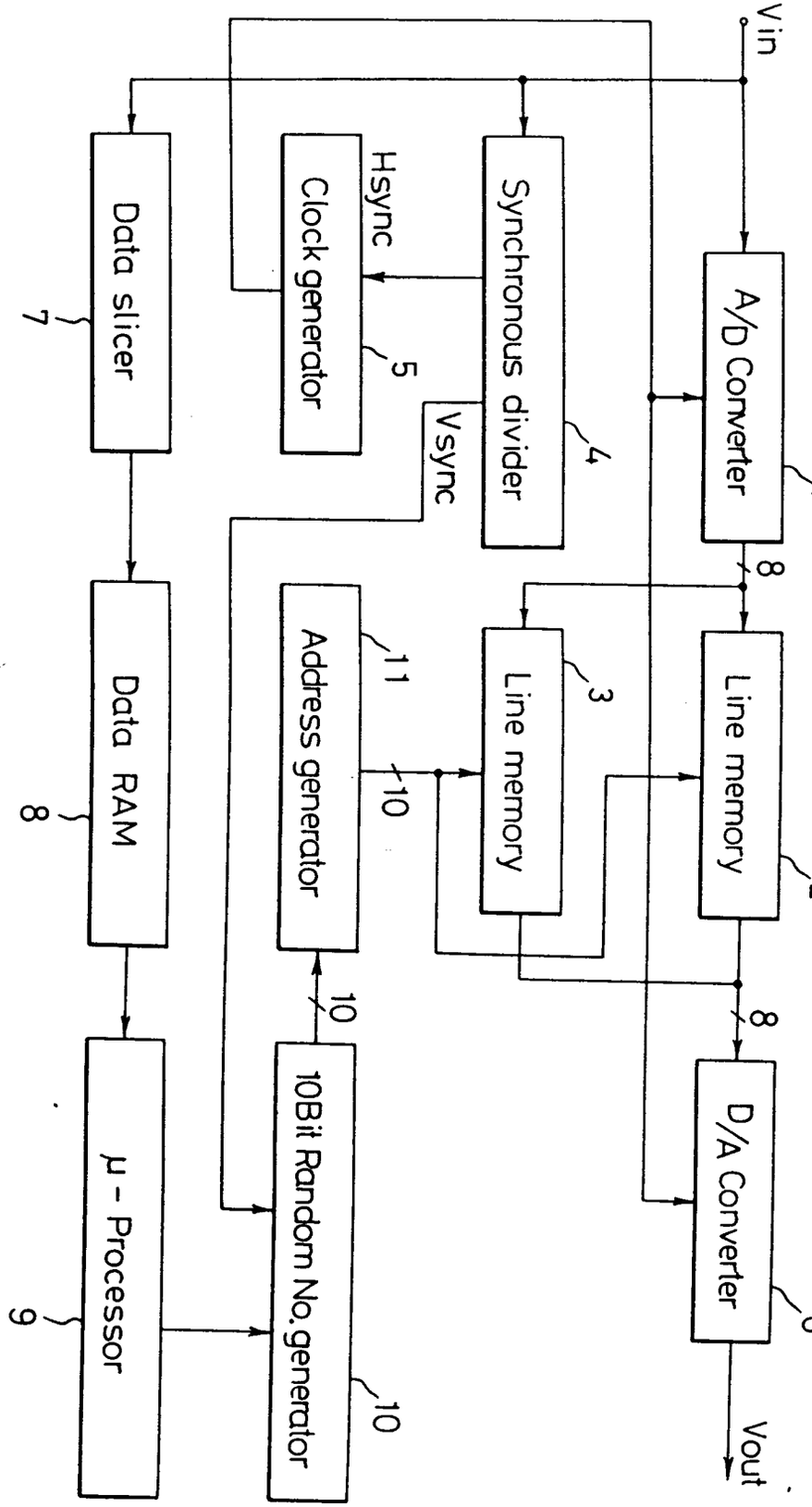
$$T_n = 1 \text{ (dans le cas de } T_n = Tj, Ra(j + n)) ; 0 \text{ (dans le cas des autres)}$$

$$Y = T_n A ,$$

$$A = T_{a-n} Y$$

où :

Y =	matrice du signal vidéo composite brouillé en bits
A =	matrice du signal vidéo composite numérisé
j =	nombre entier positif compris entre 1 et a, a = nombre de bits du signal vidéo composite numérisé
n =	nombre entier positif aléatoire comprenant zéro
x =	j + n
Tj, Ra (j + n) =	le reste, lorsque x est divisé par a (mais, lorsque le reste est zéro, Tj, Ra (j+n)) est considéré comme a.



F I G. 1
PRIOR ART

FIG. 2A
PRIOR ART

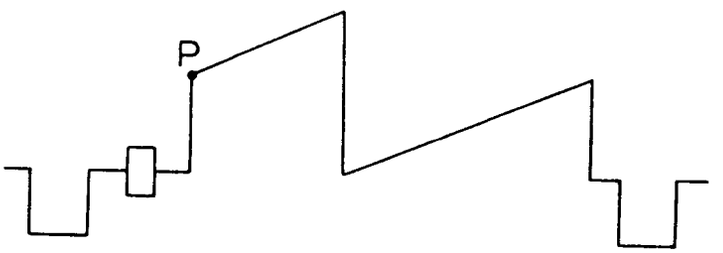
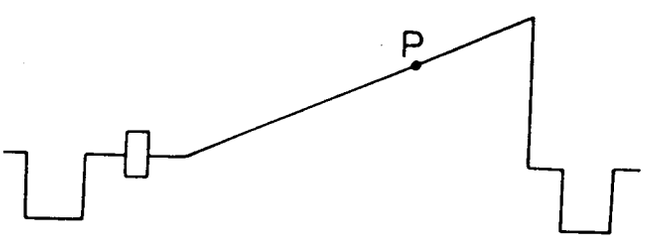
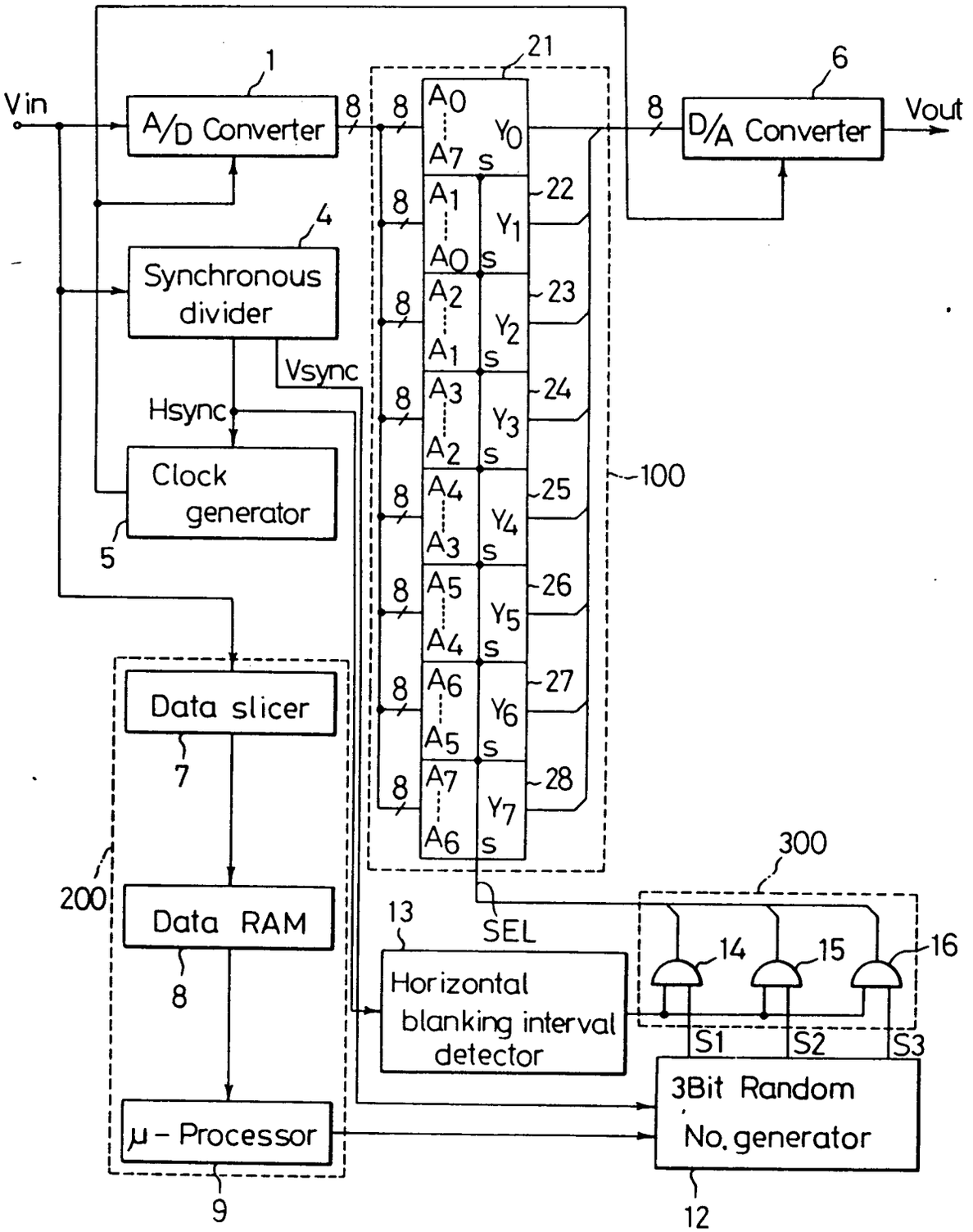


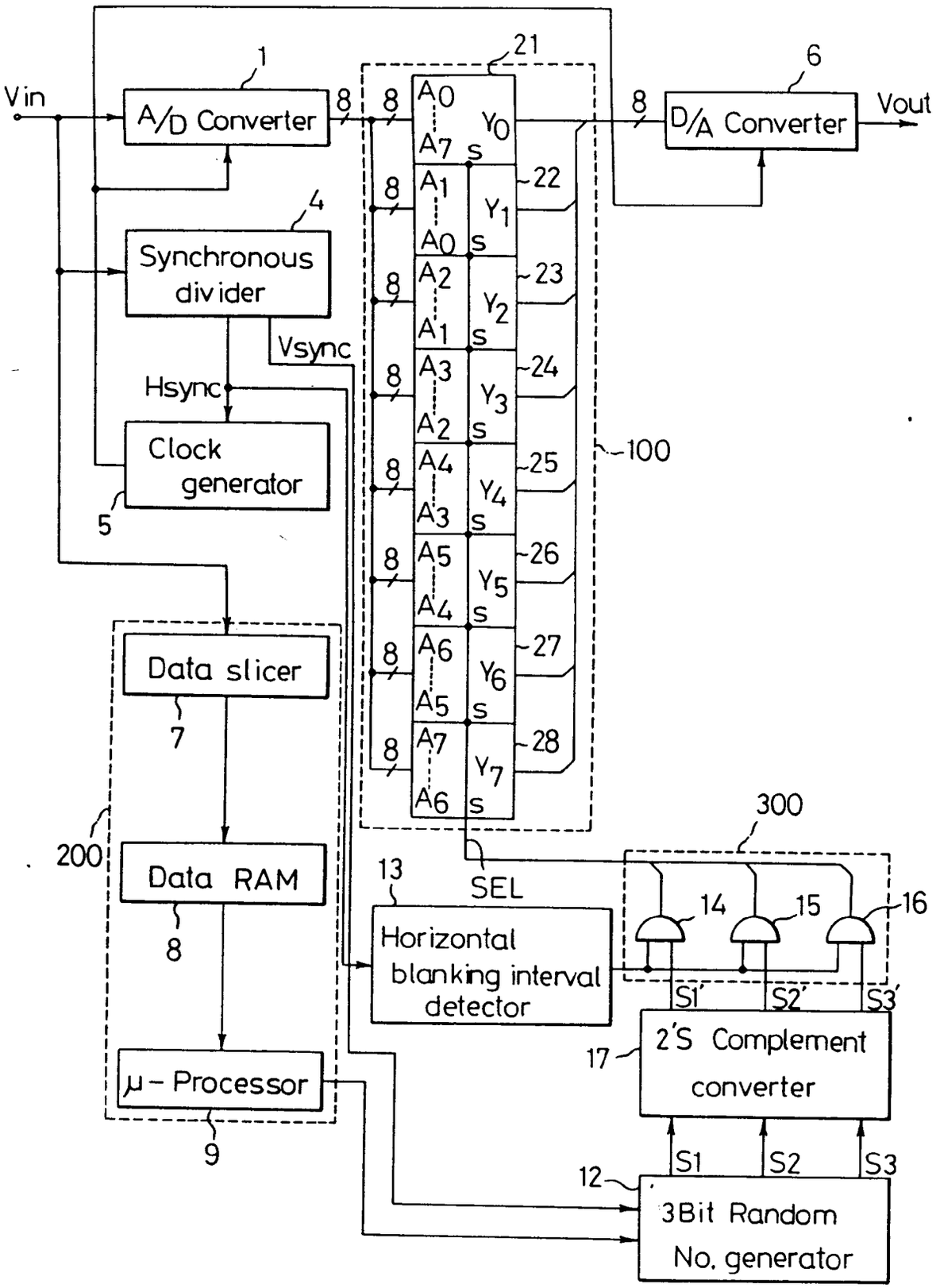
FIG. 2B
PRIOR ART



F I G. 3


Vin
A/D Converter
1
8
8
21
A0
A7
Y0
s
8
D/A Converter
6
Vout
8
A1
A0
Y1
22
4
Synchronous divider
8
A2
A1
Y2
23
Vsync
Hsync
8
A3
A2
Y3
24
Clock generator
5
8
A4
A3
Y4
25
100
8
A5
A4
Y5
26
Data slicer
7
8
A6
A5
Y6
27
8
A7
A6
Y7
28
300
200
Data RAM
8
13
SEL
14
15
16
Horizontal blanking interval detector
S1
S2
S3
3Bit Random No. generator
12
μ - Processor
9

F I G. 4


Vin
A/D Converter
1
8
21
6
D/A Converter
Vout
4
Synchronous divider
Vsync
Hsync
Clock generator
5
100
22
23
24
25
26
27
28
Data slicer
7
200
Data RAM
8
μ - Processor
9
13
SEL
Horizontal blanking interval detector
300
14
15
16
S1'
S2'
S3'
17
2'S Complement converter
S1
S2
S3
12
3Bit Random No. generator

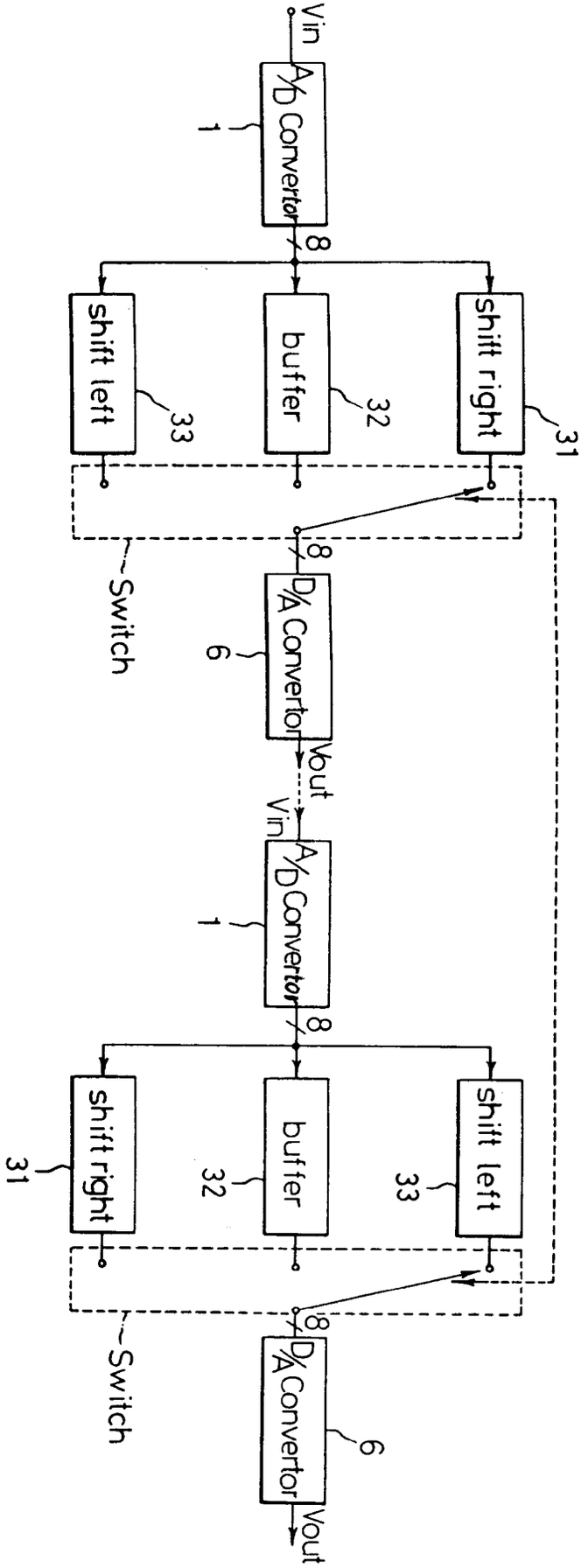

Vin
A/D Convertor
1
8
shift left
33
buffer
32
shift right
31
Switch
8
D/A Convertor
6
Vout
Vin
A/D Convertor
1
8
shift right
31
buffer
32
shift left
33
Switch
8
D/A Convertor
6
Vout

FIG. 5