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(54) Quasi-static level shifter.

(57) The level shifter (40) in accordance with the invention comprises an output stage including a first transistor (16) which is controlled directly by the input signal, and a further transistor (20) which is controlled, via a capacitance (24) by an input signal combined with a recurrent, spike-shaped signal. The level shifter (40) thus behaves as a static level shifter but has a lower current consumption and requires less surface area.

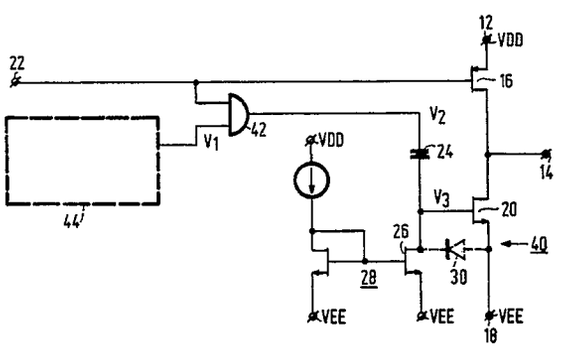

FIG.2

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The invention relates to a level shifter, comprising a charging path between a first supply voltage and an output, and a discharging path between the output and a second supply voltage, the paths being controllable in a mutually complementary fashion by an input signal on an input, one of the paths being DC coupled to the input while the other path is coupled thereto *via* a capacitance, and also comprising a driver circuit which includes such level shifters and a display provided with such a driver circuit.

A level shifter of this kind is known *per se*. The operation of the known level shifter is fully dynamic, *i.e.* its output signal is not available in static form. Driving of further circuits by means of this output signal requires either a time-critical behaviour of these circuits or special steps to safeguard control of these circuits because at least one of the levels of this output signal is not stable. Therefore, it is an object of the invention to provide a level shifter of the kind set forth which does not have said drawbacks.

This object is achieved by a level shifter in accordance with the invention which is characterized in that in order to regenerate a control voltage on a control input of the other path, the input signal is logically combined with a recurrent signal which can be applied to a control input *via* the capacitance. The signal transferred via the capacitance, on the gate electrode is then continuously regenerated by a recurrent signal. The logic combination with the input signal ensures that the level shifter behaves as a static level shifter on the output, *i.e.* both logic levels on the output are substantially constant.

In the context of the present Patent Application a recurrent signal is to be understood to mean not only a signal which recurs after a regular time interval, but also a signal which recurs after an irregular time interval and/or with a deviating waveform.

In comparison with static level shifters, the level shifter in accordance with the invention also requires less surface area. Moreover, the power consumption of the level shifter in accordance with the invention is substantially lower.

The level shifter is preferably used in a driver circuit for controlling the row-wise and column-wise arranged display elements of a display, for example an LCD display. A plurality of level shifters can then be advantageously combined so that a number of components can be used in common in a number of level shifters. For example, a spike generator can then apply the same recurrent signal to several level shifters simultaneously. Such common use results in a substantial further reduction of the surface area required.

It is to be noted that the level shifter and driver circuits in accordance with the invention can be realised on a semiconductor substrate or also according to the so-called thin-film technique. In this respect reference is made to the article by J.C. Erskine and P.A. Snopko "A thin-film-transistor-controlled liquid-crystal numeric display", IEEE TED 26 (5), 1979, pp. 802-806. Thin-film integrated circuits can be advantageously used for display applications where the circuits are integrated in a thin film on a substrate, for example a glass plate or a quartz plate. The substrate then forms part of the screen of the (LCD) display. It will be evident that a higher degree of system integration can thus be achieved.

The invention will be described in detail hereinafter with reference to a drawing; therein:

Fig. 1 shows an example of a dynamic level shifter,

Fig. 2 shows an example of a level shifter in accordance with the invention,

Fig. 3 shows the voltages at various points in the circuit shown in Fig. 2, and

Fig. 4 shows an array of level shifters in accordance with the invention which use parts in common.

Fig. 1 shows a dynamic level shifter 10 which is integrated on a semiconductor substrate in the present example. The level shifter 10 comprises a P-channel transistor 16 between a first supply terminal 12 and the output 14 and an N-channel transistor 20 between the output 14 and a second supply terminal 18. The supply voltage on the terminal 12 is, for example 5 V and that on the terminal 18 is, for example minus 30 V. The input 22 receives input signals whose level (for example, 0-5 V) is transformed by the level shifter 10. The input 22 is directly connected to the gate of the transistor 16 and the capacitance 24 realises a capacitive coupling between the input 22 and the gate of the transistor 20. There is also provided a control discharging path for the gate of the transistor 20 which in this case comprises the output branch 26 of a current mirror 28. The control discharging path ensures that an accumulation of charge on the gate of the transistor 20, caused by a positive signal transition on the input 22, flows to the terminal 18. On the other hand, the PN-junction 30, being inherent of a P-well technology, provides equalization in the case of a negative signal transition on the input 22. The control discharging path as well as said PN-junction prevent a floating potential on the gate. It is a drawback of this circuit that the lowest level of the output signal on the output 14 does not have a fixed value, because the transistor 20 is turned on only during and briefly after a positive transition of the input signal. The circuits controlled by the output signal thus have to respond only briefly to the negative transition of the

output signal or buffering is required at the input side.

Fig. 2 shows an embodiment of a level shifter 40 in accordance with the invention which does not have said drawbacks. The reference numerals corresponding to those used in Fig. 1 denote similar or identical components. Instead of the direct capacitive coupling of the input 22 to the gate of the N-channel transistor 20, the input signal is first combined with a spike-shaped recurrent signal in the logic gate 42 whose input side is connected to the input 22 and to a spike generator 44. The signals present at various points in the circuit are shown in Fig. 3. The upper line V_{22} represents the input signal on the input 22. The second line V_1 represents the spike-shaped recurrent output signal of the spike generator 44; the line V_2 therebelow represents the signal combined in the logic gate 42 which is subjected to the capacitance 24. V_3 represents the signal filtered by the capacitance 24 and present on the gate of the transistor 20, and the line 14 represents the output signal of the level shifter on the output 14. As a result of the combination operation, the voltage on the gate of the transistor 20 is periodically regenerated. This means that the logic high level of this voltage remains defined within a given range and hence also the low level of the output signal V_{14}.

Instead of a spike-shaped signal, a signal having an arbitrary waveform can be used when this signal is recurrently applied to the logic gate 42 during a short period of time.

Fig. 4 shows an embodiment comprising a plurality of n level shifters in accordance with the invention, the spike generator 44 as well as the input branch of the current mirror 28 being shared by a plurality of level shifters a ... n. This embodiment offers the advantage that the surface area required and also the current consumption are reduced. In this Figure each of the elements of the level shifters a... n is denoted by the same reference numeral as used in Fig. 2, supplemented by one of the letters a n.

It is to be noted that the described embodiments relate to combined control of the N-channel transistor. A similar arrangement in the complementary case, *i.e.* in the case of capacitive control of the P-channel transistor, can be controlled in a similar manner.

It is also to be noted that the same principle can also be used, for example in the case of a push-pull stage consisting of two N-channel transistors.

Finally it is to be noted that instead of a current mirror as used in the abovepreferred embodiment, other control input discharging paths can be used, such as a diode, for example a high-ohmic polydiode, a resistor, a parallel connection of a resistor and a diode.

Claims

1. A level shifter comprising a charging path between a first supply voltage and an output, and a discharging path between the output and a second supply voltage, the paths being controllable in a mutually complementary fashion by an input signal on an input, one of the paths being dc coupled to the input while the other path is coupled thereto *via* a capacitance, characterized in that in order to regenerate a control voltage on a control input of the other path, the input signal is logically combined with a recurrent signal which can be applied to the control input *via* the capacitance.

2. A level shifter as claimed in Claim 1, characterized in that the level shifter comprises a spike generator for generating a recurrent pulse signal and a logic gate for combining the pulse signal with the input signal.

3. A level shifter as claimed in Claim 1, comprising an output branch of a current mirror arranged in a further discharging path for the control input which extends between the control input and the second supply voltage.

4. A driver circuit comprising at least one level shifter as claimed in Claim 1, 2 or 3.

5. A driver circuit as claimed in Claim 4, comprising a plurality of level shifters, at least one of the following components being used in common for said plurality:
   - a spike generator for generating the recurrent signal;
   - an input branch of a current mirror, a respective output branch of which is connected in a further discharging path between the control input of a relevant other path and the second supply voltage.

6. A driver circuit as claimed in Claim 4 or 5 which is integrated on a semiconductor substrate.

7. A display comprising a matrix of picture elements which are arranged in rows and columns and provided with a driver circuit as claimed in Claim 4 or 5 for controlling at least the rows or the columns.

8. A display as claimed in Claim 7, provided on a substrate, for example a glass plate or a quartz plate, the driver circuit being integrated at least

partly on the substrate.

9. A data display arrangement comprising a display as claimed in Claim 7 or 8.

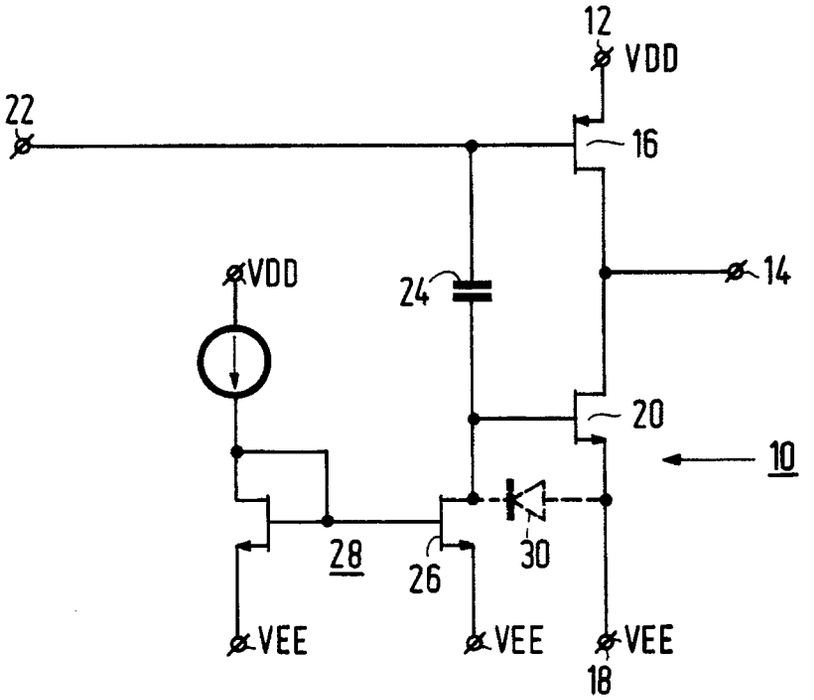
12
VDD
22
16
VDD
24
14
20
10
28
26
30
VEE
VEE
VEE
18

FIG.1

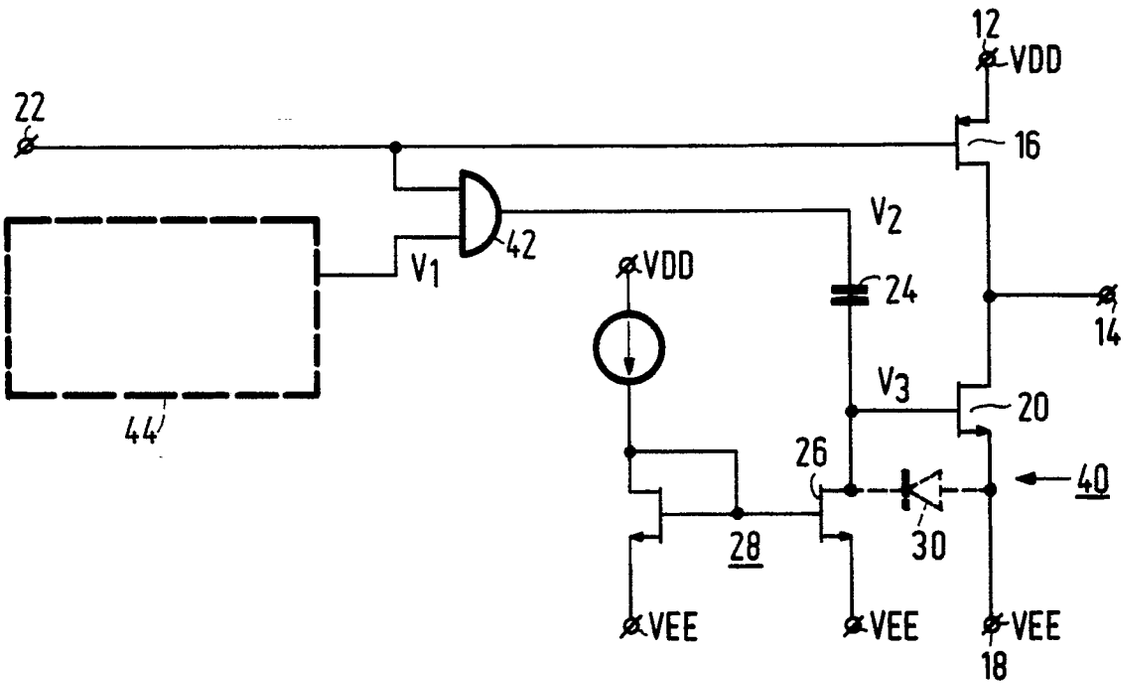
12
VDD
22
16
V2
42
V1
VDD
24
14
V3
20
44
26
40
28
30
VEE
VEE
VEE
18

FIG.2

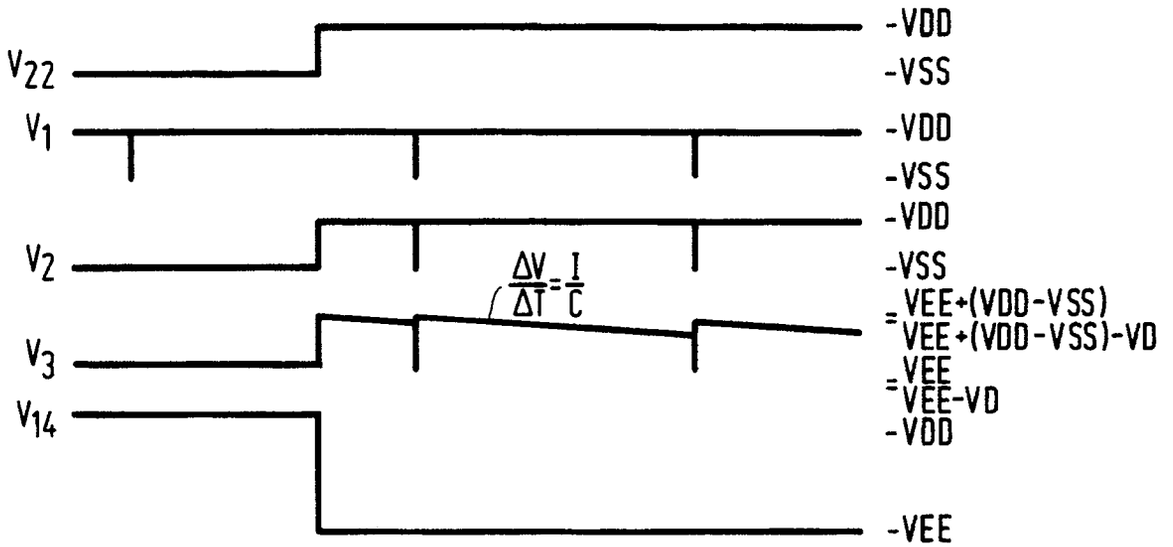
V22
V1
V2
V3
V14
ΔV/ΔT = I/C
-VDD
-VSS
-VDD
-VSS
-VDD
-VSS
= VEE+(VDD-VSS)
VEE+(VDD-VSS)-VD
= VEE
VEE-VD
-VDD
-VEE

FIG.3

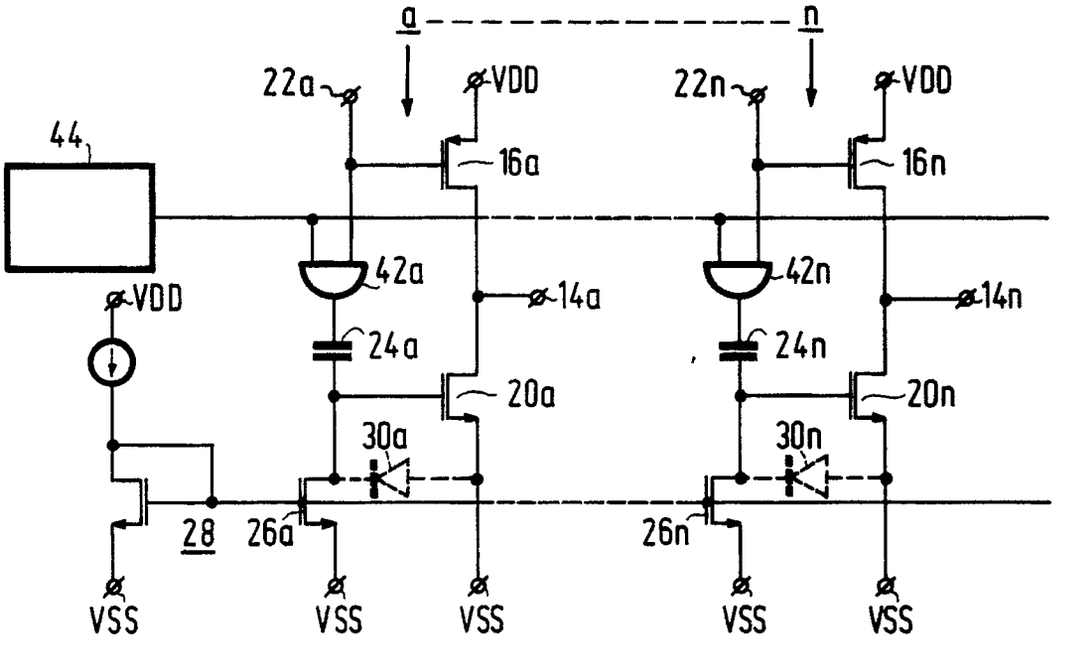
a
n
22a
VDD
22n
VDD
44
16a
16n
42a
42n
VDD
14a
14n
24a
24n
20a
20n
30a
30n
28
26a
26n
VSS
VSS
VSS
VSS
VSS

FIG.4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 20 1050

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 831 280 (A.J. CAYA) * figures 1,3A; column 3, lines 10-41 *	1	H 03 K 19/0185 G 02 F 1/133 G 09 G 3/36
A	US-A-4 384 287 (H. SAKUMA) * figures 3,5,6; column 3, line 55 - column 5, line 45 *	1,4,7,9	
A	US-A-4 064 405 (J.R. CRICCHI et al.) * figure 2; column 2, line 64 - column 3, line 22 *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 243 (E-768)(3591), 7 June 1989; & JP - A - 144619 (SEIKO EPSON CORP.) 17.02.1989	1	
D,A	IEEE TRANSACTIONS ON ELECTRON DEVICES vol. ED-26, no. 5, May 1979, pages 802-806; J.C. ERSKINE et al.: "A Thin-Film-Transistor-Controlled Liquid-Crystal Numeric Display" * figure 8; abstract *	1,4,6,7,9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 02 F 1/133
G 09 G 3/18
G 09 G 3/36
H 03 K 5/02
H 03 K 17/687
H 03 K 19/00
H 03 K 19/0185
H 03 K 19/0948
H 03 K 19/096

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	12 June 91	ARENDT M

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