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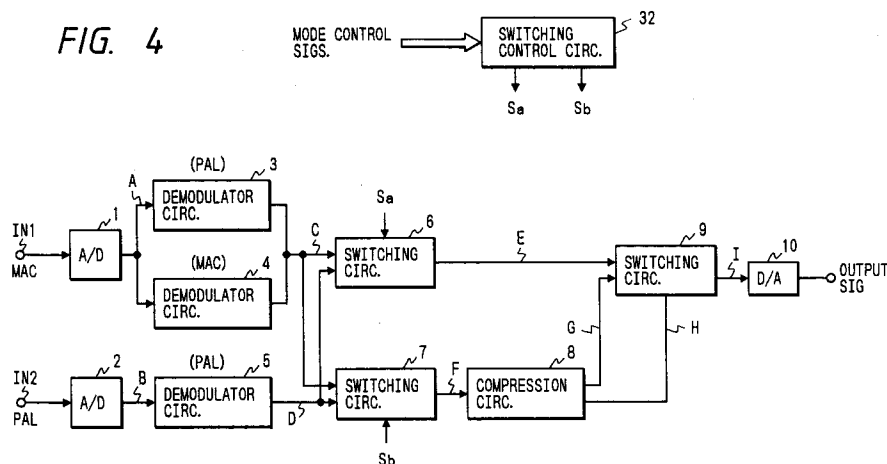
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(54) **Video signal processing circuit for compressed picture insertion function of television receiver.**

(57) A video signal processing circuit for providing a compressed picture insertion function in a television receiver, whereby a compressed-size picture expressed by one video signal is displayed as an insert within a full-size picture that is expressed by another video signal, by demodulating and combining the video signals, which can be of respectively different television standards, such as the PAL and MUSE standards. The circuit utilizes only one de-

modulator circuit for one video signal and two demodulator circuits for the other signal. When one of the video signals is in accordance with a broadcast standard such as the MUSE standard, which requires a large-scale demodulator circuit, a significant reduction in overall circuit scale is achieved by comparison with the prior art, in which two demodulator circuits are required for each of the video signals.

FIG. 4



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EUROPEAN SEARCH REPORT

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EP 91 10 8714

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 86 (E-720)(3434) 28 February 1989 & JP-A-63 262 985 (SANYO) 31 October 1988 * abstract ** - - -	1,3	H 04 N 5/45
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 437 (E-826)(3785) 29 September 1989 & JP-A-1 164 187 (TOSHIBA) 28 June 1989 * abstract ** - - -	1,3	
A	EP-A-0 334 351 (SANYO) * abstract; figure 4A ** - - - - -	1,3	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H 04 N
Place of search		Date of completion of search	Examiner
The Hague		22 January 92	SCHINNERL A.
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