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(54) **Polycrystalline silicon resistors for integrated circuits**

Widerstände aus polykristallinem Silizium für integrierte Schaltungen

Résistance en silicium polycristallin pour circuits intégrés

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- **IBM TECHNICAL DISCLOSURE BULLETIN. vol. 26, no. 2 , July 1983 , NEW YORK US pages 623 - 625 H.S.BHATIA ET AL. 'PROCESS FOR MAKING SIDEWALL RESISTORS WITH SINGLE CRYSTAL CONTACTS'**
- **PATENT ABSTRACTS OF JAPAN vol. 009, no. 004 (E-288)10 January 1985 & JP-A-59 155 128 (MITSUBISHI DENKI K.K.) 4 September 1984**

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Description

The present invention relates generally to integrated circuits, and more specifically to a method for fabricating polycrystalline silicon resistor structures therein.

IBM Tech Disclosure Bulletin Vol 26, No 2, July 1983 pages 623-625 relates to a process for making high value polysilicon resistors. A silicon dioxide layer is formed over an insulating layer. Rectangular windows are etched in the SiO_2 layer using a mask. A layer of doped poly is deposited, and a blanket RIE is used to form sidewalls. The sidewalls form the body of the resistor.

CMOS SRAMs often use a four transistor cell design having resistive load devices. This design is used in order to save chip layout area over the traditional six transistor cell design. Two N-channel transistors are used to form a cross-coupled latch, while two additional N-channel transistors are used to provide access to the cell for reading and writing data. Two load devices are connected between the N-channel transistors in the latch and the power supply.

In the prior art, the resistive load devices are formed after formation of the transistors. After the transistors have been formed, a dielectric layer is deposited and contact openings are formed to the substrate. A second polycrystalline silicon layer is deposited and lightly doped N-type to achieve a resistivity in the range of 10^6 to 10^{13} ohms/square. This blanket implant determines the load resistor value. The resistivity of the load resistors must be low enough to supply ample current to compensate for transistor leakages, but high enough to allow for sufficient standby currents for proper device operation under adverse conditions.

Resistance of the polycrystalline silicon load structures is a function of four variables. These are: the grain structure of the polycrystalline silicon used to form the resistor structure, the impurity levels used to dope the polycrystalline silicon; the cross-sectional area of the resistive device; and the length of the device. Impurity levels and polycrystalline silicon grain structure can be controlled only to limits determined by the process technology being used. If cross-sectional area of the structure could be reduced, length of the load resistor could also be reduced to preserve a given resistance for a small overall structure.

It would be desirable to provide a polycrystalline silicon resistor structure, and a method for fabricating same, which resulted in resistor structures having a reduced cross-sectional area. It would further be desirable for such a method to be compatible with existing process technologies.

It is therefore an object of the present invention to provide a polycrystalline silicon resistor structure, and method for making same, having a reduced cross-sectional area.

It is a further object of the present invention to provide such a structure and method which is compatible with current process technologies.

It is another object of the present invention to provide such a structure and method which adds a minimal amount of complexity to the process flow used to fabricate the device.

Therefore, according to the present invention, a method for fabricating polycrystalline silicon resistor structure includes steps directed to the provision of a polycrystalline silicon structure having a decreased width. Sidewall spacers are used to narrow a region in which the polycrystalline silicon resistors are formed. This technique provides a reduced cross-section for the resistor structures, allowing shorter resistors to be used, or providing increased resistance for longer resistors.

According to one aspect of the present invention there is provided a method for fabricating a resistor structure in an integrated circuit device, comprising the steps of:

forming a first insulating layer over the device; patterning the first insulating layer to define a resistor structure region for formation of the resistor structure; forming a second insulating layer over the device; anisotropically etching the second insulating layer, leaving insulating sidewalls in the resistor structure region, wherein a narrowed resistor structure region is defined; depositing a layer of polycrystalline silicon over the device; and anisotropically etching the polycrystalline silicon layer, wherein polycrystalline silicon remains in the narrowed resistor structure region to form a resistor structure.

According to another aspect of the present invention there is provided an integrated circuit device structure, comprising: an insulating layer having a resistor structure region between two contact regions, said resistor structure region having substantially vertical side walls; insulating side wall regions along the side walls of the resistor structure region, defining a narrowed region therebetween; and a polycrystalline silicon region located in the narrowed region, wherein said polycrystalline silicon region forms a resistor.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1-4 illustrate the formation of polycrystalline silicon resistor structures according to a first preferred embodiment of the present invention;

Figure 5 illustrates the formation of polycrystalline silicon resistor structures according to an embodiment which does not form part of the invention as claimed.

Figure 6 is a planned view of a resistor formed according to the technique described in connection with **Figures 1-4**; and

Figure 7 illustrates resistive structures formed according to the technique described in connection with **Figure 5**.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to **Figure 1,** integrated circuit devices are formed in a substrate **10.** Field oxide regions **12, 14** separate and define active areas within the substrate **10.** Polycrystalline silicon signal line **16** is used to conduct signals on the device. Signal line **16** is separated from the substrate **10** by gate oxide layer **18.** Sidewall oxide spacers **20** are formed on either side of the signal line **16** as known in the art.

Although the cross-sectional view through signal line **16** shows the same structure as a field effect transistor, signal line **16** can be a non-gate signal line which is utilized in a shared contact region. Signal line **16** will be so used as will be described further below. Active regions **22, 24** function as the source/drain regions of the field effect device if polycrystalline silicon signal line **16** actually functions as a field effect gate. In a shared contact layout, the active areas **22, 24** may actually be connected out of the plane of the drawing, so that the signal line **16** does not function as a gate.

Polycrystalline silicon signal line **26** rests on field oxide region **14**. Oxide sidewall spacers **28** are formed thereon at the same time as sidewall spacers **20**.

Processing to form the elements just described is conventional as known in the art. After formation of the transistor structures, dielectric layer **30** is deposited over the surface of the integrated circuit device. This layer **30** is preferably LPCVD/APCVD/LTO silicon dioxide followed by a deposited layer of LPCVD silicon nitride as known in the art. Other insulating layers may be used if desired.

After formation of dielectric layer **30**, insulating layer **32** is deposited over the surface of the device. Layer **32** is preferably a dielectric which can be easily planarized. Layer **32** may be a reflow glass, for example, BPSG which is deposited and heated to reflow as known in the art. If BPSG is used, the reflow is preferably performed in an ambient atmosphere including steam. The reflow cycle, or other planarization step, results in a near planar surface as shown in Figure 1.

Referring to **Figure 2**, an insulating layer **34** is deposited over the surface of the device. Insulating layer **34** is preferably an LPCVD silicon nitride layer deposited to a depth of approximately 2000-4000 angstroms. Nitride layer **34** is then patterned and etched to define a region **36** in which polycrystalline silicon resistors are to be formed.

Another insulating layer (not shown) is deposited over the surface of the chip, and anisotropically etched without masking to form sidewall spacers **38** within the resistor region **36**. The insulating layer used to form the spacers 38 may be an oxide layer and is preferably an LPCVD/LTO silicon oxide layer. The oxide layer is deposited to a thickness which results in the width of the oxide regions 38 resulting as desired. As known in the art, the width of the spacers 38 is approximately equal to the thickness of the oxide layer from which they are formed. Thus, for example, if a 0.2 micron opening is desired between the spacers 38, and the region 36 is one micron wide, the oxide layer used to produce spacers 38 is deposited to a depth of approximately 4000 angstroms.

After formation of the sidewall spacers **38**, contacts are opened to the substrate **10** and other underlying features through insulating layers **30, 32**, **34**. As examples of the types of contacts which may be formed, contact opening **40** makes contact with active region **22** within a substrate **10**. Contact opening **42** makes contact with both the polycrystalline silicon signal line **16** and active region **24**. The contact to be formed in opening **42** is part of a shared contact region. Contact opening **44** is opened simply to allow contact to underlying polycrystalline silicon line **26**.

Referring to **Figure 3**, a layer of polycrystalline silicon 46 is deposited over the device. Layer 46 is preferably deposited to a depth of approximately 500 to 1500 angstroms. A blanket impurity implant is then made to control the resistivity of the polycrystalline silicon resistors to be fabricated in region 36. If N-type resistors are to be formed, an N^- implant is made.

Referring to **Figure 4**, the polycrystalline silicon layer **46** is patterned and etched to remove it except in the desired contact regions **40, 42, 44** and interconnect regions as desired. This results in various polycrystalline silicon contact structures **48** as shown. The layer 46 is etched to completely clear it, which can be accomplished by etching until the end point is reached as known in the art, and continuing the etch for a period of time approximately ten percent beyond reaching the end point Such an over etch insures that undesired polycrystalline silicon regions do not remain behind.

During etching of the polycrystalline silicon layer **46**, resistor region **36** is left unmasked. This causes the polycrystalline silicon overlying such region **36** to be etched away. However, due to the depth of the region **36**, some material remains in the region between the sidewall spacers **38**. This polycrystalline silicon region **50** provides the resistor desired for use in the device.

As will be apparent to those skilled in the art, the cross-sectional area of resistor **50** is much smaller than a resistor which fills the resistor region **36**.

A masked N^+ implant can then be made to reduce the resistivity of the polycrystalline silicon contacts and interconnect **48**. Remaining fabrication steps for the device, such as formation of further polycrystalline silicon and metal interconnect layers, is completed in a conventional manner. To a great extent, the device is already planarized due to the planarization of insulating layer **32**, so that further planarization steps may be minimized or not required.

Referring to **Figure 5**, an alternative technique for fabricating small cross-section polycrystalline silicon resistor structures is shown. This technique does not form part of the invention as claimed. The technique used is very similar to that described in connection with **Figures 1 - 4**. The difference is that the deposition of the oxide layer, and anisotropic etching thereof to form sidewall spacers **38**, is not performed. Instead, when polycrystalline silicon layer 46 is deposited over the device, it extends across the entire width of resistor region **36**. When the polycrystalline silicon is anisotropically etched to form contact and interconnect regions **48**, sidewall polycrystalline silicon regions **52** are formed within the resistor region **36**. These regions **52** are separated by region **54** in much the same manner that sidewall oxide regions **38** were separated as described in connection with **Figure 2**. The width of the polycrystalline silicon resistors **52** is controlled by the depth to which polycrystalline silicon layer **46** is deposited. The height of the resistor regions **52** is controlled by the depth to which the nitride layer **34** is deposited. Decreasing the depth of nitride layer **34**, or the thickness of polycrystalline silicon layer **46**, results in resistor regions **52** having a smaller cross-sectional area

Further processing of the device after the stage shown in **Figure 5** is completed in a conventional manner as described above in connection with **Figure 4**.

Figure 6 illustrates a plan view of a polycrystalline silicon resistor formed according to the techniques described in connection with **Figures 14**. Polycrystalline silicon contacts **60** connect to signal lines **62**. Lines **64** indicate the boundaries of the resistor region **36**. Polycrystalline silicon resistor **66** connects the contacts **60**.

As can be seen, the cross-sectional area of the polycrystalline silicon resistor **66** is greatly reduced from that which would normally be formed connecting contact regions **60**. This allows a much higher valued resistor to be formed, or a shorter resistor to be used. Use of shorter resistor **66** allows the contacts **60** to be placed closer together, if desired, thereby reducing the overall layout area required for circuit structures such as 4-transistor SRAM cells.

Figure 7 is a plan view of a device constructed according to the method described in connection with **Figure 5**. This devices does not form part of the invention as claimed. Contact regions **70** are connected to signal lines **72**. Polycrystalline silicon resistors **74** connect the contact regions **70**. Since the resistors are formed on both sidewalls of the resistor region **36**, two parallel resistors **74** are formed. The twin resistor structures **74** shown in **Figure 7** have the same advantages as the single structure **66** shown in **Figure 6**, and can be fabricated with a lesser number of process steps.

The resistor structures described above provide polycrystalline silicon resistor structures which have a reduced width, and thus a reduced cross-sectional area Use of such resistor structures in circuits such as CMOS SRAM cells allows the use of shorter resistors for a given required resistance. This can lead to smaller cell layout areas, and increased device density on an integrated circuit chip.

Claims

1. A method for fabricating a resistor structure (50,66) in an integrated circuit device, comprising the steps of:

   forming a first insulating layer (34) over the device;

   patterning the first insulating layer (34) to define a resistor structure region (36) for formation of the resistor structure;

   forming a second insulating layer over the device;

   anisotropically etching the second insulating layer, leaving insulating sidewalls (38) in the resistor structure region, wherein a narrowed resistor structure region is defined;

   depositing a layer of polycrystalline silicon (46) over the device; and

   anisotropically etching the polycrystalline silicon layer (46), wherein polycrystalline silicon remains in the narrowed resistor structure region to form a resistor structure (50,66).

2. The method of claim 1, further comprising the step of:

   before said polycrystalline silicon etching step, masking portions of the polycrystalline silicon layer (46) to protect selected regions thereof, leaving the resistor structure region unmasked, wherein the selected regions of the polycrystalline silicon layer (48) are protected from etching during the polycrystalline silicon etching step.

3. The method of claim 2, further comprising the step of:

before said polycrystalline silicon deposition step, etching contacts (40) to underlying circuit structures, wherein the contacts (40), after the polysilicon deposition step, will be masked so as to be included in the selected regions (48).

4. The method of claim 1, wherein the first insulating layer (34) comprises silicon nitride.

5. The method of claim 1, wherein the second insulating layer comprises a deposited oxide.

6. The method of claim 1, further comprising the step of:

prior to said first insulating layer forming step, planarizing a surface of the integrated circuit device.

7. The method of claim 6, wherein said planarizing step comprises the steps of:

depositing a layer of reflowable glass (32) over the device; and

heating the device to a temperature sufficient to cause the glass layer to flow into a relatively planar layer (32).

8. The method of claim 7, wherein the reflowable glass comprises BPSG.

9. An integrated circuit device structure, comprising:

an insulating layer (34) having a resistor structure region (36) between two contact regions (60) said resistor structure region (36) having substantially vertical side walls;

insulating side wall regions (38) along the side walls of the resistor structure region (36), defining a narrowed region therebetween; and

a polycrystalline silicon region (50) located in the narrowed region, wherein said polycrystalline silicon region (50) forms a resistor(50,66).

10. The structure of claim 9, wherein the resistor comprises a load structure for an SRAM cell.

Patentansprüche

1. Verfahren zum Herstellen einer Widerstandsstruktur (50, 66) in einem Bauelement einer integrierten Schaltung, welches die Schritte umfaßt:

Ausbilden einer ersten Isolationsschicht (34) über dem Bauelement;

Strukturieren der ersten Isolationsschicht (34), um einen Widerstandsstrukturbereich (36) für die Ausbildung der Widerstandsstruktur zu definieren;

Ausbilden einer zweiten Isolationsschicht über dem Bauelement;

anisotropes Ätzen der zweiten Isolationsschicht, wobei die isolierenden Seitenwände (38) in dem Widerstandsstrukturbereich zurückbleiben, wodurch ein verengter Widerstandsstrukturbereich definiert wird;

Auftragen einer Schicht aus polykristallinem Silizium (46) über dem Bauelement; und

anisotropes Ätzen der Schicht (46) aus polykristallinem Silizium, wobei das polykristalline Silizium in dem verengten Widerstandsstrukturbereich zum Ausbilden einer Widerstandsstruktur (50, 66) zurückbleibt.

2. Verfahren nach Anspruch 1, welches ferner den Schritt umfaßt:

vor dem Ätzschritt des polykristallinen Siliziums Abschnitte der Schicht (46) aus polykristallinem Silizium zu maskieren, um ausgewählte Bereiche davon zu schützen, wobei der Widerstandsstrukturbereich unmaskiert bleibt, und die ausgewählten Bereiche der Schicht (48) aus polykristallinem Silizium während des Ätzschrittes des polykristallinen Siliziums ätzgeschützt werden.

3. Verfahren nach Anspruch 2, welches ferner den Schritt umfaßt:

vor dem Auftragungsschritt des polykristallinen Siliziums Kontakte (40) zu darunterliegenden Schaltungsstrukturen zu ätzen, wobei die Kontakte (40) nach dem Auftragungsschritt des Polysiliziums so maskiert werden, daß sie in den ausgewählten Bereichen (48) enthalten sind.

4. Verfahren nach Anspruch 1, bei welchem die erste Isolationsschicht (34) Siliziumnitrid enthält.

5. Verfahren nach Anspruch 1, bei welchem die zweite Isolationsschicht ein aufgetragenes Oxid enthält.

6. Verfahren nach Anspruch 1, welches ferner den Schritt umfaßt:

vor dem Ausbildungsschritt der ersten Isolationsschicht eine Oberfläche des Bauelementes der integrierten Schaltung zu planarisieren.

7. Verfahren nach Anspruch 6, bei welchem der Planarisierungsschritt die Schritte umfaßt:

Auftragen einer Schicht aus aufschmelzbarem Glas (32) über dem Bauelement; und

Aufheizen des Bauelementes auf eine Temperatur, die ausreichend ist, daß die Glasschicht

in eine relativ planare Schicht (32) ausfließt.

8. Verfahren nach Anspruch 7, bei welchem das aufschmelzbare Glas BPSG enthält.

9. Bauelementestruktur einer integrierten Schaltung mit:

einer Isolationsschicht (34) mit einem Widerstandsstrukturbereich (36) zwischen zwei Kontaktbereichen (60), wobei der Widerstandsstrukturbereich (36) im wesentlichen vertikale Seitenwände aufweist;
Isolationsseitenwandbereichen (38) entlang der Seitenwände des Widerstandsstrukturbereiches (36), die dazwischen einen verengten Bereich definieren; und
einem Bereich (50) aus polykristallinem Silizium, der in dem verengten Bereich angeordnet ist, wobei der Bereich (50) aus polykristallinem Silizium einen Widerstand (50, 66) ausbildet.

10. Struktur nach Anspruch 9, bei welcher der Widerstand eine Laststruktur für eine SRAM-Zelle ausweist.

Revendications

1. Procédé pour fabriquer une structure de résistance (50, 66) dans un dispositif à circuit intégré, comprenant les étapes consistant à :

former une première couche isolante (34) sur le dispositif ;
affecter d'un motif la première couche isolante (34) pour définir une zone de structure de résistance (36) pour la formation de la structure de résistance ;
former une seconde couche isolante sur le dispositif ;
effectuer une attaque anisotropique de la seconde couche isolante, en laissant des parois latérales isolantes (38) dans la zone de structure de résistance, dans laquelle une zone de structure de résistance restreinte est définie ;
déposer une couche de silicium polycristallin (46) sur le dispositif ; et
effectuer une attaque anisotropique de la couche de silicium polycristallin (46), dans laquelle du silicium polycristallin demeure dans la zone de structure de résistance restreinte pour former une structure de résistance (50, 66).

2. Procédé de la revendication 1, comprenant en outre l'étape consistant à :

avant ladite étape d'attaque de silicium polycristallin, masquer des parties de la couche de silicium polycristallin (46) pour protéger des zones sélectionnées de celle-ci, en laissant la zone de structure de résistance non masquée, dans laquelle les zones sélectionnées de la couche de silicium polycristallin (48) sont protégées contre une attaque durant l'étape d'attaque de silicium polycristallin.

3. Procédé de la revendication 2, comprenant en outre l'étape consistant à :

avant ladite étape de dépôt de silicium polycristallin, attaquer des contacts (40) vers des structures de circuit sous-jacentes, dans laquelle les contacts (40), après l'étape de dépôt de polysilicium, seront masqués de manière à être compris dans les zones sélectionnées (48).

4. Procédé de la revendication 1, dans lequel la première couche isolante (34) comprend du nitrure de silicium.

5. Procédé de la revendication 1, dans lequel la seconde couche isolante comprend un oxyde déposé.

6. Procédé de la revendication 1, comprenant en outre l'étape consistant à :

avant ladite étape de formation de la première couche isolante, aplanir une surface du dispositif à circuit intégré.

7. Procédé de la revendication 6, dans lequel ladite étape d'aplanissement comprend les étapes consistant à :

déposer une couche de verre de fusion (32) sur le dispositif ; et
chauffer le dispositif jusqu'à une température suffisante pour faire en sorte que la couche de verre s'écoule en une couche relativement plane (32).

8. Procédé de la revendication 7, dans lequel le verre de fusion comprend du BPSG.

9. Structure de dispositif à circuit intégré, comprenant :

une couche isolante (34) ayant une zone de structure de résistance (36) entre deux zones de contact (60), ladite zone de structure de résistance (36) ayant des parois latérales sensiblement verticales ;
des zones de parois latérales isolantes (38) le long des parois latérales de la zone de structure de résistance (36), définissant une zone restreinte entre celles-ci ; et
une zone de silicium polycristallin (50) située dans la zone restreinte, dans laquelle ladite zone de silicium polycristallin (50) forme une ré-

sistance (50, 66).

10. Structure de la revendication 9, dans laquelle la résistance constitue une structure de charge pour une cellule de SRAM.

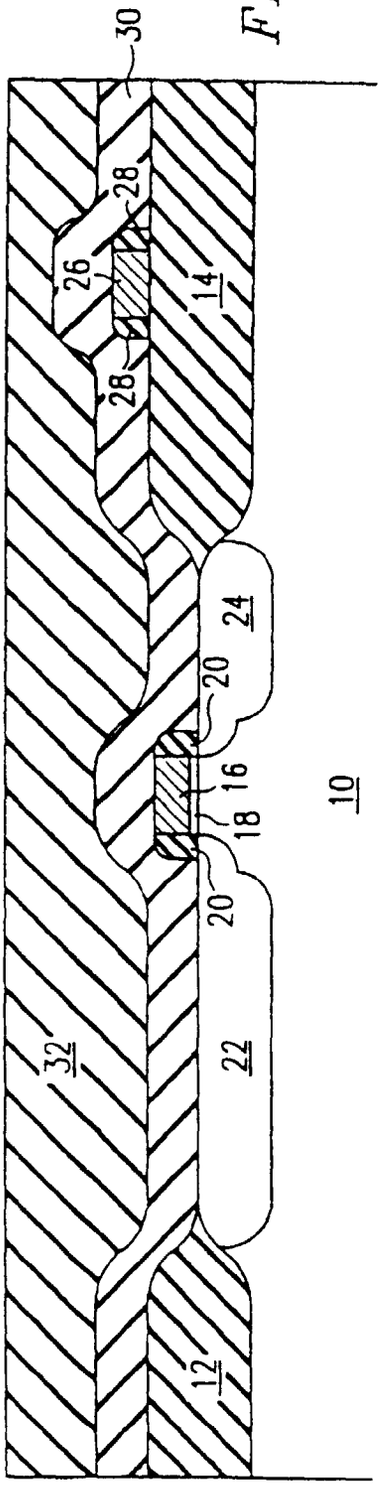
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FIG. 1

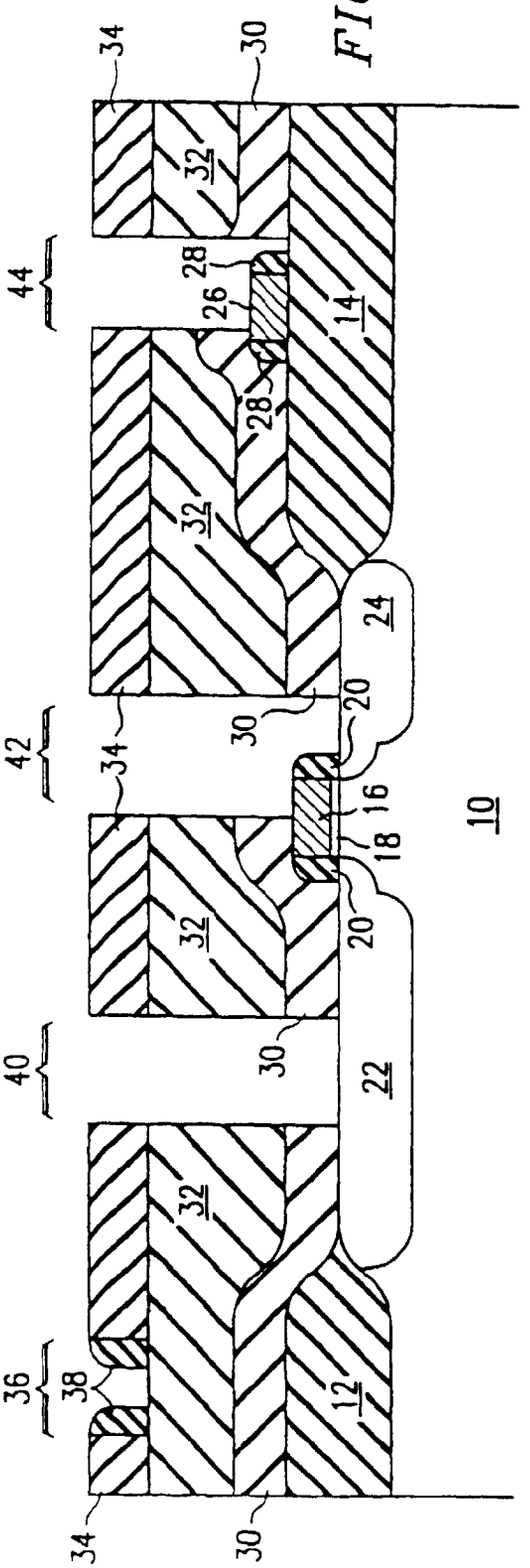
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FIG. 2

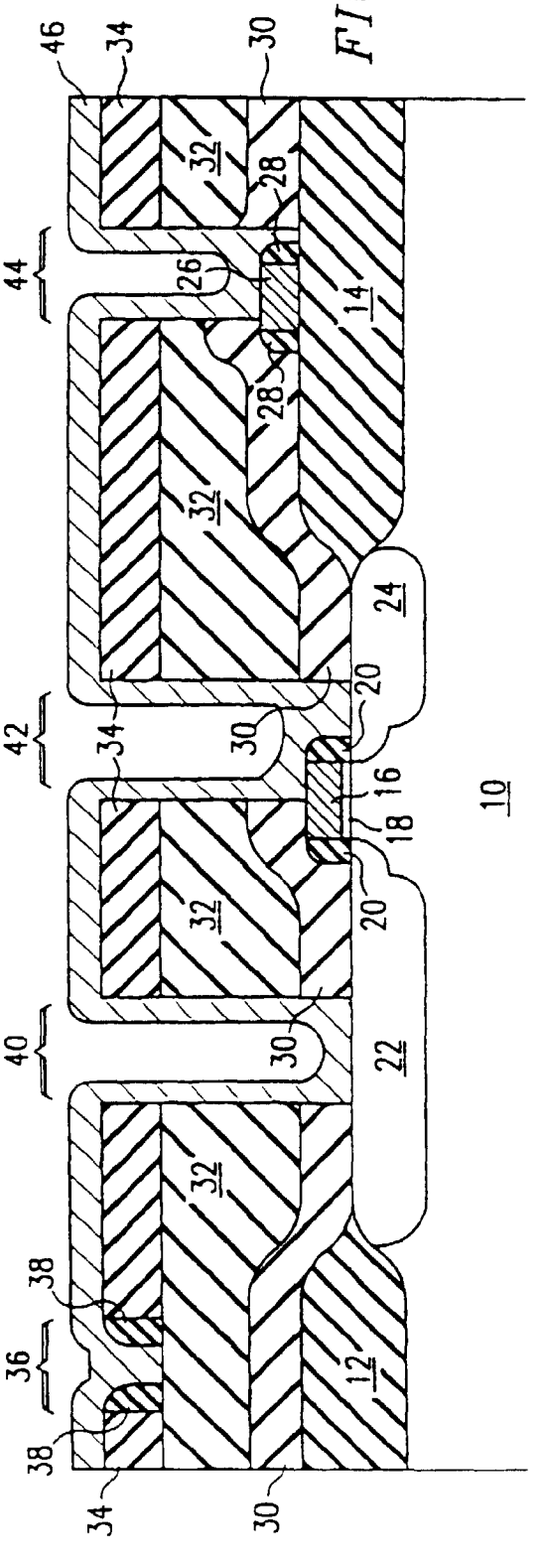
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FIG. 3

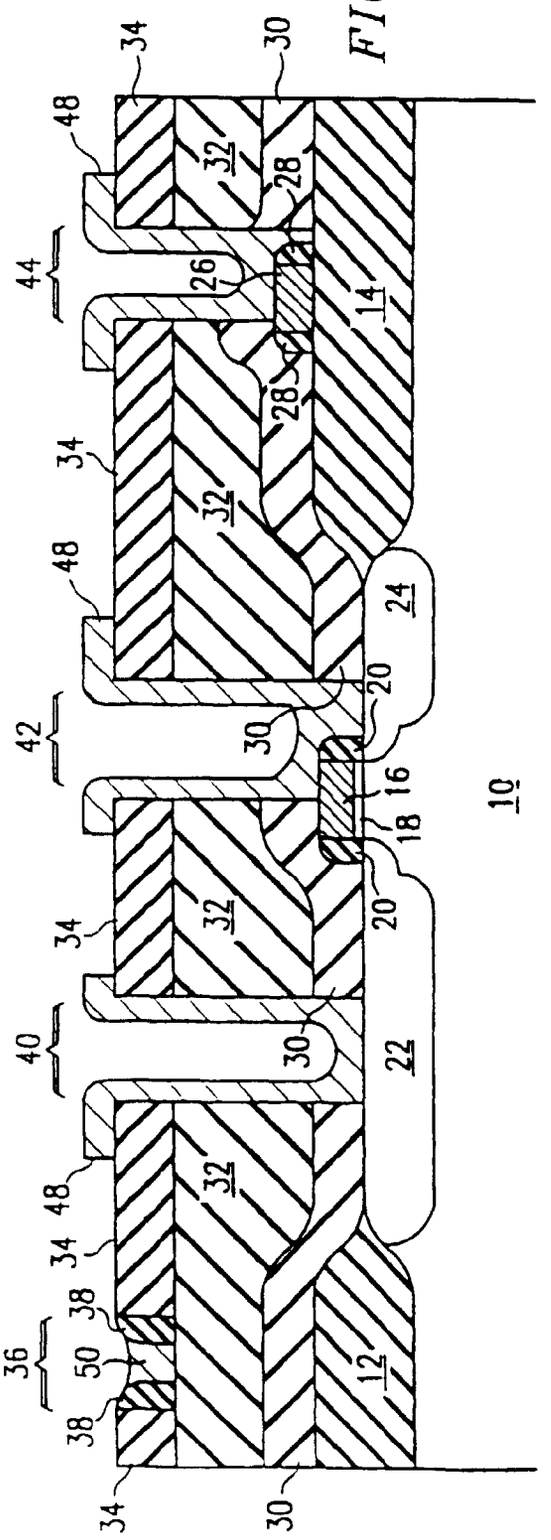
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FIG. 4

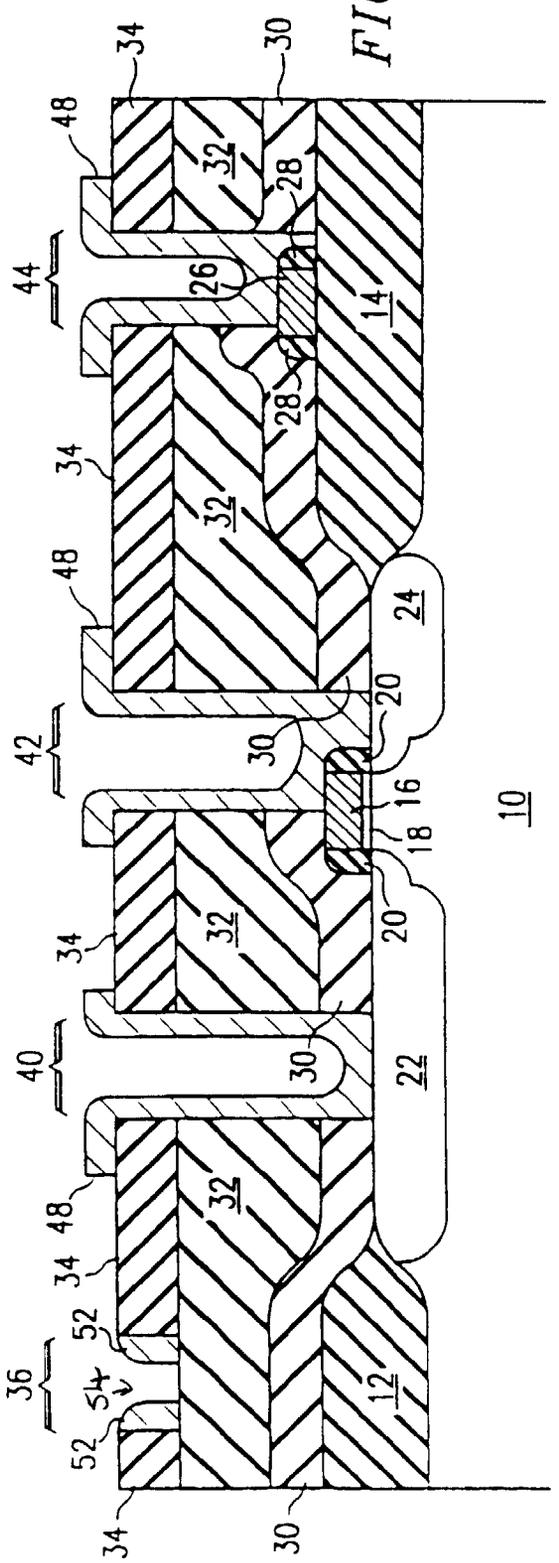

FIG. 5

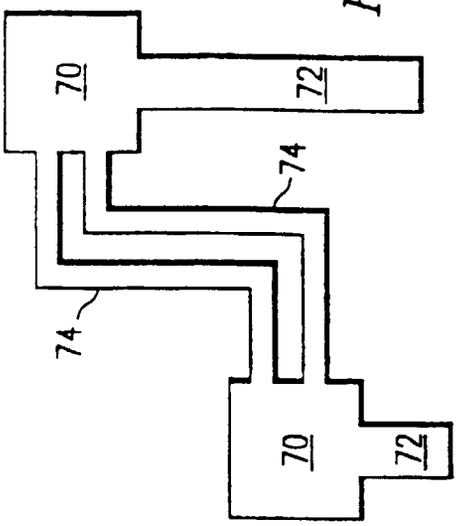

FIG. 7

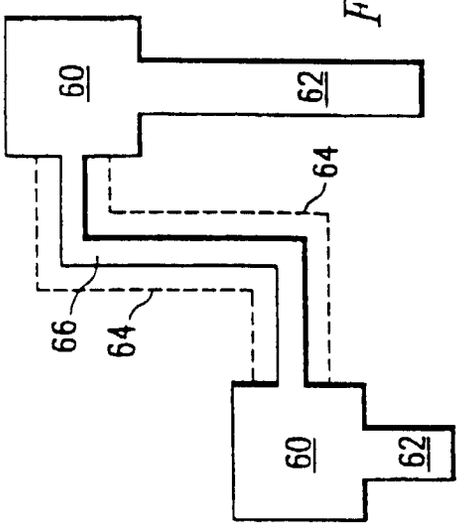

FIG. 6