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54 **Dynamic random access memory device.**

57 A semiconductor memory device comprises first sense amplifier driving lines ($l_2, l_1: L_n, L_p$) and second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42}$; SAN, SAP), the first sense amplifier driving lines ($l_2, l_1: L_n, L_p$) are formed in a first wiring layer (W_1) along the word line direction (WL), and the second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42}$; SAN, SAP) are formed in a second wiring

layer (W_2) along the bit line direction (BL). Therefore, a current flowing in the each of the first sense amplifier driving lines ($l_2, l_1: L_n, L_p$) becomes small, and the width of the the first sense amplifier driving lines ($l_2, l_1: L_n, L_p$) becomes small, so that occupancy area of the semiconductor memory device can be decreased and a large scale integration can be realized.

Fig.10A

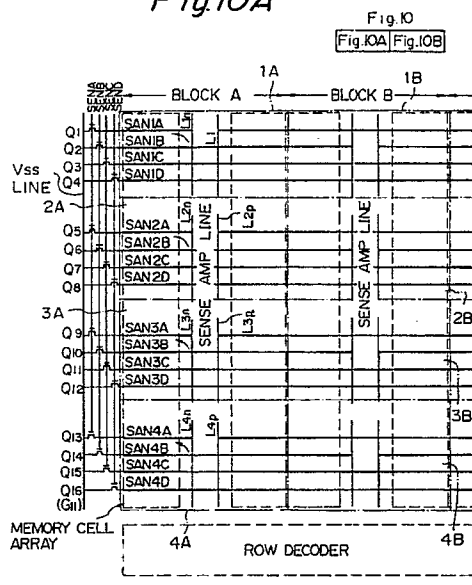
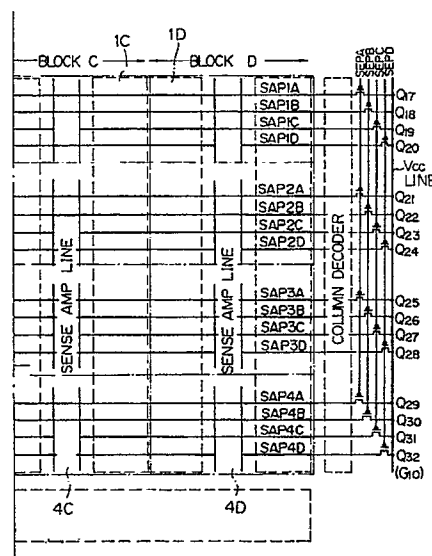


Fig.10B



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The present invention relates to a semiconductor memory device, more particularly, to a large capacity dynamic random access memory device for decreasing an occupancy area by providing sense amplifier driving lines over sense amplifiers and memory cells.

Recently, in a semiconductor memory device, it is required that an area of each portion in the semiconductor memory device be made small in accordance with increasing the capacity of a bit line. It is useful for decreasing the occupancy area of each portion in the semiconductor memory device to minutely form a configuration of the semiconductor memory device, and to provide efficient wirings.

Generally, in a semiconductor memory device, a plurality of lines are required, for example, bit lines, word lines, data buses, sense amplifier driving lines, column select lines, power supply lines, and the like. The bit lines are constituted by polycrystal silicon and a diffusion layer formed on a substrate, and the word lines are constituted by polycrystal silicon accompanied with a gate of the memory cell transistor, and a metal (aluminium) wiring backing the polycrystal silicon to decrease a resistance thereof. For example, the wiring layers are constituted by seven layers, i.e., four polycrystal silicon layers, two aluminium layers, and one diffusion layer. The sense amplifier driving lines and the data buses running in the lengthwise direction (word line direction) and the column select lines running in the lateral direction (bit line direction) are constituted in respective aluminium wiring over the memory portion. Nevertheless, the power supply lines for applying a low and a high voltage to each of the sense amplifier driving lines along the lengthwise direction are not formed over the memory portion but are formed in the circumference of the memory portion along the lateral direction, and data bus lines connected to the data buses and data latch circuit are formed in the circumference of the memory cell portion along the lateral direction. Namely, the areas for the power supply lines and the data bus lines along the lateral direction should be provided in the circumference of the memory cell portion. Furthermore, a plurality of sense amplifiers arranged as a line-shape in the lengthwise direction are connected to the same sense amplifier driving lines in the lengthwise direction, and thus a width of each sense amplifier driving line becomes large. Therefore, the occupancy area of the semiconductor memory device becomes large.

Furthermore, in the conventional semiconductor memory device, when the sense amplifier driving lines are running along the word line direction (sense amp line direction), all sense amplifiers in the sense amp line are driven by the same driving

lines. Note, the width of the driving lines close to the power lines should be made large, as the currents flowing in all the sense amplifiers in the sense amp line are flown to the power lines through the driving lines close to the power lines.

Additionally, in recent years, the capacity of DRAM devices become large, and a memory cell of the DRAM is constituted by a solid structure of a three dimensional stacked capacitor cell. This stacked capacitor cell is useful for reducing an occupancy area of the memory cell without decreasing the capacitance thereof. In the circumference of the memory cell portion, a plurality of peripheral circuits, for example, a sense amplifier, a bit line driver, a row decoder, a column decoder, and the like, are provided. Note, these peripheral circuits are constituted by normal semiconductor elements whose height corresponds to a single layer, the memory cell is constituted by the three dimensional stacked capacitor cell whose height corresponds to a plurality of layers, and thus an excessive difference is caused at the border portion between the memory cell portion and the peripheral circuit portion. This level difference between the memory cell portion and the peripheral circuit portion can not be included in a depth of focus of a exposure system. Therefore, the aluminium wirings can not be freely formed over the memory cell portion and peripheral circuit portion in high accuracy, and thus an occupancy area of the DRAM device can not be decreased.

It is an object of the present invention to provide a semiconductor memory device having a large capacity and a small occupancy area. Furthermore, it is another object of the present invention to provide a semiconductor memory device having a large capacity and a high speed operation.

According to the present invention, there is provided a semiconductor memory device comprising: a plurality of word lines; a plurality of bit lines formed crossing the word lines; a plurality of memory cells, each connected between the one word line and the one bit line; a plurality of sense amplifiers, arranged along the word line direction; a first power supply line; a second power supply line; a plurality of first sense amplifier driving lines, connected to the sense amplifiers and formed in a first wiring layer; and a plurality of second sense amplifier driving lines, each connected between the corresponding first sense amplifier driving line and one of the first and second power supply lines, and formed in a second wiring layer.

The first sense amplifier driving lines may be formed along the word line direction, and the second sense amplifier driving lines may be formed along the bit line direction. The first sense amplifier driving lines may be connected to the first and

second power supply line at a plurality of portions through a plurality of the second sense amplifier driving lines.

The sense amplifiers and the memory cells may be divided into a plurality of blocks. Each of the second sense amplifier driving lines may be connected to one of the first and second power supply lines through a gate transistor, so that one of the divided blocks may be selected. The sense amplifiers may be arranged as a sense amplifier line of a line-shape along the word line direction, and the memory cells may be divided into two groups provided for both sides of the sense amplifier line, in each of the blocks.

Each of the blocks may be divided into a plurality of units. Each of the first sense amplifier driving lines may be divided into a plurality of first unit sense amplifier driving lines corresponding to the units, each of the second sense amplifier driving lines may be divided into a plurality of second unit sense amplifier driving lines connected to the corresponding first unit sense amplifier driving lines. Each of the second unit sense amplifier driving lines may be connected to the first and second power supply lines through a gate transistor.

The gate transistors connected to the corresponding second unit sense amplifier driving lines in the same divided block may be controlled by the same control signal, so that one of the divided blocks may be selected and the units in the selected block are selected at the same timing. The gate transistors connected to the corresponding second unit sense amplifier driving lines in the same divided block may be controlled by one read out signal and the other refresh signals, so that one unit including a memory cell for reading out in a selected block may be read out at high speed and the other units in the selected block are only refreshed at different timing than the read out operation. A voltage value of the read out signal may be higher than that of the refresh signal, so that the read-out operation unit may be speedily driven and the refresh operation unit may be slowly driven.

The semiconductor memory device may further comprise data bus lines and a data latch circuit, the data bus lines may be connected between the sense amplifiers and the data latch circuit. The data bus lines may comprise first data bus lines connected to the sense amplifiers and formed in the first wiring layer along the word line direction, and second data bus lines connected between the corresponding first bus lines and the data latch circuit and formed in the second wiring layer along the bit line direction. The second data bus lines may be connected to a plurality of the first data bus lines and the data latch circuit through gate transistors, the gate transistors may be controlled by a selector, so that one of the first

data bus lines may be selected and connected to the data latch circuit. The first data bus lines may be divided into a plurality of group bus lines, the second data bus lines and the data latch circuit may be provided in accordance with the divided group bus lines, and the second data bus lines may be connected to the corresponding group bus lines and the data latch circuit through a switching circuit, so that each one of the group bus lines may be selected and connected to the each data latch circuit.

The semiconductor memory device may comprise further signal lines formed in the first wiring layer and the second wiring layer. The second sense amplifier driving lines may be formed between a memory cell portion and a peripheral circuit portion, and the second sense amplifier driving lines may be connected to the one of the first and second power supply lines through a connection conductor. Each of the memory cell may comprise a stacked capacitor and a memory cell transistor. The first wiring layer and the second wiring layer provided above the memory cells and the sense amplifiers may be used to form data bus lines, sense amplifier driving lines, the other signal lines, and power supply lines.

Furthermore, according to the present invention, there is also provided a semiconductor memory device comprising: a plurality of word lines; a plurality of bit lines formed crossing the word lines; a plurality of memory cells, each connected between the one word line and the one bit line; a plurality of sense amplifiers, each connected to a pair of the bit lines; a first power supply line; a second power supply line; and a pair of sense amplifier driving layers, connected between the first and second power supply lines and each of the sense amplifiers, and formed in a wiring layer over the memory cells and the sense amplifiers.

The present invention will be more clearly understood from the description of the preferred embodiments as set forth below with reference to the accompanying drawings, wherein:

Figure 1 is a circuit diagram for explaining an example of a semiconductor memory device in a related art;

Figure 2 is a block diagram for explaining problems of the semiconductor memory device in the related art;

Figure 3 is a basic diagram indicating a first embodiment of a semiconductor memory device according to the present invention;

Figure 4 is a circuit diagram indicating the first embodiment of the semiconductor memory device according to the present invention;

Figure 5 is a circuit diagram indicating a modification of the first embodiment of the semiconductor memory device according to the present

invention;

Figure 6 is a block diagram indicating a layout of memory cell blocks and sense amplifier lines of a DRAM device;

Figure 7 is a basic diagram indicating a second embodiment of a semiconductor memory device according to the present invention;

Figure 8 is a circuit diagram indicating the second embodiment of the semiconductor memory device according to the present invention;

Figure 9 is a block circuit diagram indicating a part of the semiconductor memory device shown in Fig. 8;

Figure 10 is a circuit diagram indicating a third embodiment of a semiconductor memory device according to the present invention;

Figure 11 is a sectional diagram indicating a part of the semiconductor memory device shown in Fig. 10;

Figure 12 is a circuit diagram indicating a part of the semiconductor memory device shown in Fig. 10;

Figure 13 is a block circuit diagram indicating a modification of the third embodiment of the semiconductor memory device according to the present invention;

Figure 14 is a diagram indicating a timing chart for explaining an operation of a preferable sense amplifier for the semiconductor memory device shown in Fig. 13;

Figure 15A is a circuit diagram indicating an example of a driving signal generation circuit for a sense amplifier;

Figure 15B is a diagram indicating a timing chart explaining an operation of the driving signal generation circuit shown in Fig. 15A;

Figure 16A is a circuit diagram indicating another example of a driving signal generation circuit of a sense amplifier;

Figure 16B is a diagram indicating a timing chart explaining an operation of the driving signal generation circuit shown in Fig. 16A;

Figure 17 is a diagram indicating a timing chart for explaining an operation of a semiconductor memory device of a Pseudo Static type;

Figure 18 is a sectional diagram indicating an aluminium wiring between a memory cell element and a peripheral circuit element according to a related art;

Figure 19 is a sectional diagram indicating an aluminium wiring between a memory cell element and a peripheral circuit element according to the present invention; and

Figures 20A to 20G are sectional diagrams for explaining a method of forming the aluminium wiring between the memory cell element and the peripheral circuit element shown in Fig. 19.

First, a semiconductor memory device accord-

ing to a related art will be explained, with reference to Figs. 1 and 2.

In a semiconductor memory device, a plurality of word lines, bit lines, data bus lines, sense amplifier driving lines, column select lines and power supply lines, and the like are formed and used. The number of these lines becomes large in accordance with an increase in capacity, and these lines cannot be formed in a single wiring layer. Therefore, in recent years, the conduction lines are formed in a plurality of wiring layers as a multi-layer device.

Figure 1 is a circuit diagram for explaining an example of a semiconductor memory device in a related art. Note, the circuit diagram shown in Fig. 1 corresponds to a wiring layout on the semiconductor memory device (chip). In Fig. 1, reference WL running in a lengthwise direction denotes a word line, references BL and \overline{BL} running in a lateral direction denote bit lines, and these word line WL and bit lines BL and \overline{BL} are plurally provided in the semiconductor memory device. A memory cell MC is provided at an intersection between each of the word lines WL and each of the bit lines BL and \overline{BL} . Note, in Fig. 1, only units M_{00} and M_{11} are described in detail, and the units $M_{00}, M_{01}, M_{02}, \dots, M_{10}, M_{11}, M_{12}, \dots$ have the same configuration.

As shown in Fig. 1, the sense amplifiers SA are arranged as a sense amp line in the lengthwise direction, or along the word line direction (WL), and data buses DB_2 and DB_3 are formed in parallel to the sense amp line, or along the word line direction (WL). In the unit M_{00} , the bit lines BL and \overline{BL} are connected to the corresponding bus lines in the data bus DB_2 through column gate transistors G_2 and G_3 . Similarly, in the unit M_{10} the bit lines BL and \overline{BL} are connected to the corresponding bus lines in the data bus DB_3 through column gate transistors. Note, the semiconductor memory device shown in Fig. 1 is a DRAM device of a four-bit simultaneous read out type, and the bit lines BL and \overline{BL} in the units $M_{00}, M_{01}, M_{02}, M_{03}$ are connected to eight bus lines of the data bus DB_2 through column gate transistors. Data read out to the data bus DB_2 are latched by data latch circuits DL, and read out externally through gate transistors G_1 and data bus DB_1 running in the bit line direction (lateral direction).

In Fig. 1, lines ℓ_1 and ℓ_2 are sense amplifier driving lines, the sense amplifier driving line ℓ_1 is connected to a high potential power supply line V_{cc} through a gate transistor G_{10} of a p-type MOS transistor, the driving line ℓ_2 is connected to a low potential power supply line V_{ss} through a gate transistor G_{11} of an n-type MOS transistor, and an operation of the sense amplifiers SA is controlled by the gate transistors G_{10} and G_{11} . Note, gate transistors G_4, G_5 and G_6, G_7 are used as cut

gates, transistors Q_{01} , Q_{02} and Q_{03} , Q_{04} are used as reset (short-circuit) transistors, lines ℓ_5 and ℓ_7 are ON/OFF control signal lines of the transistors Q_{01} , Q_{02} and Q_{03} , Q_{04} , and lines ℓ_6 and ℓ_8 are power supply lines for a short-circuit between the bit lines BL and \overline{BL} . The configuration of the other blocks and units are as same as the blocks M_0 , M_1 and the units M_{00} , M_{10} . An X-decoder 10 selects a word line WL, a Y-decoder 20 selects bit lines. Note, in this example, the Y-decoder 20 selects four pairs of bit lines, and reference DR denotes a gate driver circuit.

The memory cells are provided for both sides of right and left of the sense amp line, when selecting the left side memory cells, the right side memory cells are cut off by the cut gate transistors G_6 and G_7 . Conversely, when selecting the right side memory cells, the left side memory cells are cut off by the cut gate transistors G_4 and G_5 .

Generally, the bit lines are constituted by polycrystal silicon and a diffusion layer formed on a substrate. The word lines are constituted by polycrystal silicon accompanied with a gate of the memory cell transistor, and a metal (aluminium) wiring backing the polycrystal silicon to decrease a resistance thereof. In the case that a memory cell is a stacked type, the memory cell is constituted by two layers of polycrystal silicon. Note, in this example, the wiring layers are constituted by seven layers, i.e., four polycrystal silicon layers, two aluminium layers, and one diffusion layer. The data buses DB_2 and DB_3 running in the lengthwise direction (along the word line direction) and the column select lines ℓ_3 and ℓ_4 are constituted by a first layer and a second layer of the two aluminium wirings, respectively. The column select lines ℓ_3 and ℓ_4 and the like are commonly used in both blocks M_{00} and M_{10} to decrease the occupancy area of the semiconductor memory device.

Nevertheless, in the semiconductor memory device shown in Fig. 1, each data bus DB_2 and DB_3 is constituted by eight bus lines (four pairs of bus lines), when assuming a pitch of the bus line to be $3\text{ }\mu\text{m}$, the required width of the each data bus DB_2 and DB_3 becomes $24\text{ }\mu\text{m}$ ($4\text{ pairs} \times 2 \times 3\text{ }\mu\text{m} = 24\text{ }\mu\text{m}$). In the case that the semiconductor memory device is a large capacity (for example, 16 M-bit) DRAM, as shown in Fig. 6, sixteen cell blocks each having a capacity of 1 M-bit are provided in parallel. Note, each cell block comprises 2 K (2048) sense amplifiers (sense amp line) and 512 K cell blocks provided for both sides of the sense amp line. Therefore, in a 16 M-bit capacity DRAM, an occupancy area of the total data buses becomes $384\text{ }\mu\text{m}$ ($16\text{ groups} \times 24\text{ }\mu\text{m} = 384\text{ }\mu\text{m}$), so that the occupancy area becomes large. Note, a required width of the data bus DB_1 , which is formed close to the memory cell portion, corresponds to

the width of each data bus DB_2 and DB_3 , so that the area for the data bus DB_1 becomes large.

Figure 2 is a block diagram for explaining problems of the semiconductor memory device in the related art. Note, the block diagram shown in Fig. 2 corresponds to a wiring layout on the semiconductor memory device (chip). As shown in Figs. 1 and 2, in the sense amp line, each sense amplifier SA is supplied with the power supplies Vss and Vcc through the gate transistors and the pair of sense amplifier driving lines $Ln(\ell_2)$ and $Lp(\ell_1)$ which are running along the word line direction (the lengthwise direction). Note, each sense amplifier driving lines drive 2 K (2048) sense amplifiers, a current flowing in each of the driving lines $Ln(\ell_2)$ and $Lp(\ell_1)$ becomes large, and thus a width of the driving line $Ln(\ell_2)$ and $Lp(\ell_1)$ should be determined to about $40\text{ }\mu\text{m}$. Namely, when assuming the number of sense amplifiers to be m , and the current flowing in each sense amplifier to be I_n , then the total current I_{total} flowing in the sense amplifier driving line (Ln), especially at the driving line Ln close to the gate transistor Q_{61} , becomes a value of $(I_n \times m)$.

In recent years, the occupancy area of the sense amp line (sense amplifiers) is not a result of the transistor size in the sense amplifiers, but of the width of the sense amplifier driving lines $Ln(\ell_2)$ and $Lp(\ell_1)$ provided over the sense amp line. For example, in a 16 M-bit DRAM device, an occupancy area of the total sense amplifier driving lines becomes about $1280\text{ }\mu\text{m}$ ($16\text{ groups} \times 2 \times 40\text{ }\mu\text{m} = 1280\text{ }\mu\text{m}$), so that the occupancy area of the DRAM device becomes large. Additionally, as shown in Figs. 1 and 2, the power supply lines connected to the sense amplifier driving lines $Ln(\ell_2)$ and $Lp(\ell_1)$ are provided close to the memory portion along the word line direction. Namely, the high potential power supply line Vcc and the low potential power supply line Vss should be provided at the upper (lower) side and the lower (upper) side of the memory portion in order to apply the low and high potentials to the sense amplifiers through the sense amplifier driving lines $Ln(\ell_2)$ and $Lp(\ell_1)$. The width of the power supply lines Vcc and Vss are also large, and thus the occupancy area of the DRAM device becomes large.

It is an object of the present invention to provide a semiconductor memory device having a large capacity and a small occupancy area.

Below, the preferred embodiments of a semiconductor memory device according to the present invention will be explained with reference to the drawings.

Figure 3 is a basic diagram indicating a first embodiment of a semiconductor memory device according to the present invention. Note, the block diagrams and the circuit diagrams shown in Figs. 3

to 5, 7 to 10, 12 and 13 correspond to wiring layouts on the semiconductor memory device (chip).

As shown in Fig. 3, the semiconductor memory device of the first embodiment comprises a plurality of word lines WL, a plurality of bit lines BL and \overline{BL} , a plurality of sense amplifiers SA, and data buses DB₂ and DB₃. The data buses DB₂ and DB₃ are provided along the word line direction (lengthwise direction) for outputting a potential of the bit lines BL and \overline{BL} amplified by the sense amplifiers SA to an external destination. Note, the data buses DB₂ and DB₃ are connected to a data latch circuit DL through data bus lines ℓ_{12} and ℓ_{13} running along the bit line direction and switching circuit SW (gate transistors 31, 32). The data bus lines ℓ_{12} and ℓ_{13} are provided above memory cells MC and the sense amplifiers SA crossing the data buses DB₂ and DB₃ in a wiring layer. Consequently, the data bus DB₁ shown in Fig. 1 can be deleted, and thus an occupancy area of the semiconductor memory device can be decreased. Furthermore, one data latch circuit DL can be used for receiving data through both data buses DB₂ and DB₃ by controlling the switching circuit SW.

Figure 4 is a circuit diagram indicating the first embodiment of the semiconductor memory device according to the present invention. As shown in Fig. 4, a configuration of the semiconductor memory device of the first embodiment is similar to the semiconductor memory device shown in Fig. 1. The same references in Figs. 1 and 2 indicate the same portion in all drawings.

Namely, in Fig. 4, reference WL denotes a word line, references BL and \overline{BL} denote bit lines, reference MC denotes memory cell, and reference SA denotes a sense amplifier. Note, in Fig. 4, a pair of bit lines BL and \overline{BL} , memory cells MC connected to the bit lines BL and \overline{BL} and a sense amplifier SA are included in each unit (block) M₀₀, M₀₁, M₀₂, ... and M₁₀, M₁₁, M₁₂, ..., and block M₀ and M₁ are formed by a plurality of units M₀₀, M₀₁, M₀₂, ... and M₁₀, M₁₁, M₁₂, ... which are arranged in the lengthwise direction (word line direction).

In Fig. 4, the sense amplifiers SA are arranged as a sense amp line in the word line direction, and data buses DB₂ and DB₃ are formed in parallel to the sense amp line. In the unit M₀₀, the bit lines BL and \overline{BL} are connected to the corresponding bus lines in the data bus DB₂ through column gate transistors G₂ and G₃. Similarly, in the unit M₁₀ the bit lines BL and \overline{BL} are connected to the corresponding bus lines in the data bus DB₃ through column gate transistors. Note, this semiconductor memory device is a DRAM device wherein four-bit data are simultaneously read out, and the bit lines BL and \overline{BL} in the units M₀₀, M₀₁, M₀₂, M₀₃ are connected to eight bus lines of the data bus DB₂

through column gate transistors. Data read out to the data bus DB₂ are latched by data latch circuits DL through the data bus lines ℓ_{12} and gate transistors 31, similarly, data read out to the data bus DB₃ are latched by the data latch circuits DL through the data bus lines ℓ_{13} and gate transistors 32, and read out externally through the data latch circuits DL.

The memory cells are provided for both right and left sides of the sense amp line, when selecting the left side memory cells, the right side memory cells are cut off by the cut gate transistors G₆ and G₇. Conversely, when selecting the right side memory cells, the left side memory cells are cut off by the cut gate transistors G₄ and G₅.

In Fig. 4, data bus lines ℓ_{12} and ℓ_{13} are provided at a wiring layer in the lateral direction, or the bit line direction. Namely, the bus lines ℓ_{12} , which are eight lines corresponding to eight bus lines of the data bus DB₂, are connected between a data latch circuit DL and the bus lines of the data bus DB₂ running along the left sense amplifier arrangement. Similarly, the bus lines ℓ_{13} , which are also eight lines corresponding to eight bus lines of the data bus DB₃, are connected between the data latch circuit DL and the bus lines of the data bus DB₃ running along the right sense amplifier arrangement. Note, the bus lines ℓ_{12} and the bus lines ℓ_{13} are commonly connected to the same data latch circuit DL through select gate transistors 31 and 32 which are controlled by a selector circuit 35, and both select gate transistors 31 and 32 are not switched ON at the same time. Therefore, the same data latch circuit DL can be used for both bus lines ℓ_{12} and ℓ_{13} . The data read out to the data latch circuit DL are output externally through a specific path (which is not shown in the drawings).

A wiring ℓ_{15} running in the lateral direction is used for another signal line, and a wiring ℓ_{11} running in the lateral direction is used for a column select line connected to the Y-decoder 20 which corresponds to the signal lines ℓ_3 and ℓ_4 shown in Fig. 1.

Figure 5 is a circuit diagram indicating a modification of the first embodiment of the semiconductor memory device according to the present invention. In Fig. 5, sense amplifier driving lines are provided at the wiring layer of the lateral direction as broad width wiring layers ℓ_{16} and ℓ_{17} . Note, the wiring layer ℓ_{16} is connected to the low potential power supply line Vss through a gate transistor G₁₁ and to the sense amplifier driving line ℓ_2 of the sense amplifier SA through a plurality of through-holes H. Similarly, the wiring layer ℓ_{17} is connected to the high potential power supply line Vcc through a gate transistor G₁₀ and to the sense amplifier driving line ℓ_1 of the sense am-

plifier SA through a plurality of through-holes H. In this modification of the first embodiment, the wiring layers ℓ_{16} and ℓ_{17} are formed with a broad width and connected to the sense amplifier driving lines ℓ_2 and ℓ_1 of both right and left sense amplifiers by the same wiring layers ℓ_{16} and ℓ_{17} . However, the wiring layers ℓ_{16} and ℓ_{17} can be formed as a plurality of wirings and connected to corresponding driving lines of each of the sense amplifier driving lines ℓ_2 and ℓ_1 , respectively.

As described above, in accordance with the modification of the first embodiment of the present invention, the power supply lines Vcc and Vss (wiring layers ℓ_{16} and ℓ_{17}) are provided over the memory cell area and the sense amplifier area (memory cell portion), and thus the power supply lines Vcc and Vss whose width are merely wide can be deleted from the neighboring area of the memory cell portion. Consequently, the occupancy area of the semiconductor memory device can be small.

Figure 6 is a block diagram indicating a layout of memory cell blocks and sense amp lines of a DRAM device. In Fig. 3, the sense amp lines are only described as two lines, but in a large capacity memory device such as a 16 M-bit DRAM device, the sense amp lines become plural. As shown in Fig. 6, in the 16 M-bit DRAM device sixteen cell blocks each having 1 M-bit capacity are arranged in parallel. Note, each cell block comprises 2 K (2048) sense amplifiers (sense amp line) and two 512 K cell blocks are provided on both sides of the sense amp line. In this case, the data latch circuit DL can be commonly used for the sense amp lines which are not operated at the same time by using selector 35 and the select gate transistors 31, 32 shown in Fig. 4. Note, sense amplifier driving lines ℓ_{12} , ℓ_{13} , and the other lines, which are running in the lateral direction and crossing the sense amp lines, extend to specific portions acrossing these cell blocks.

Figure 7 is a basic diagram indicating a second embodiment of a semiconductor memory device according to the present invention.

As shown in Fig. 7, the semiconductor memory device of the first embodiment comprises a plurality of word lines WL, a plurality of bit lines BL and \overline{BL} , a plurality of sense amplifiers SA, and data buses DB₂₁, DB₂₂ and DB₃₁, DB₃₂. The data buses DB₂₁, DB₂₂ and DB₃₁, DB₃₂ are provided along the word line direction (lengthwise direction) for outputting a potential of the bit lines BL and \overline{BL} amplified by the sense amplifiers SA to an external destination. Note, the data buses are divided into a plurality of groups DB₂₁, DB₂₂ and DB₃₁, DB₃₂ along the word line direction. Namely, the data bus DB₂ shown in Fig. 3 is divided into the data buses DB₂₁, DB₂₂, and the bus DB₃

shown in Fig. 3 is divided into the data buses DB₃₁, DB₃₂. The data buses DB₂₁ and DB₃₁ are connected to a first data latch circuit DL through first data bus lines ℓ_{12} and ℓ_{13} running along the bit line direction and switching circuit SW, similarly, the data buses DB₂₂ and DB₃₂ are connected to a second data latch circuit DL through second data bus lines ℓ_{12} and ℓ_{13} running along the bit line direction and switching circuit SW. The first and the second data bus lines ℓ_{12} and ℓ_{13} are provided above memory cells MC and the sense amplifiers SA crossing the data buses DB₂₁, DB₂₂ and DB₃₁, DB₃₂.

Furthermore, as shown in Fig. 7, sense amplifier driving lines ℓ_1 and ℓ_2 running in the word line direction (lengthwise direction) are connected to power supply lines Vcc and Vss at a plurality of connection portions by a plurality of wirings extending over the memory cell array and the sense amplifiers.

Figure 8 is a circuit diagram indicating the second embodiment of the semiconductor memory device according to the present invention. The semiconductor memory device of Fig. 8 is the same large capacity memory device of the 16 M-bit DRAM shown in Fig. 6. In Fig. 8, a sense amp line (which is constituted by 2 K (2048) sense amplifiers arranged as a line-shape in the lengthwise direction) are divided into two sense amp lines each having 1 K (1024) sense amplifiers. This semiconductor memory device is also a DRAM of a four-bit simultaneous read out type and eight data bus lines are required, but there are only four bus lines (two pairs) for each divided sense amp line.

In Fig. 8, lines ℓ_{12a} , ℓ_{13a} and ℓ_{12b} , ℓ_{13b} are connected to data latch circuits DL₁, DL₂ and DL₃, DL₄ through switching transistors SW which are controlled by a selector circuit 30, and latched data in each of the data latch circuits DL₁, DL₂, DL₃, and DL₄ are output externally through a specific path (which is not shown in the drawings). Note, when the left sense amp line operates, the right sense amp line does not operate. Conversely, when the right sense amp line operates, the left sense amp line does not operate. Therefore, the same data latch circuit DL₁, DL₂, DL₃, and DL₄ can be used for both left and right sense amp lines.

The sense amplifier driving lines ℓ_1 and ℓ_2 of both left and right sense amp lines are connected to the low potential power supply line Vss and the high potential power supply line Vcc through sense amplifier driving lines ℓ_{31} , ℓ_{32} and ℓ_{41} , ℓ_{42} running in the lateral direction and gate transistors G₁₁ and G₁₀, respectively. Namely, the sense amplifier driving line ℓ_1 is connected to the high potential power supply line Vcc through the sense amplifier driving lines ℓ_{32} and ℓ_{42} and the gate transistors G₁₀, and the sense amplifier driving line

ℓ_2 is connected to the low potential power supply line Vss through the sense amplifier driving lines ℓ_{31} and ℓ_{41} and the gate transistors G_{11} . Note, each one sense amplifier driving line ℓ_1 is connected to the power supply line Vcc by a plurality of (two) driving lines ℓ_{32} and ℓ_{42} , and each one sense amplifier driving line ℓ_2 is connected to the power supply line Vss by a plurality of (two) driving lines ℓ_{31} and ℓ_{41} , and a current in each of the sense amplifier driving lines ℓ_1 and ℓ_2 is divided and flown into both two driving lines ℓ_{32} , ℓ_{42} and ℓ_{31} , ℓ_{41} . Therefore, a width of each of the sense amplifier driving lines ℓ_1 and ℓ_2 can be made small, and an occupancy area of the sense amplifier driving lines ℓ_1 and ℓ_2 can be decreased.

As described above, the sense amplifier driving lines ℓ_{31} , ℓ_{32} and ℓ_{41} , ℓ_{42} running in the lateral direction are provided in plural, and the sense amplifier driving lines ℓ_1 and ℓ_2 running in the lengthwise direction are supplied with the power Vss and Vcc through the plural driving lines, and thus the width of each driving lines ℓ_1 and ℓ_2 can be small.

When the sense amp lines are divided into two sense amp lines along the lengthwise direction in the 16 M-bit DRAM device, the width of the data bus can be decreased to $384/2 = 192 \mu\text{m}$, and the width of the sense amplifier driving line can be decreased to $1280/2 = 640 \mu\text{m}$.

Figure 9 is a block circuit diagram indicating a part of the semiconductor memory device shown in Fig. 8, and a layout of various wirings in a lateral direction in one group consisting of sixteen sense amplifiers is described therein. In Fig. 9, references $SA_1 \sim SA_{16}$ denote sixteen sense amplifiers, and $BL_1 \sim BL_{16}$ denote sixteen pairs of word lines. Further, references C_1, C_2, \dots denote column select lines, G_{21}, G_{22}, \dots denote column select gate transistors, which are indicated by the reference ℓ_3 and G_2, G_3 in Fig. 8. Additionally, references DBa and DBb denote four data bus pairs DB_{21}, \dots .

Two pairs of bit lines are connected to the corresponding data bus pairs DBa and DBb by one of the column select lines C_1, C_2, \dots , and four-bit data are simultaneously read out or written by sixteen sense amp lines which are not shown. In this embodiment, the bit line pairs BL_1 and BL_3 are controlled and connected to the data bus pairs DBa and DBb by the column select line C_1 , the bit line pairs BL_2 and BL_4 are controlled and connected to the data bus pairs DBb and DBa by the column select line C_2 , and the others bit line pairs are also controlled and connected to the corresponding data bus pairs by the column select lines in the same manner as above.

When one lateral direction wiring (column select line) is running over one sense amplifier, sixteen lateral direction wirings can be provided over

sixteen sense amplifiers $SA_1 \sim SA_{16}$. Note, one column select line $C_1 \sim C_8$ processes two bit-line pairs $BL_1 \sim BL_{16}$ and eight column select lines are enough, and thus a space corresponding to eight wiring lines, which are provided over the sense amplifiers $SA_5 \sim SA_{12}$ in Fig. 9, can be kept. Namely, in this embodiment, the column select lines are provided at the upper portion by four lines $C_1 \sim C_4$ and at the lower portion by four lines $C_5 \sim C_8$. Therefore, the space corresponding to eight lines at the center portion remains, and the power supply lines Vss, Vcc, the other signal lines (for example, the line ℓ_{31} in Fig. 8), or the data bus DBc (for example, the line ℓ_{12a} , ℓ_{13a} , ℓ_{12b} , ℓ_{13b} in Fig. 8) can be provided for the eight remaining lines at the center portion.

As described above, in accordance with the second embodiment of the present invention, the width of the data buses and the sense amplifier driving lines running along the sense amp line (lengthwise direction) can be decreased, especially in a large capacity semiconductor memory device, and the occupancy area thereof can be extremely decreased.

Figure 10 is a circuit diagram indicating a third embodiment of a semiconductor memory device according to the present invention. In Fig. 10, all memory cells are divided into four blocks A~D in the bit line direction (lateral direction), and each block A~D is divided into four units (blocks) along the word line direction (lengthwise direction), for example, the block A is divided into units 1A, 1B, 1C and 1D. Note, each block A~D includes a sense amp line where a plurality of sense amplifiers are arranged as a line-shape in the lengthwise direction, and two memory cell lines (blocks) in the lengthwise direction each having a plurality of memory cells. The two memory cell blocks are provided on both sides of the sense amp line. In the practical use, however, the memory cells are not divided into only four blocks in each direction, but are divided into 32 or 64 blocks in each direction.

As shown in Fig. 10, in each block A~D, each of the sense amplifier driving lines L_n and L_p running along the lengthwise direction is divided into four wirings (sense amplifier driving lines) $L_{1n} \sim L_{4n}$ and $L_{1p} \sim L_{4p}$, respectively. The wirings $L_{1n} \sim L_{4n}$ are connected to the corresponding wirings (sense amplifier driving lines) $SAN_{1A} \sim SAN_{4A}$ running along the lateral direction, and the sense amplifier driving lines $L_{1p} \sim L_{4p}$ are connected to the corresponding wirings $SAP_{1A} \sim SAP_{4A}$ running along the lateral direction. Note, the wirings $SAN_{1A} \sim SAN_{4A}$ and $SAP_{1A} \sim SAP_{4A}$ are formed in a wiring layer which is another layer having the wirings $L_{1n} \sim L_{4n}$ and $L_{1p} \sim L_{4p}$, and thus the wirings $SAN_{1A} \sim SAN_{4A}$, $SAN_{1B} \sim SAN_{4B}$,

SAN1C~SAN4C, SAN1D~SAN4D and the wirings L1n~L4n and L1p~L4p can be formed the same as the circuit diagram shown in Fig. 10. For example, the wirings SAN1D~SAN4D for connecting between the sense amplifiers (SA) in the block D and the low potential power supply line Vss can be formed over the blocks A, B and C, and the wirings SAP1A~SAP4A for connecting between the sense amplifiers in the block A and the high potential power supply line Vcc can be formed over the blocks B, C and D. Note, the wirings L1n~L4n (Ln) and L1p~L4p (Lp) are formed over the sense amp line, and the occupancy area for the sense amp line is limited by the size of the wirings L1n~L4n (Ln) and L1p~L4p (Lp).

In the conventional semiconductor memory device, when the sense amplifier driving lines Ln and Lp are running along the word line direction (sense amp line direction) as shown in Fig. 2, all sense amplifiers in the sense amp line are driven by the same driving lines Ln and Lp. Note, the width of the driving lines Ln and Lp close to the power lines Vss and Vcc should be made large, as the currents flowing in all the sense amplifiers in the sense amp line are flown to the power lines Vss and Vcc through the driving lines Ln and Lp close to the power lines Vss and Vcc. However, in the present embodiment, the sense amplifier driving lines Ln and Lp in Fig. 2 are divided into four wirings L1n~L4n and L1p~L4p, and each of the wirings L1n~L4n and L1p~L4p is connected to the low potential power supply line Vss and the high potential power supply line Vcc running along the word line direction through the corresponding wirings SAN1A~SAN4A and SAP1A~SAP4A. Therefore, a width of each sense amplifier driving line L1n~L4n and L1p~L4p can be decreased by the number of its driving sense amplifiers. Namely, in the conventional art, all sense amplifiers in the sense amp line are driven by the same sense amplifier driving line (Ln, Lp), and thus a width of the sense amplifier driving line (Ln, Lp) becomes large in order to flow a sufficient current to the sense amplifiers connected thereto. Nevertheless, in the present embodiment, the sense amplifiers in each sense amp line are divided into four blocks (units 1A~1D), the sense amplifier driving line Ln and Lp are also divided into four wirings L1n~L4n and L1p~L4p, and these wirings L1n~L4n and L1p~L4p are supplied with the low and high voltage Vss and Vcc through corresponding wirings SAN1A~SAN4A and SAP1A~SAP4A. Therefore, in the present embodiment, the width of the sense amplifier driving lines L1n~L4n and L1p~L4p becomes small, and the occupancy area of the sense amp line over which the wirings L1n~L4n and L1p~L4p are formed becomes small.

Additionally, in the present embodiment, the

power supply lines Vss and Vcc formed in the circumference of the memory portion along the lateral direction (bit line direction) can be deleted by using power supply lines Vss and Vcc formed in the circumference of the memory portion along the lengthwise direction (word line direction, or sense amp line direction) and the wirings SAN1A~SAN4A and SAP1A~SAP4A running along the lateral direction. Note, the length of the memory cell portion in the lateral direction is longer than the length of the memory cell portion in the lengthwise direction and the wirings SAN1A~SAN4A and SAP1A~SAP4A are formed over the memory cell portion, so that the occupancy area for the power supply lines become small.

In Fig. 10, references Q₁~Q₁₆ denote sense amplifier driving transistors (gate transistors), and these transistors are normally switched OFF. When $\overline{\text{RAS}}$ signal is activated and an address for selecting a word line is defined, the word line which is discriminated is included in blocks A~D, and then one of four sense amplifier activation clocks SENA~SEND is generated. For example, when the word line in the block A are driven, the sense amplifier activation clock SENA is changed to a high level and the sense amplifier driving transistors Q₁, Q₅, Q₉, and Q₁₃ are switched ON, and then the sense amplifier driving lines SAN1A~SAN4A are connected to the low potential power supply line Vss, so that the sense amplifiers in the block A are only activated, and that the other sense amplifiers in the block B, C, and D are not activated. Note, when the sense amplifier activation clock SENA is changed, the corresponding activation clock SEPA is also changed and the sense amplifier driving transistors Q₁₇, Q₂₁, Q₂₅, and Q₂₉ are also switched ON, and then the sense amplifier driving lines SAP1A~SAP4A are connected to the high potential power supply line Vcc.

In the above descriptions, the width of one sense amplifier driving line SAN1A~SAN4A can be decreased in accordance with increasing the divided number thereof, and thus these sense amplifier driving lines can be formed in the same wiring layer where the data bus lines and the column select lines are formed.

Figure 11 is a sectional diagram indicating a part of the semiconductor memory device shown in Fig. 10. As shown in Fig. 10, a plurality of sense amplifier driving lines running along the word line direction Ln, Lp (L1n~L4n, L1p~L4p; ℓ_2, ℓ_1) are formed in a first wiring layer W₁, and a plurality of second sense amplifier driving lines running along the bit line direction SAN1A~SAN4A, ..., SAP1A~SAP4A, ...; $\ell_{31}, \ell_{41}, \ell_{32}, \ell_{42}$) are formed in a second wiring layer W₂. Note, these wiring layers W₁ and W₂ are provided above the memory cell portion including a plurality of mem-

ory cells and sense amplifiers.

Figure 12 is a sectional diagram indicating a part of the semiconductor memory device shown in Fig. 10.

In Fig. 12, references $Q_{41} \sim Q_{44}$ denote transistors constituting a sense amplifier (SA1), and references Q_{49} , Q_{50} denote gate transistors for selecting a column and gates of the gate transistors Q_{49} , Q_{50} are connected to an output CL1 of a column decoder provided at the end of the memory cell portion (memory cell array). The wiring CL1 is formed in the second aluminium wiring W_2 running along the bit line direction, or crossing direction of the word line. In Fig. 12, references $Q_{45} \sim Q_{48}$ denote switching transistors for a shared sense amplifier. Note, in the sense amplifier SA1, the sense amplifier driving lines L1n and L1p are running along the lengthwise direction and formed in the first aluminium wiring layer W_1 . Note, a sense amplifier SA2 is the same configuration of the sense amplifier SA1, and the sense amplifier SA2 is not required at the portion close to the sense amplifier SA1. As shown in Fig. 12, in an area of the sense amplifier SA2, the sense amplifier driving lines SAN1A and SAP1A for driving the sense amplifiers provided in the block A (unit 1A) are formed, and these driving lines SAN1A and SAP1A are formed in the second wiring layer W_2 and connected to the sense amplifier driving lines L1n and L1p, respectively. A reference SA3 denotes a sense amplifier (shared sense amplifier) in the same block A, where the other sense amplifier driving line SAN1B for driving the sense amplifiers provided in the block B (unit 1B) is formed, and this driving line SAN1B is formed in the second wiring layer W_2 above the sense amplifier SA3 through an insulation layer.

As described above, the sense amplifier driving lines SAN1A~SAN4A,..., SAP1A~SAP4A, ... running along the lateral direction are formed in the second wiring layer W_2 above the sense amplifier (SA), and thus the sense amplifier driving lines can be provided over the memory cell array, when the memory cell array is divided into a plurality of blocks in the bit line direction.

Figure 13 is a block circuit diagram indicating a modification of the third embodiment of the semiconductor memory device according to the present invention.

In Fig. 13, the driving transistors for the sense amplifiers are divided into four blocks in the word line direction, and each driving transistor in the divided block is independently controlled by a sense amplifier activation clock. Namely, for example, the sense amplifier activation clock SENA for controlling the sense amplifier driving transistors Q_1 , Q_5 , Q_9 , and Q_{13} shown in Fig. 10 is divided into four sense amplifier activation clocks

SEN1A~SEN4A. Note, for example, the sense amplifier driving transistor Q_1 is controlled by the sense amplifier activation clock SEN1A, and the sense amplifier driving transistor Q_5 is controlled by the sense amplifier activation clock SEN2A. Similarly, for example, the sense amplifier activation clock SEPA for controlling the sense amplifier driving transistors Q_{17} , Q_{21} , Q_{25} , and Q_{29} shown in Fig. 10 is divided into four sense amplifier activation clocks SEP1A~SEP4A.

By dividing the sense amplifier activation clock dependently, for example, when accessing a first block (unit) 1A in the block A, in the semiconductor memory device shown in Fig. 10, the sense amplifier activation clock SENA is changed to a high level. However, in this semiconductor memory device shown in Fig. 13, the voltage values in the activation clock SEN1A for reading out operation and the activation clocks SEN2A~SEN4A for only a refreshing operation are different. Namely, the voltage value of the activation clock SEN1A for a reading out operation is higher than that of the activation clocks for only a refreshing operation SEN2A~SEN4A. Note, the unit 1A is powerfully driven by the activation clock SEN1A, or the data bus for the unit 1A is driven by a low impedance (an internal resistance of the sense amplifiers in the unit 1A is a low value), so that an operation speed in the circuit for reading out data from the memory cell becomes high. Furthermore, the other units 2A~4A, where only a refresh operation is carried out, are weakly driven compared with the unit 1A, the operation in the units 2A~4A becomes slow. Therefore, a generated current at the beginning of the operations in the units 1A~4A can be small. In this embodiment, there are only four divided units (blocks), but practically, there may be 32 divided units. Namely, when all sense amplifiers are divided into 32 blocks, only 1/32 of all the blocks is required for a high speed operation (read out operation), and the other 31/32 blocks only carry out a refresh operation of the memory cell. Note, the average current, or the total current flowing in all the sense amplifiers is not changed, but the timing of current flowing in the sense amplifier for a reading out operation and the other sense amplifiers for only a refresh operation can be different, so that an internal noise and erroneous operation in the semiconductor memory device can be decreased.

Figure 14 is a diagram indicating a timing chart for explaining an operation of a preferable sense amplifier for the semiconductor memory device shown in Fig. 13.

In Fig. 14, when changing a row address strobe \overline{RAS} clock to a low level, a row address is fetched into a chip (semiconductor memory device) and a word line corresponding to the row address is

selected, and each of the sense amplifier activation clocks SEN1A~ SEN4A is changed to a high level. All selected sense amplifiers in the block A begin to operate at the same time by the sense amplifier activation clocks SEN1A~ SEN4A. Note, a driving current flowing in each of the sense amplifiers is small and the operation speed thereof is slow, as all sense amplifiers in the block A are driven by approximately the same current value. The reason why the current value flowing in each of the sense amplifiers is approximately determined at the same value, is that a gate voltage of each sense amplifier driving transistor is limited to about half the value of the power supply voltage and each driving transistor begins to operate in a range similar to pentode characteristics of a vacuum tube having constant-current characteristics.

After changing the $\overline{\text{RAS}}$ clock to the low level and after about 20 nsec.~30 nsec., a column address strobe $\overline{\text{CAS}}$ clock is changed to a low level, so that a column address is fetched into the chip. In this case, an attribute block of the accessing column can be recognized, and thus a voltage value of the operation and the sense amplifier activation clock SEN1A, which is supplied to the gate of the sense amplifier driving transistor for driving or selecting, is determined to a higher level than that of the other clocks SEN2A~ SEN4A which is supplied to the gate of the sense amplifier driving transistor for only refreshing and nonselecting. This selection operation is carried out by decoding a part of the column address. For example, when there are four divided blocks are four, the two bits of the column address are decoded, and when there are 32 divided blocks, the five bits of the column address are decoded, as 32 is indicated by 2^5 . Therefore, the sense amplifier in only one unit (block) 1A is driven by a high speed operation. Note, an amplitude of the bit line in the unit 1A is larger or higher than that of the other units 2A~4A. Further, the operation speed of selecting block is higher than that of the column decoder, as a bit number for decoding in the column decoder is more than a decoded bit number for selecting a block.

As described above, the sense amplifier in the unit 1A powerfully drives the column switch (Q_{49} and Q_{50} in Fig. 12) corresponding to the accessing column, and the sense amplifier powerfully drives the data bus lines, so that the circuits from a memory cell array to a data output amplifier can be driven first. On the other hand, the sense amplifiers in nonselected units 2A~4A are slowly (weakly) driven, and thus the current flowing in the sense amplifiers is not large at the beginning of the operations. Note, in the nonselected units 2A~4A, only a refresh operation is carried out therein until the RAS-cycle being completed. Concretely, the

sense amplifiers in the nonselected units are adequate for carrying out the amplifying operation during a long time of 40 nsec.~50 nsec. In this embodiment, the sense amplifier flowing current is not flown at the beginning of the operation, but is flown on average.

Figure 15A is a circuit diagram indicating an example of a driving signal generation circuit for a sense amplifier, and Fig. 15B is a diagram indicating a timing chart explaining an operation of the driving signal generation circuit shown in Fig. 15A.

As shown in Figs. 15A and 15B, an $\overline{\text{SE}}$ clock is the sense amplifier driving signal and is normally at a high level (V_{cc}), which is generated by using the $\overline{\text{RAS}}$ clock. A transistor Q_{100} is switched ON by the $\overline{\text{SE}}$ clock, and the clock SEN1A is generated at a specific level lower by the threshold values of the transistor Q_{101} , Q_{102} than the V_{cc} level, and thus the sense amplifier is weakly (slowly) driven. The column address is decoded and an access block (selected block) is recognized, a block selection signal BS1 in the access block is changed to the V_{cc} level, and an output of a NAND gate G1 is changed to a low level (V_{ss}). Therefore, a transistor Q_{104} is switched ON, the clock SEN1A is changed to the V_{cc} level, and thus the sense amplifier in the unit 1A is highly (powerfully) driven. In the blocks 2A~4A where only a refresh operation is carried out, the block selection signal is maintained at the V_{ss} level, and thus an operation speed of the transistors corresponding to the transistor Q_{104} is maintained to be slow.

Figure 16A is a circuit diagram indicating the other example of a driving signal generation circuit of a sense amplifier, and Fig. 16B is a diagram indicating a timing chart explaining an operation of the driving signal generation circuit shown in Fig. 16A.

As described above with reference to Figs. 15A and 15B, the operation speed of the selected sense amplifier can be different from that of the nonselected sense amplifiers by varying the gate voltages of the driving transistors. Nevertheless, in Figs. 16A and 16B, the sense amplifier driving transistor is constituted by two different size transistors. Namely, the sense amplifier can be driven by both large size transistors and small size transistors. Note, the large size transistors are controlled by the sense amplifier driving clock SEN1AA (and SEP1AA), and the small size transistors are controlled by the sense amplifier driving clock SEN1A (and SEP1A). Note, in this driving signal generation circuit, at the beginning of the operation, the sense amplifiers in all units 1A~4A are driven by the small size transistors by receiving the driving clock SEN1A, after outputting the block select signal, the sense amplifier corresponding the selected unit 1A is driven by the large size transis-

tors by receiving the driving clock SEN1AA.

Figure 17 is a diagram indicating a timing chart for explaining an operation of the semiconductor memory device of a Pseudo Static type.

As shown in Fig. 17, in the Pseudo Static type DRAM device, an address multiplex operation is not carried out when a \overline{CS} clock corresponding to the \overline{RAS} clock changes to a low level, and addresses of both row side and column side are fetched into the chip. Note, in the Pseudo Static type DRAM the sense amplifiers can be divided into a high speed operation unit and low speed operation units where only refresh operations are carried out at the beginning of the operations, as a accessing column block (selected column block) is defined at the beginning of the operations. The other operations are the same as in Fig. 14.

As described above, according to the third embodiment of the present invention, the width of one sense amplifier driving lines can be decreased in accordance with increasing the divided number thereof, and thus the width of the sense amplifier driving lines, or the occupancy area of the sense amp line, running along the word line direction, can be decreased. Furthermore, the sense amplifier driving lines can be formed in the same wiring layer where the data bus lines and the column select lines are formed, and thus the occupancy area of the semiconductor memory device can be decreased. Additionally, by dividing the sense amplifier activation clocks dependently, the timing of current flowing in the sense amplifier for a reading out operation and the other sense amplifiers for only a refreshing operation can be different, so that an internal noise and erroneous operation in the semiconductor memory device can be decreased.

Incidentally, the capacity of DRAM devices has become large, and a memory cell of the DRAM is constituted by a solid structure of a three dimensional stacked capacitor cell. This stacked capacitor cell is useful for reducing an occupancy area of the memory cell without decreasing the capacitance thereof. In the circumference of the memory cell portion, a plurality of peripheral circuits, for example, a sense amplifier, a bit line driver, a row decoder, a column decoder, and the like, are provided. Note, these peripheral circuits are constituted by normal semiconductor elements whose height corresponds to a single layer, the memory cell is constituted by the three dimensional stacked capacitor cell whose height corresponds to a plurality of layers, and thus an excessive difference is caused at the border portion between the memory cell portion and the peripheral circuit portion.

Figure 18 is a sectional diagram indicating an aluminium wiring between a memory cell element and a peripheral circuit element according to a related art. Note, this aluminium wiring may be

used as the data bus lines or sense amplifier driving lines running along the lateral direction (bit line direction) formed in the wiring layers W_1 or W_2 in Fig. 11.

In Fig. 18, reference numeral 1 denotes a memory cell element, 2 denotes a peripheral circuit element, 3 denotes a p-type silicon substrate, 4 denotes field insulation film, and 5 denotes a stacked capacitor. Note, reference numeral 6 denotes a peripheral circuit wiring of an aluminium wiring which is not only used as the data bus lines or sense amplifier driving lines running along the lateral direction, but also a wiring (peripheral circuit wiring) for connecting the peripheral circuit element 2 to another peripheral circuit element (not shown).

As shown in Fig. 18, in the conventional semiconductor memory device, a large level difference is caused at the border portion between the memory cell portion and the peripheral circuit portion. This level difference between the memory cell portion and the peripheral circuit portion cannot be included in a depth of focus of a exposure system. Therefore, the aluminium wirings cannot be freely formed over the memory cell portion and peripheral circuit portion with high accuracy, and thus an occupancy area of the DRAM device cannot be decreased.

Figure 19 is a sectional diagram indicating an aluminium wiring between a memory cell element and a peripheral circuit element according to the present invention. In Fig. 19, reference numeral 1 denotes a memory cell element, 2 denotes a peripheral circuit element, 3 denotes a p-type silicon substrate, 4 denotes a field insulation film, 5 (5C) denotes a stacked capacitor, 6 denotes an aluminium wiring (data bus line, sense amplifier driving line, peripheral circuit wiring), 5T denotes a memory cell transistor, and 7 denotes a connection conductor of tungsten (W). Concretely, for example, when the memory cell element 1 is formed as 5000 Å and the connection conductor 7 is formed as 3000 Å onto the peripheral circuit element 2, the level difference between the memory cell portion and the peripheral circuit portion becomes 2000 Å, and the level difference can be included in a depth of focus of an exposure system. Therefore, the aluminium wirings can be freely formed over the memory cell portion and peripheral circuit portion with high accuracy, and thus an occupancy area of the DRAM device can be decreased. Namely, an occupancy area of the wirings can be decreased by forming the wirings over the memory cell portion and peripheral circuit portion, as described above with reference to Figs. 3 to 10, and thus large scale integration of the DRAM device can be provided.

Figures 20A to 20G are sectional diagrams for explaining a method of forming the aluminium wir-

ing between the memory cell element and the peripheral circuit element shown in Fig. 19.

First, as shown in Fig. 20A, a field insulation film 4 is formed on a p-type silicon substrate 3, and a gate electrode of a first polycrystal silicon film P₁ (whose thickness is about 100 Å) is formed on a silicon substrate 3 through a gate insulation film 11 (whose thickness is about 100 Å). Next, a source region S and a drain region D are formed by injecting arsenic ions into the silicon substrate 3 using the gate electrode and the field insulation film 4 as a mask. Furthermore, a silicon dioxide (SiO₂) film 12 is formed over the silicon substrate 3, contact holes are opened over the source region S, and a bit line of a second polycrystal silicon film P₂ coated by tungsten silicide is formed over the contact holes.

Next, as shown in Fig. 20B, a Si₃N₄ (silicon nitride) film 13 (whose thickness is about 500 Å) is formed over the SiO₂ film 12 and the second polycrystal silicon film P₂, or the silicon substrate 3, and then four SiO₂ films 14 and three polycrystal silicon films 15 are mutually formed. Furthermore, a hole for forming a contact portion of a stacked capacitor is opened through the SiO₂ films 14, the polycrystal silicon films 15, and the Si₃N₄ film 13 to the surface of the drain region D by using a lithography method, and a polycrystal silicon film 16 (whose thickness is about 1000 Å) is formed thereover, so that a tree-shape stacked capacitor is formed. Note, a total thickness from the surface of the substrate 3 to the top surface layer of the polycrystal silicon film 16, except for the Si₃N₄ film 13, is about 5000 Å.

Furthermore, as shown in Fig. 20C, in the area without the stacked capacitor portion, the polycrystal silicon films 16, 15 and the SiO₂ films 14 except for the lowest SiO₂ film are removed by using the lithography method, so that the tree-shape stacked capacitor is formed. Next, as shown in Fig. 20D, in the area of the stacked capacitor portion, the SiO₂ films 14 provided between the polycrystal silicon films 16, 15 are removed by an etching method by immersion into a hydrofluoric acid solution, so that the tree-shape of polycrystal silicon films 16, 15 remain. This tree-shape of polycrystal silicon films 16, 15 is defined as a third polycrystal silicon film P₃. Note, in the manufacturing processes of the stacked capacitor, the Si₃N₄ film 13 is used to stop the etching process at the surface of the Si₃N₄ film 13.

Next, as shown in Fig. 20E, a dielectric film (indicated by thick line) is formed onto the surface of the third polycrystal silicon film P₃ (tree-shape of polycrystal silicon films 16, 15) by using a thermal oxidation method, and then a fourth polycrystal silicon film P₄ (whose thickness is about 1000 Å) is formed thereover. Furthermore, in the area with-

out the stacked capacitor portion, the fourth polycrystal silicon film P₄ is removed, and the remaining fourth polycrystal silicon film P₄ at the stacked capacitor portion becomes a cell plate. As described above, the stacked capacitor 5 is formed, and then a SiO₂ film 17 (whose thickness is about 1000 Å) is formed over the stacked capacitor 5.

With reference to Fig. 20F, the main portions of the memory cell element 1 and the peripheral circuit element 2 are almost all formed, and next, contact holes are opened at the peripheral circuit element 2 through the SiO₂ film 17, the Si₃N₄ film 13 and the SiO₂ film 12 to the electrode portions. Furthermore, a tungsten (W) film 7 (whose thickness is about 3000 Å) is formed by using a chemical vapor deposition (CVD) method, and then the tungsten film 7 is patterned as a connection conductor by using the lithography method, so that the height of the connection electrodes becomes high.

Finally, as shown in Fig. 20G, a phospho-silicate glass (PSG) film 18 formed onto the SiO₂ film 17 and the tungsten film 7, and then an aluminium wiring 6 is formed over the memory cell element 2, so that a data bus line, a sense amplifier driving line, or a peripheral circuit wiring can be formed. Namely, the aluminium wiring 6 is connected to the drain region D of the peripheral circuit element 2 through the connection conductor 7 of the tungsten film, so that the level difference between the memory cell portion and the peripheral circuit portion becomes small. Note, the level difference between the memory cell portion and the peripheral circuit portion can be included in a depth of focus of a exposure system, and thus the aluminium wirings can be freely formed over the memory cell portion and peripheral circuit portion with high accuracy. Consequently, an occupancy area of the wirings can be decreased by forming the wirings over the memory cell portion and the peripheral circuit portion, and thus large scale integration of the DRAM can be provided.

In the semiconductor memory device of the fourth embodiment of the present invention, the connection conductor 7 is not only limited to the tungsten film, but the connection conductor 7 can be made of polycrystal silicon, tungsten silicide (WSi₂), and the like.

Claims

1. A semiconductor memory device comprising:
 - a plurality of word lines (WL);
 - a plurality of bit lines (BL, \overline{BL}) formed crossing said word lines (WL);
 - a plurality of memory cells (MC), each connected between said one word line (WL) and said one bit line (BL, \overline{BL});
 - a plurality of sense amplifiers (SA), ar-

- ranged along the word line direction (WL);
 a first power supply line (Vss);
 a second power supply line (Vcc);
 a plurality of first sense amplifier driving lines ($l_2, l_1 : L_n, L_p$), connected to said sense amplifiers (SA) and formed in a first wiring layer (W_1); and
 a plurality of second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42} : SAN, SAP$), each connected between said corresponding first sense amplifier driving line ($l_2, l_1 : L_n, L_p$) and one of said first and second power supply lines (Vss, Vcc), and formed in a second wiring layer (W_2).
2. A semiconductor memory device as claimed in claim 1, wherein said first sense amplifier driving lines ($l_2, l_1 : L_n, L_p$) are formed along the word line direction (WL), and said second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42} : SAN, SAP$) are formed along the bit line direction (BL).
 3. A semiconductor memory device as claimed in claim 1, wherein said first sense amplifier driving lines ($l_2, l_1 : L_n, L_p$) are connected to said first and second power supply line (Vss, Vcc) at a plurality of portions through a plurality of said second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42} : SAN, SAP$).
 4. A semiconductor memory device as claimed in any claim, wherein said sense amplifiers (SA) and said memory cells (MC) are divided into a plurality of blocks ($M_0, M_1; A, B, C, D$).
 5. A semiconductor memory device as claimed in claim 4, wherein each of said second sense amplifier driving lines ($l_{31}, l_{41}; l_{32}, l_{42}$) are connected to one of said first and second power supply lines (Vss, Vcc) through a gate transistor (G_{11}, G_{10}), so that one of said divided blocks (M_0, M_1) is selected.
 6. A semiconductor memory device as claimed in claim 4, wherein said sense amplifiers (SA) are arranged as a sense amplifier line of a line-shaped along the word line direction (WL), and said memory cells (MC) are divided into two groups provided for both sides of said sense amplifier line, in each of said blocks ($M_0, M_1; A, B, C, D$).
 7. A semiconductor memory device as claimed in claim 4, wherein each of said blocks (A, B, C, D) is divided into a plurality of units (1A,2A,3A,4A, 1B,2B,3B,4B, 1C,2C,3C,4C, 1D,2D,3D,4D).
 8. A semiconductor memory device as claimed in claim 7, wherein each of said first sense amplifier driving lines (L_n, L_p) is divided into a plurality of first unit sense amplifier driving lines ($L_{1n}, L_{2n}, L_{3n}, L_{4n}, L_{1p}, L_{2p}, L_{3p}, L_{4p}$) corresponding to said units (1A,2A,3A,4A, 1B,2B,3B,4B, 1C,2C,3C,4C, 1D,2D,3D,4D), each of said second sense amplifier driving lines (SAN, SAP) is divided into a plurality of second unit sense amplifier driving lines (SAN1A, SAN2A, SAN3A, SAN4A, SAN1B, SAN2B, SAN3B, SAN4B, SAN1C, SAN2C, SAN3C, SAN4C, SAN1D, SAN2D, SAN3D, SAN4D, SAP1A, SAP2A, SAP3A, SAP4A, SAP1B, SAP2B, SAP3B, SAP4B, SAP1C, SAP2C, SAP3C, SAP4C, SAP1D, SAP2D, SAP3D, SAP4D) connected to said corresponding first unit sense amplifier driving lines ($L_{1n}, L_{2n}, L_{3n}, L_{4n}, L_{1p}, L_{2p}, L_{3p}, L_{4p}$).
 9. A semiconductor memory device as claimed in claim 8, wherein each of said second unit sense amplifier driving lines (SAN1A, SAN2A, SAN3A, SAN4A, ..., SAP1A, SAP2A, SAP3A, SAP4A, ...) is connected to said first and second power supply lines (Vss, Vcc) through a gate transistor ($Q_1, Q_5, Q_9, Q_{13}, \dots, Q_{17}, Q_{21}, Q_{25}, Q_{29}, \dots$).
 10. A semiconductor memory device as claimed in claim 9, wherein said gate transistors ($Q_1, Q_5, Q_9, Q_{13}, \dots, Q_{17}, Q_{21}, Q_{25}, Q_{29}, \dots$) connected to said corresponding second unit sense amplifier driving lines (SAN1A, SAN2A, SAN3A, SAN4A, ..., SAP1A, SAP2A, SAP3A, SAP4A, ...) in the same divided block (A, B, C, D) are controlled by the same control signal (SENA, SEPA), so that one of said divided blocks (A, B, C, D) is selected and the units (1A,2A,3A,4A,...) in said selected block (A) are selected at the same timing.
 11. A semiconductor memory device as claimed in claim 9, wherein said gate transistors ($Q_1, Q_5, Q_9, Q_{13}, \dots, Q_{17}, Q_{21}, Q_{25}, Q_{29}, \dots$) connected to said corresponding second unit sense amplifier driving lines (SAN1A, SAN2A, SAN3A, SAN4A, ..., SAP1A, SAP2A, SAP3A, SAP4A, ...) in the same divided block (A, B, C, D) are controlled by one read out signal (SEN1A, SEP1A) and the other refresh signals (SEN2A, SEN3A, SEN4A, SEP2A, SEP3A, SEP4A), so that one unit (1A) including a memory cell for reading out in a selected block (A) is read out at high speed and the other units (1B,1C,1D) in said selected

block (A) are only refreshed at different timing than the read out operation.

12. A semiconductor memory device as claimed in claim 11, wherein a voltage value of said read out signal (SEN1A) is higher than that of said refresh signal (SEN2A, SEN3A, SEN4A), so that said read-out operation unit (1A) is speedily driven and said refresh operation unit (2A, 3A, 4A) are slowly driven.
13. A semiconductor memory device as claimed in any claim wherein said semiconductor memory device further comprises data bus lines (DB₂, DB₃; ℓ_{12} , ℓ_{13}) and a data latch circuit (DL), said data bus lines (DB₂, DB₃; ℓ_{12} , ℓ_{13}) are connected between said sense amplifiers (SA) and said data latch circuit (DL).
14. A semiconductor memory device as claimed in claim 13, wherein said data bus lines comprise first data bus lines (DB₂, DB₃) connected to said sense amplifiers (SA) and formed in said first wiring layer (W₁) along the word line direction (WL), and second data bus lines (ℓ_{12} , ℓ_{13}) connected between said corresponding first bus lines (DB₂, DB₃) and said data latch circuit (DL) and formed in said second wiring layer (W₂) along the bit line direction (BL).
15. A semiconductor memory device as claimed in claim 13, wherein said second data bus lines (ℓ_{12} , ℓ_{13}) are connected to a plurality of said first data bus lines (DB₂, DB₃) and said data latch circuit (DL) through gate transistors (31, 32), said gate transistors (31, 32) are controlled by a selector (35), so that one of said first data bus lines (DB₂, DB₃) is selected and connected to said data latch circuit (DL).
16. A semiconductor memory device as claimed in claim 13, wherein said first data bus lines (DB₂, DB₃) are divided into a plurality of group bus lines (DB₂₁, DB₂₂; DB₃₁, DB₃₂), said second data bus lines (ℓ_{12} , ℓ_{13}) and said data latch circuit (DL) are provided in accordance with the divided group bus lines (DB₂₁, DB₂₂; DB₃₁, DB₃₂), and said second data bus lines (ℓ_{12} , ℓ_{13}) are connected to said corresponding group bus lines (DB₂₁, DB₂₂; DB₃₁, DB₃₂) and said data latch circuit (DL) through a switching circuit (SW), so that each one of said group bus lines (DB₂₁, DB₂₂; DB₃₁, DB₃₂) is selected and connected to said each data latch circuit (DL).
17. A semiconductor memory device as claimed in any claim wherein said semiconductor memory

device comprises further signal lines formed in said first wiring layer (W₁) and said second wiring layer (W₂).

18. A semiconductor memory device as claimed in claim 1, wherein said second sense amplifier driving lines (6: ℓ_{31} , ℓ_{41} ; ℓ_{32} , ℓ_{42} ; SAN, SAP) are formed between a memory cell portion and a peripheral circuit portion, and said second sense amplifier driving lines (6: ℓ_{31} , ℓ_{41} ; ℓ_{32} , ℓ_{42} ; SAN, SAP) are connected to said one of said first and second power supply lines (Vss, Vcc) through a connection conductor (7).
19. A semiconductor memory device as claimed in any claim wherein each of said memory cell (MC) comprises a stacked capacitor (5C) and a memory cell transistor (5T).
20. A semiconductor memory device as claimed in any claim wherein said first wiring layer (W₁) and said second wiring layer (W₂) provided above said memory cells (MC) and said sense amplifiers (SA) are used to form data bus lines (DB₂, DB₃; ℓ_{12} , ℓ_{13}), sense amplifier driving lines (ℓ_{21} , ℓ_{11} ; Ln, Lp: ℓ_{31} , ℓ_{41} ; ℓ_{32} , ℓ_{42} ; SAN, SAP), the other signal lines, and power supply lines (Vss, Vcc).
21. A semiconductor memory device comprising:
 - a plurality of word lines (WL);
 - a plurality of bit lines (BL, BL) formed crossing said word lines (WL);
 - a plurality of memory cells (MC), each connected between said one word line (WL) and said one bit line (BL, BL);
 - a plurality of sense amplifiers (SA), each connected to a pair of said bit lines (BL, BL);
 - a first power supply line (Vss);
 - a second power supply line (Vcc);and
 - a pair of sense amplifier driving layers (ℓ_{16} , ℓ_{17}), connected between said first and second power supply lines (Vss, Vcc) and each of said sense amplifiers (SA), and formed in a wiring layer over said memory cells (MC) and said sense amplifiers (SA).

Fig. 1A

LATERAL DIRECTION
(BIT LINE DIRECTION)

Fig.1
Fig.1A Fig.1B

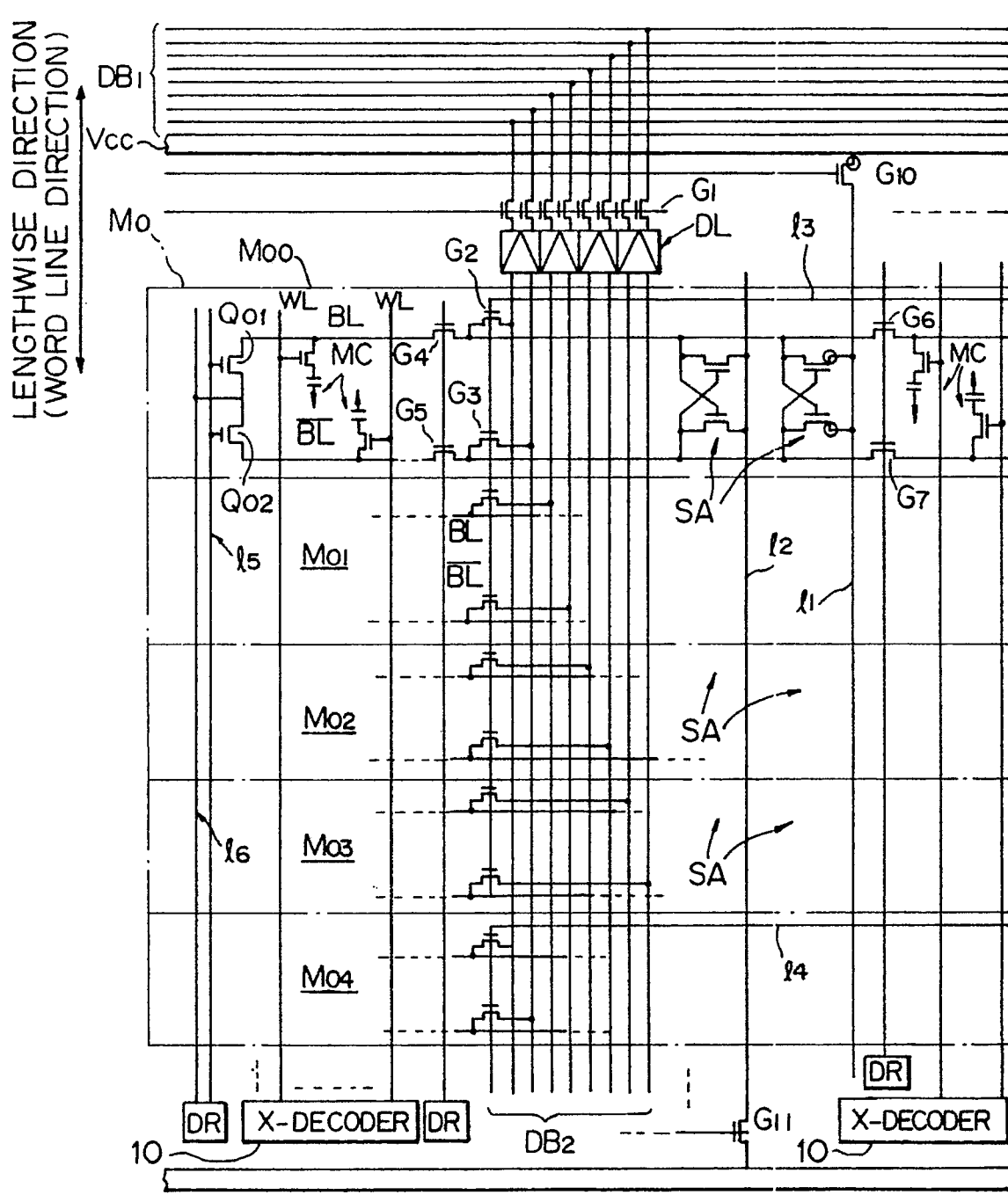


Fig. 1B

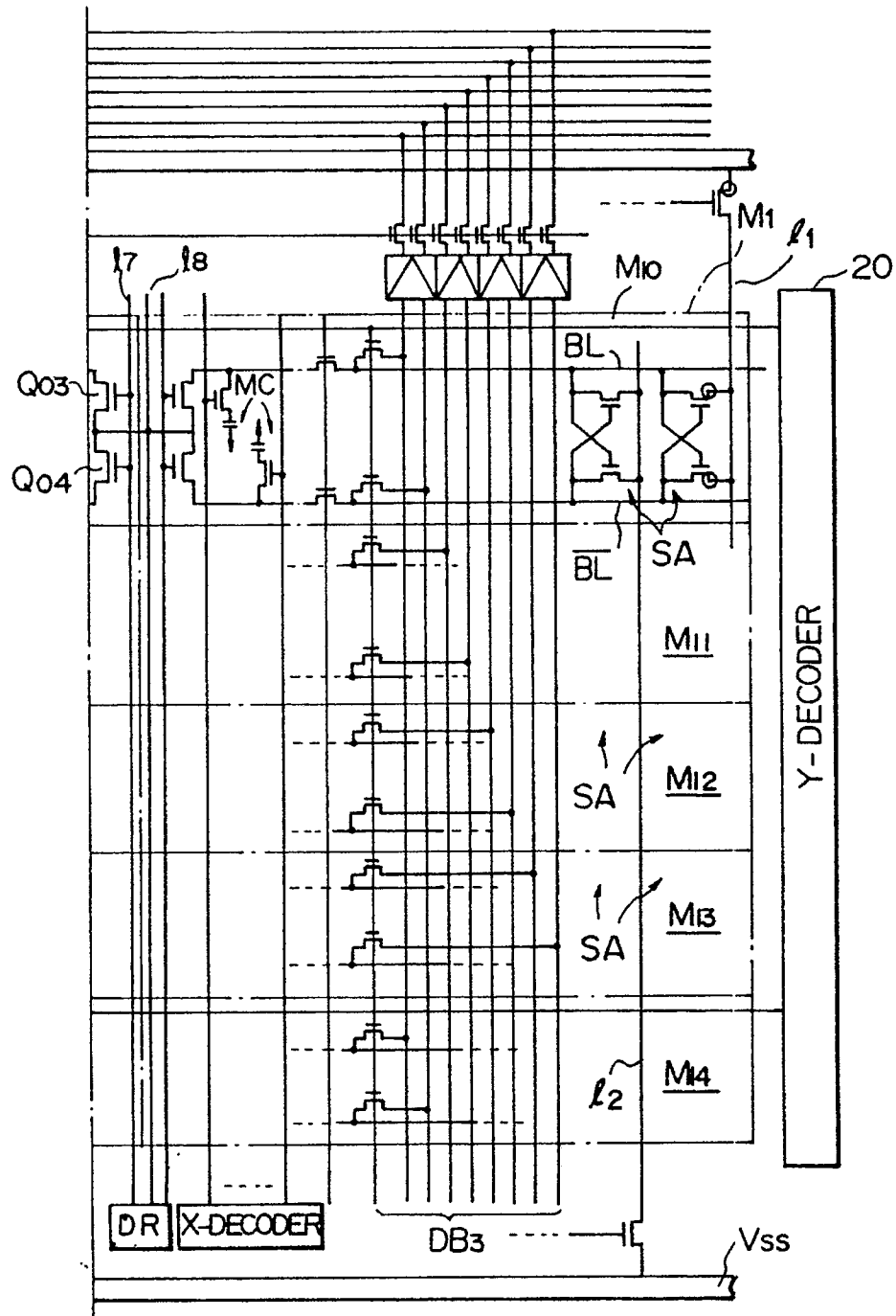


Fig.2A

Fig.2

Fig.2A Fig.2B

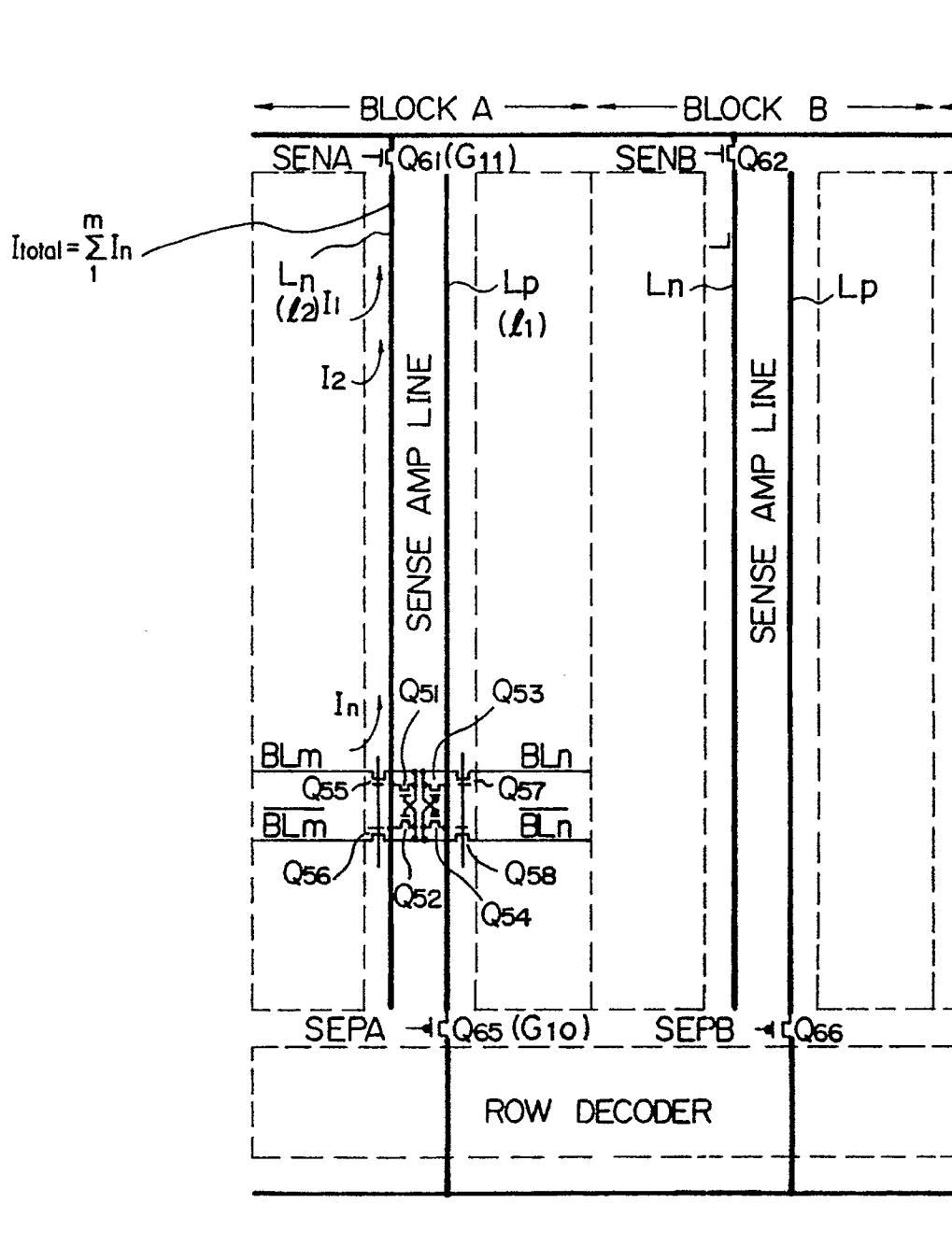


Fig.2B

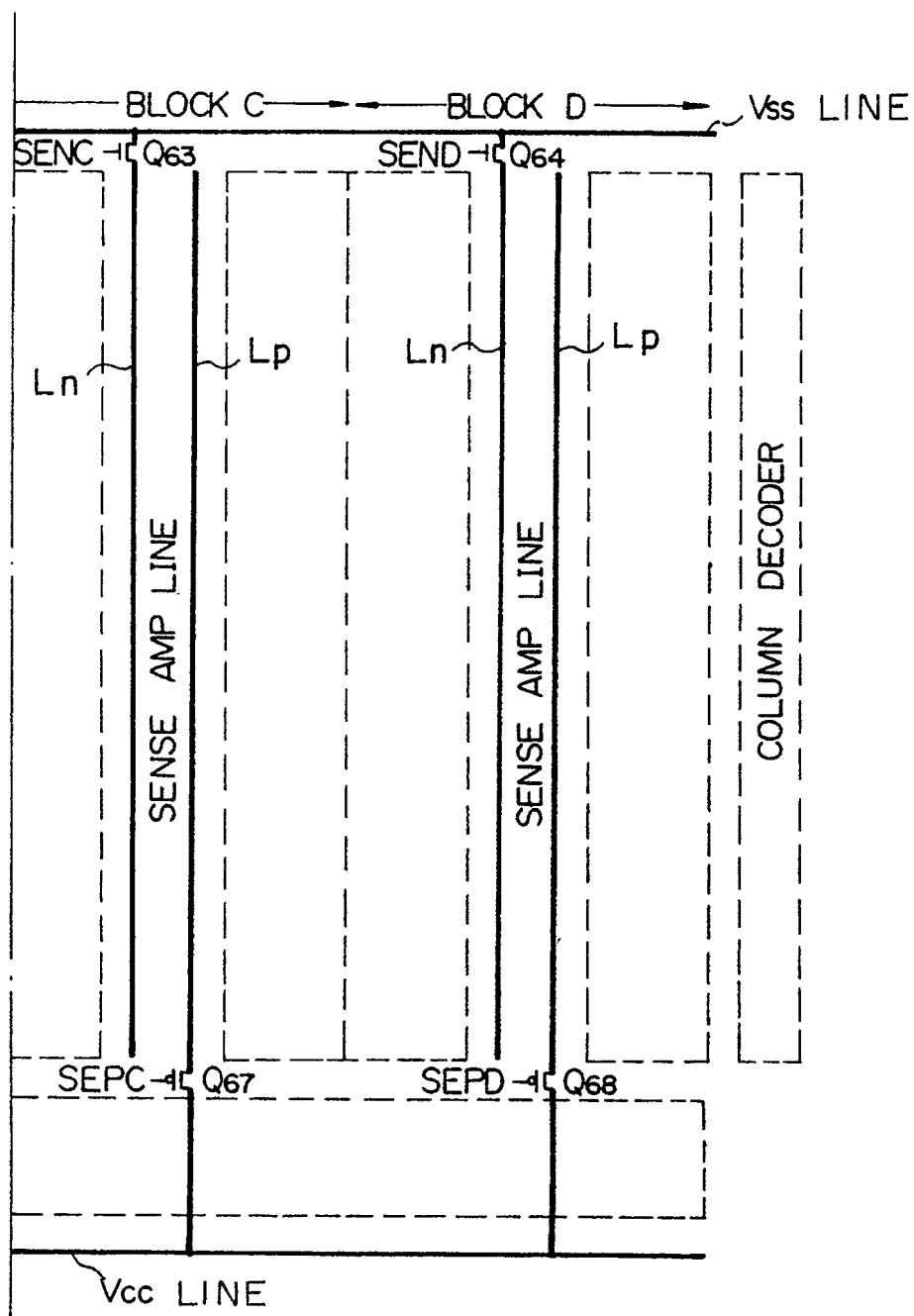


Fig. 3

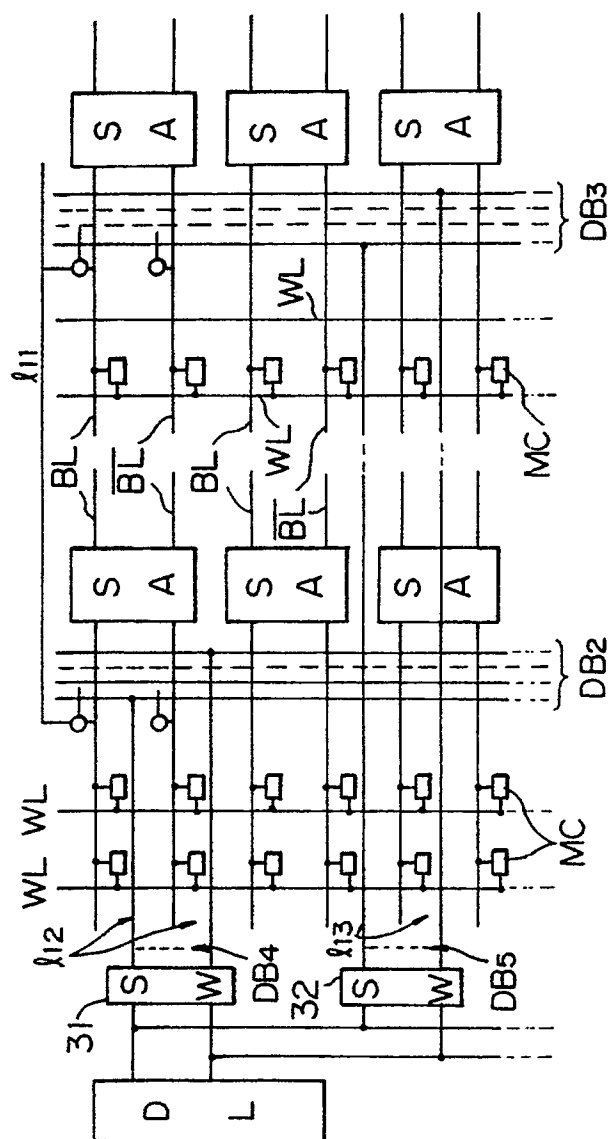


Fig.4A

Fig.4

Fig.4A Fig.4B

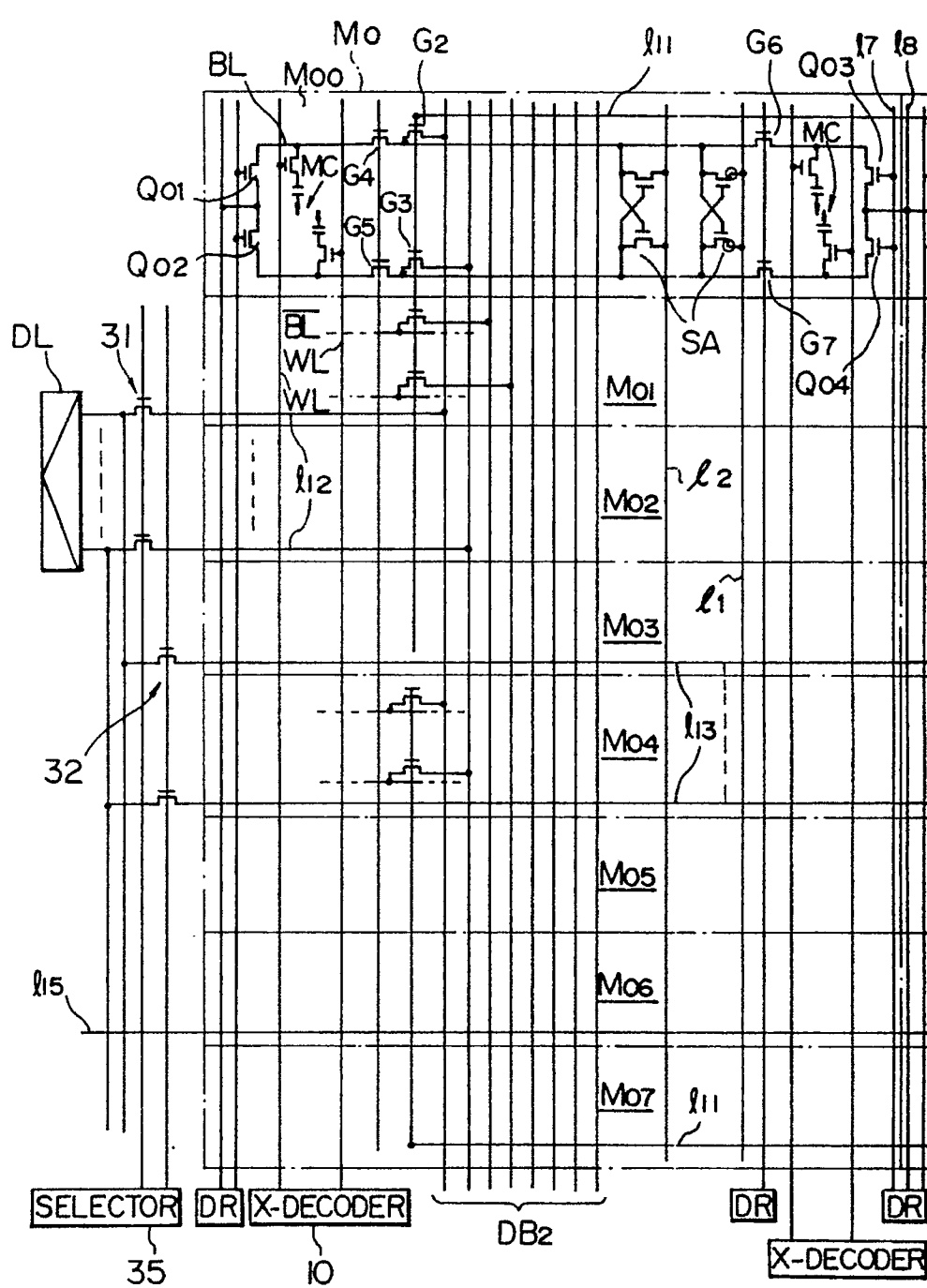


Fig.4B

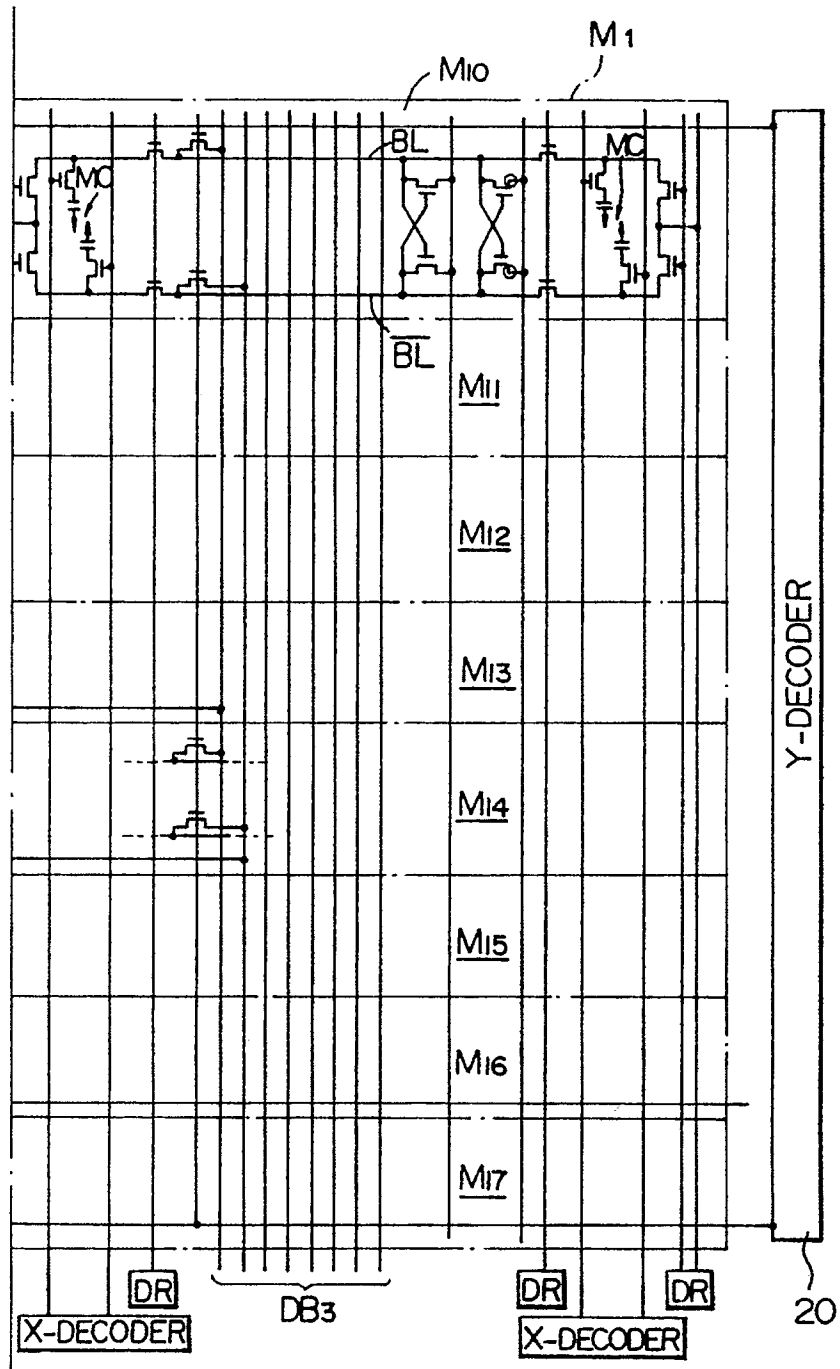


Fig. 5A

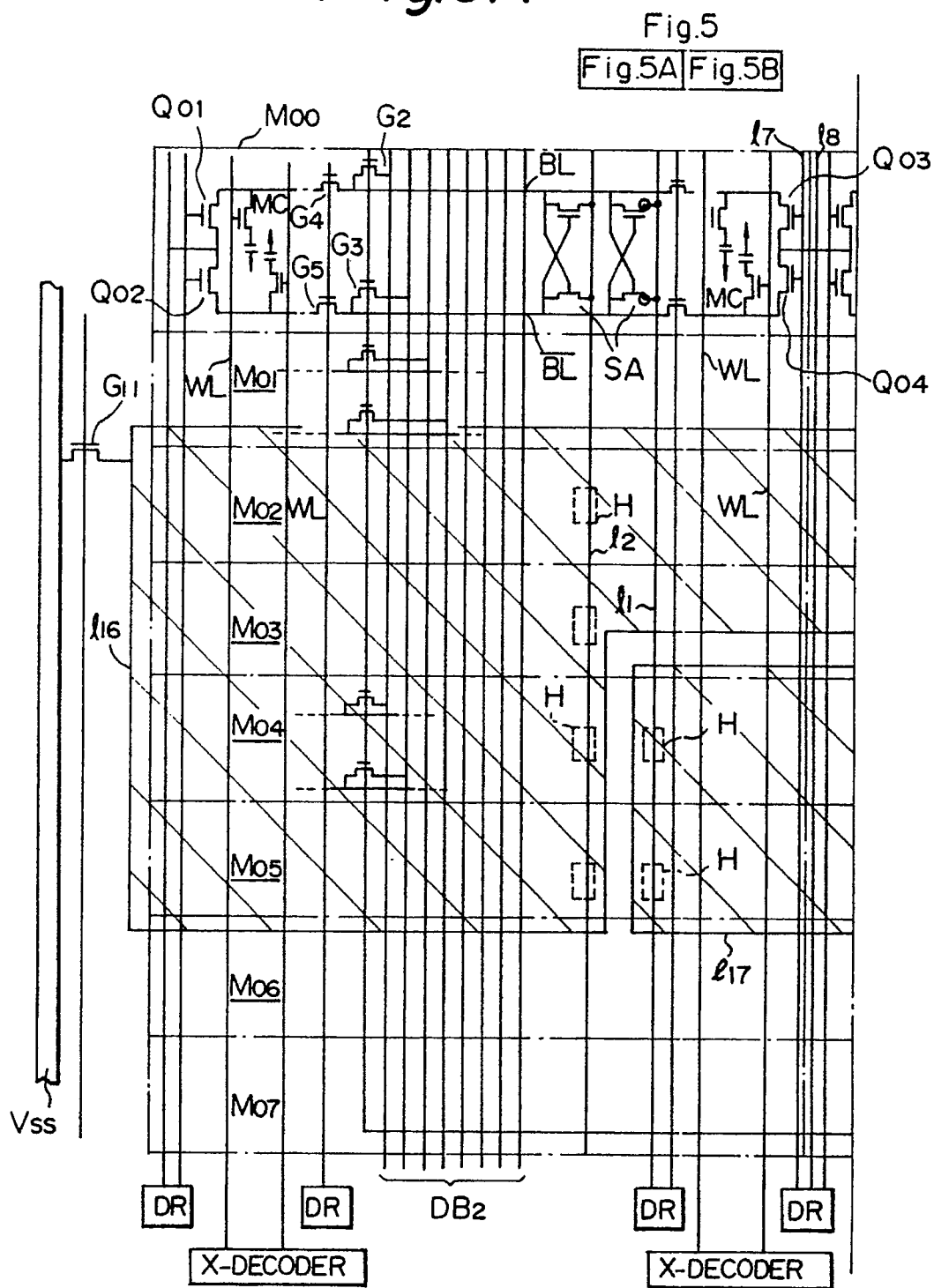


Fig.5B

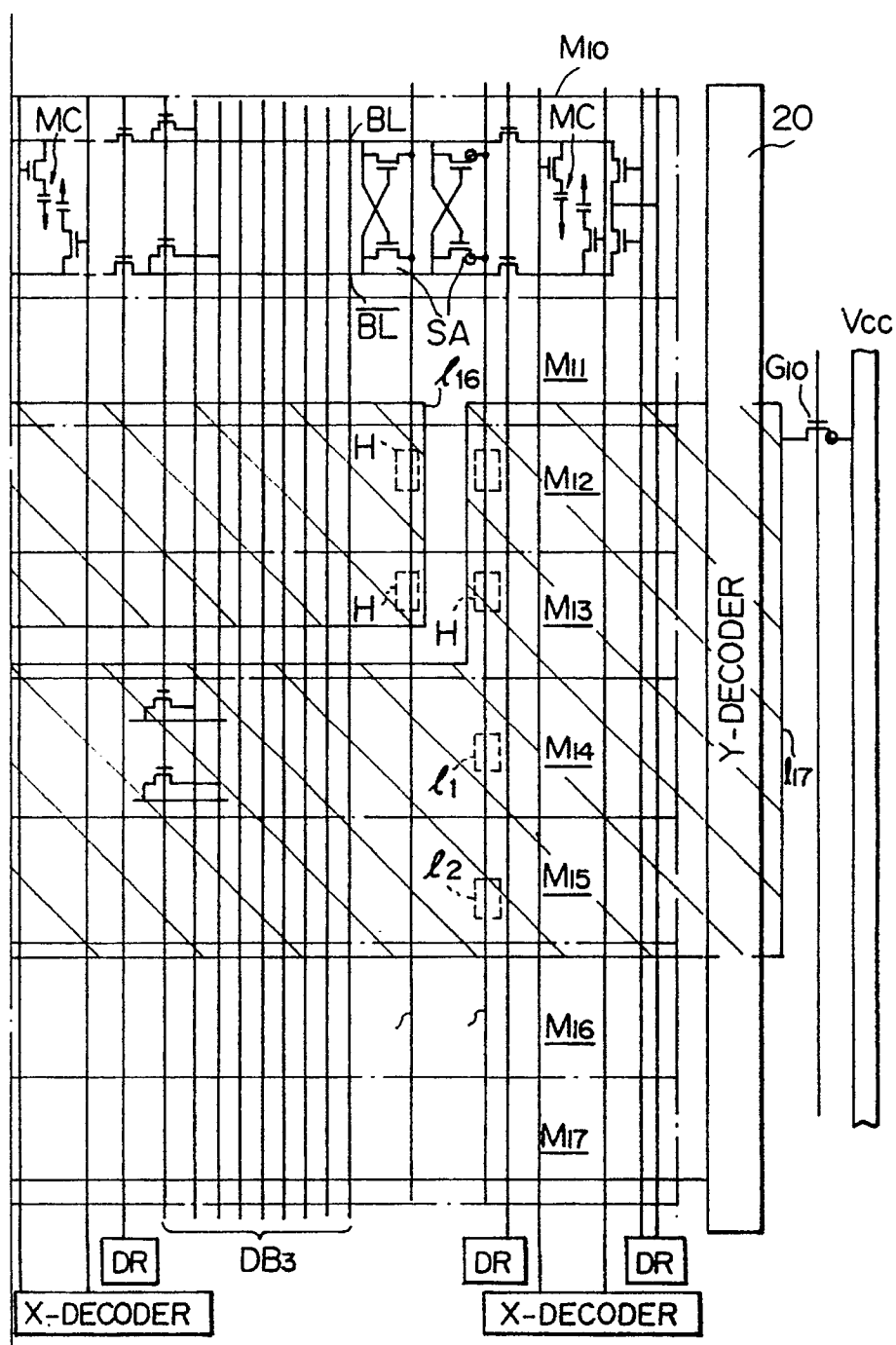


Fig.6

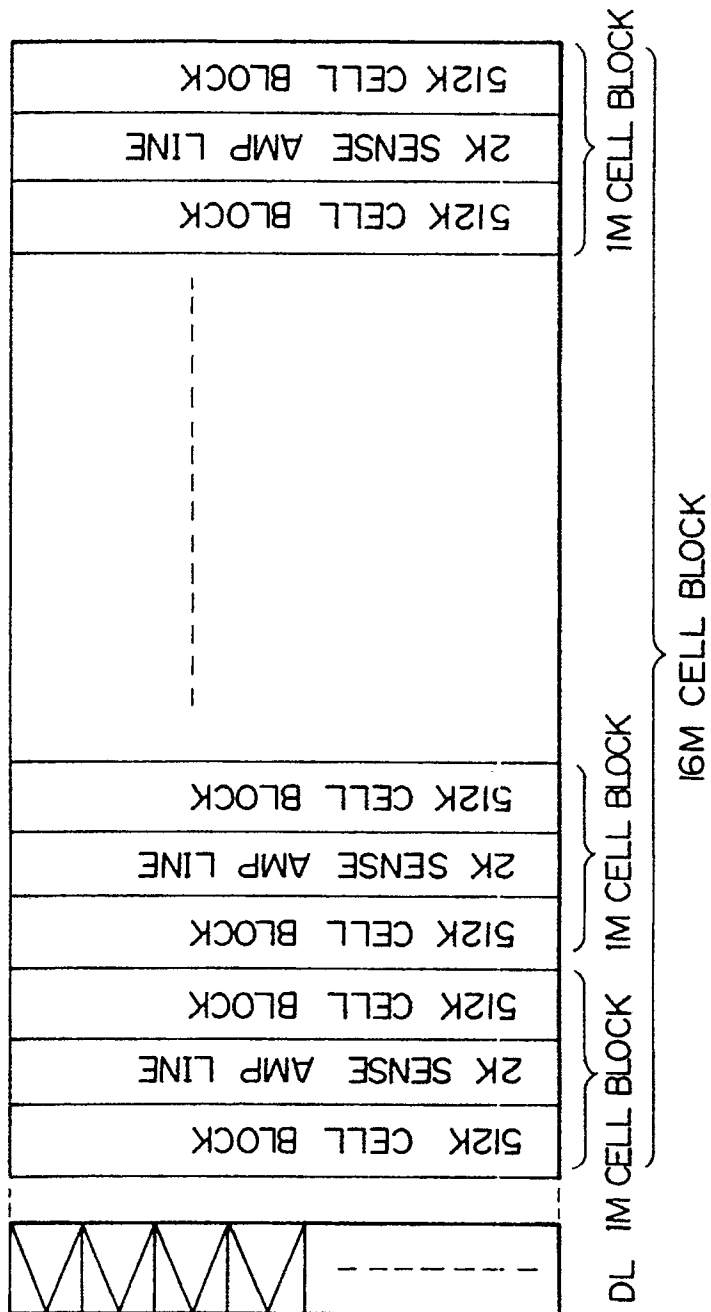


Fig. 7

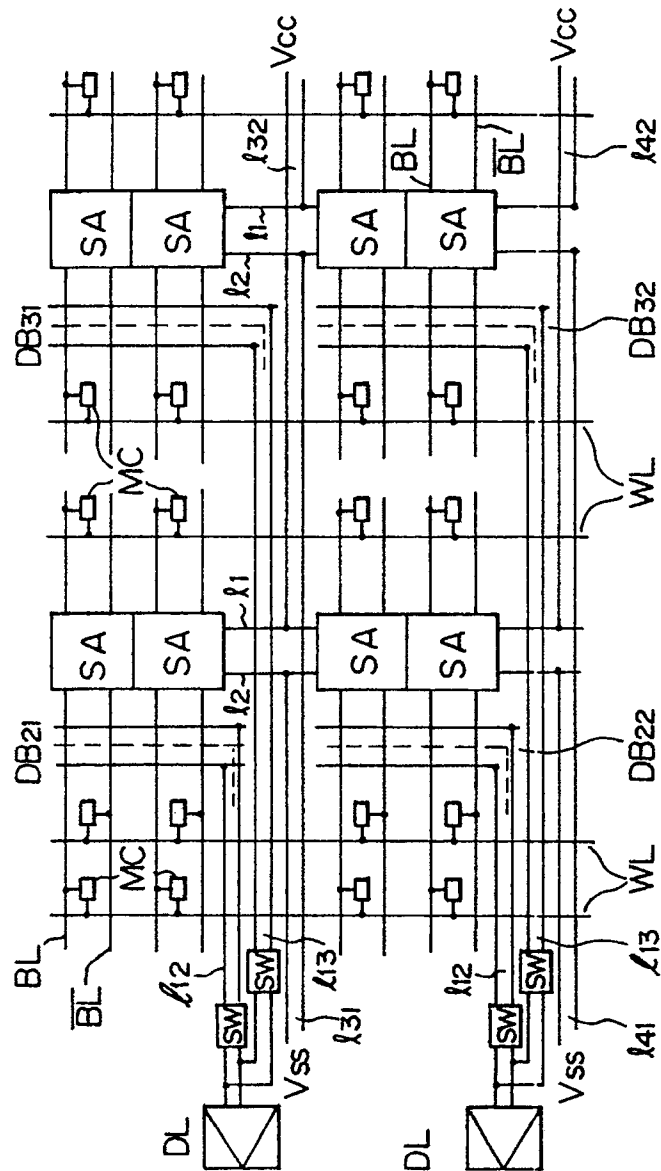


Fig. 8A

Fig.8

| | |
|--------|--------|
| Fig.8A | Fig.8B |
|--------|--------|

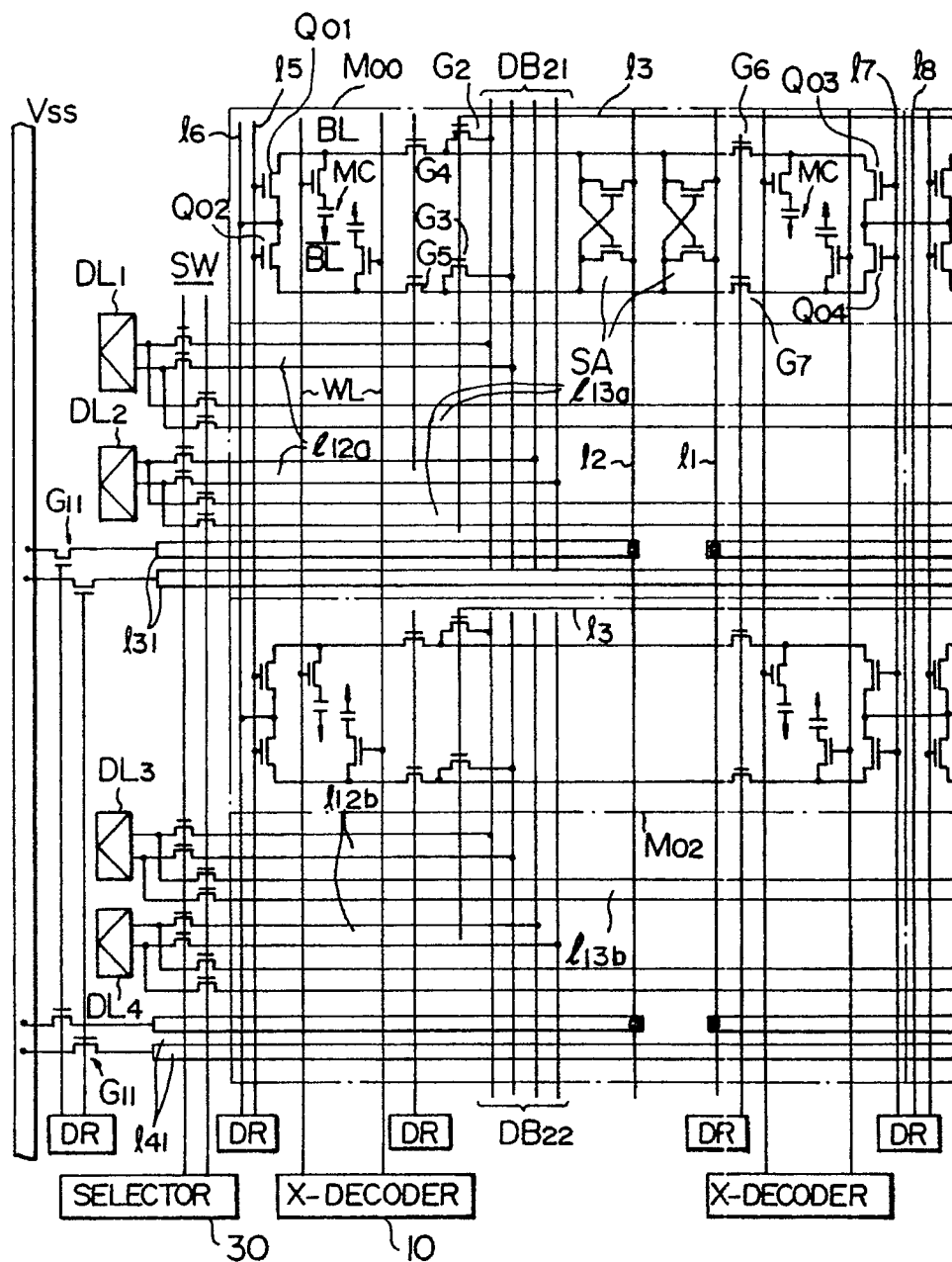


Fig. 8B

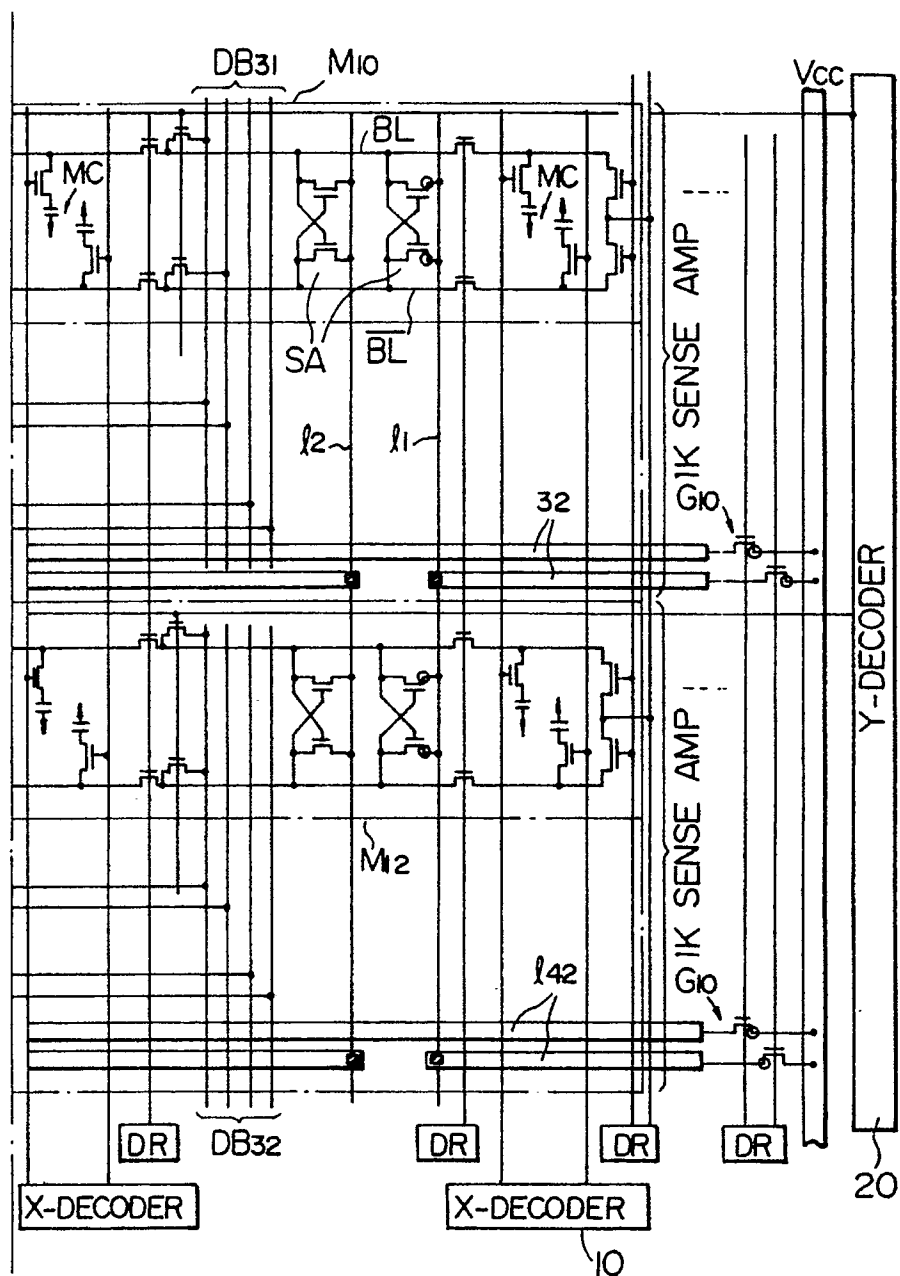


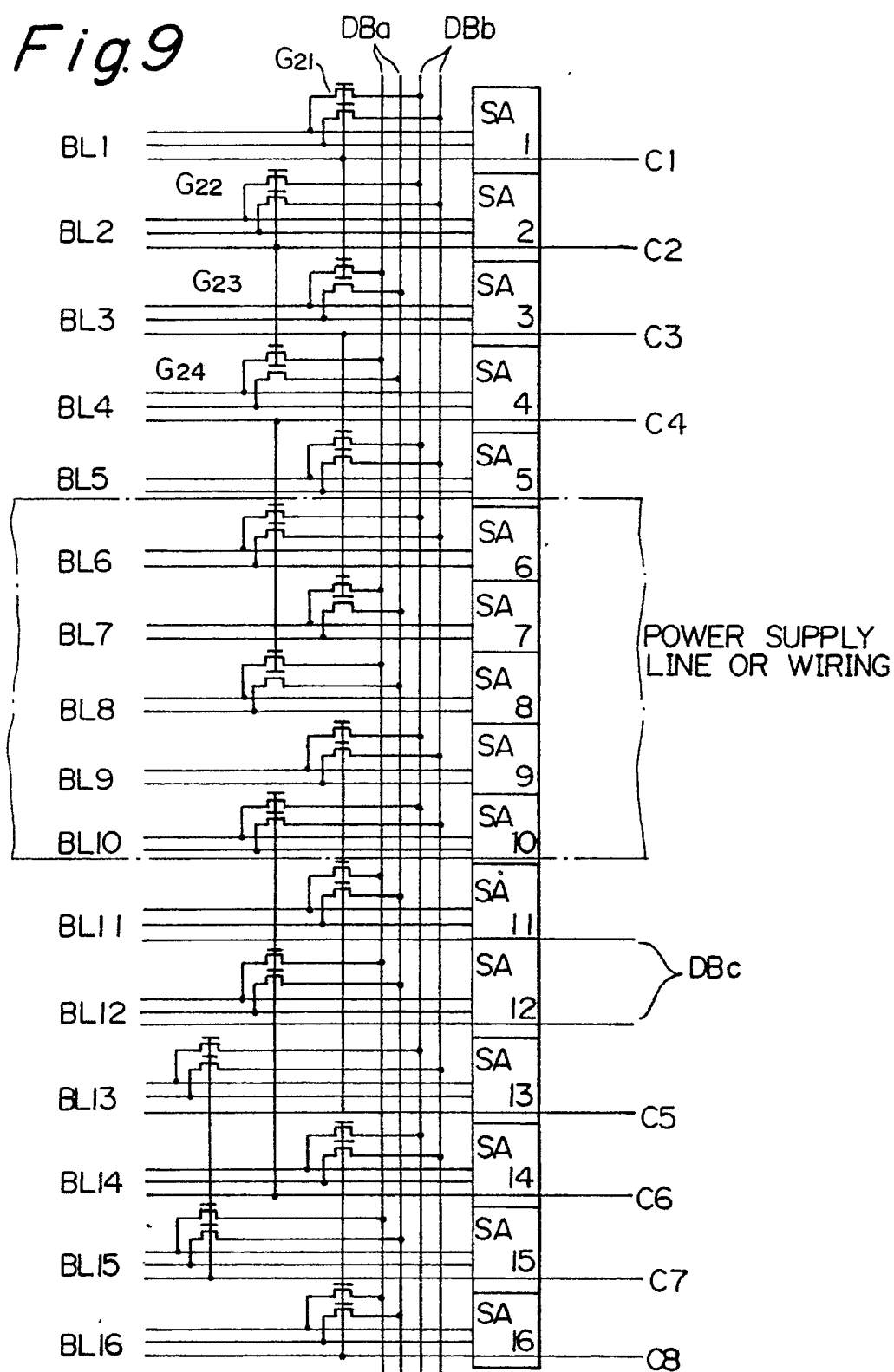
Fig.9

Fig. 10A

Fig.10

Fig.10A Fig.10B

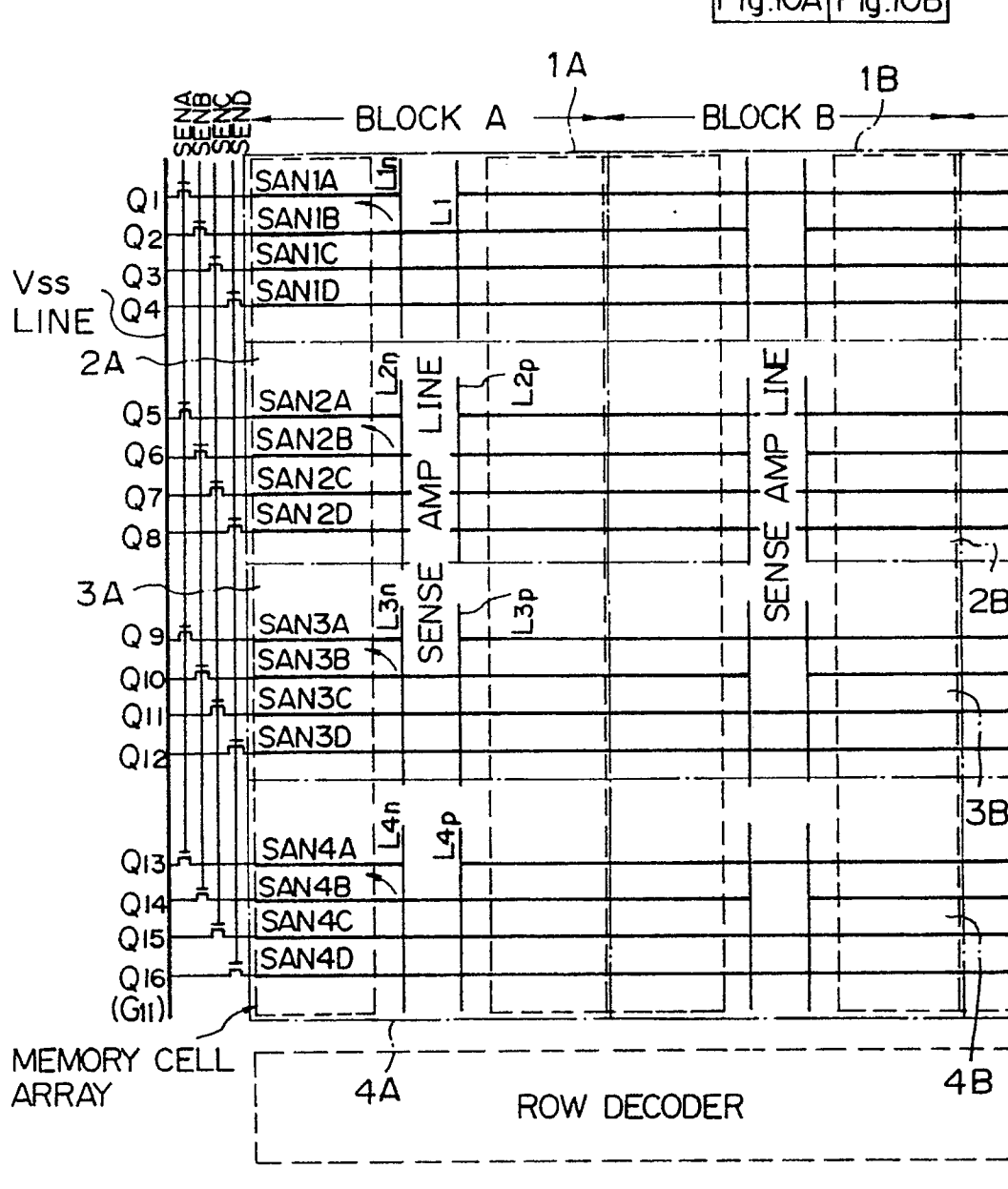


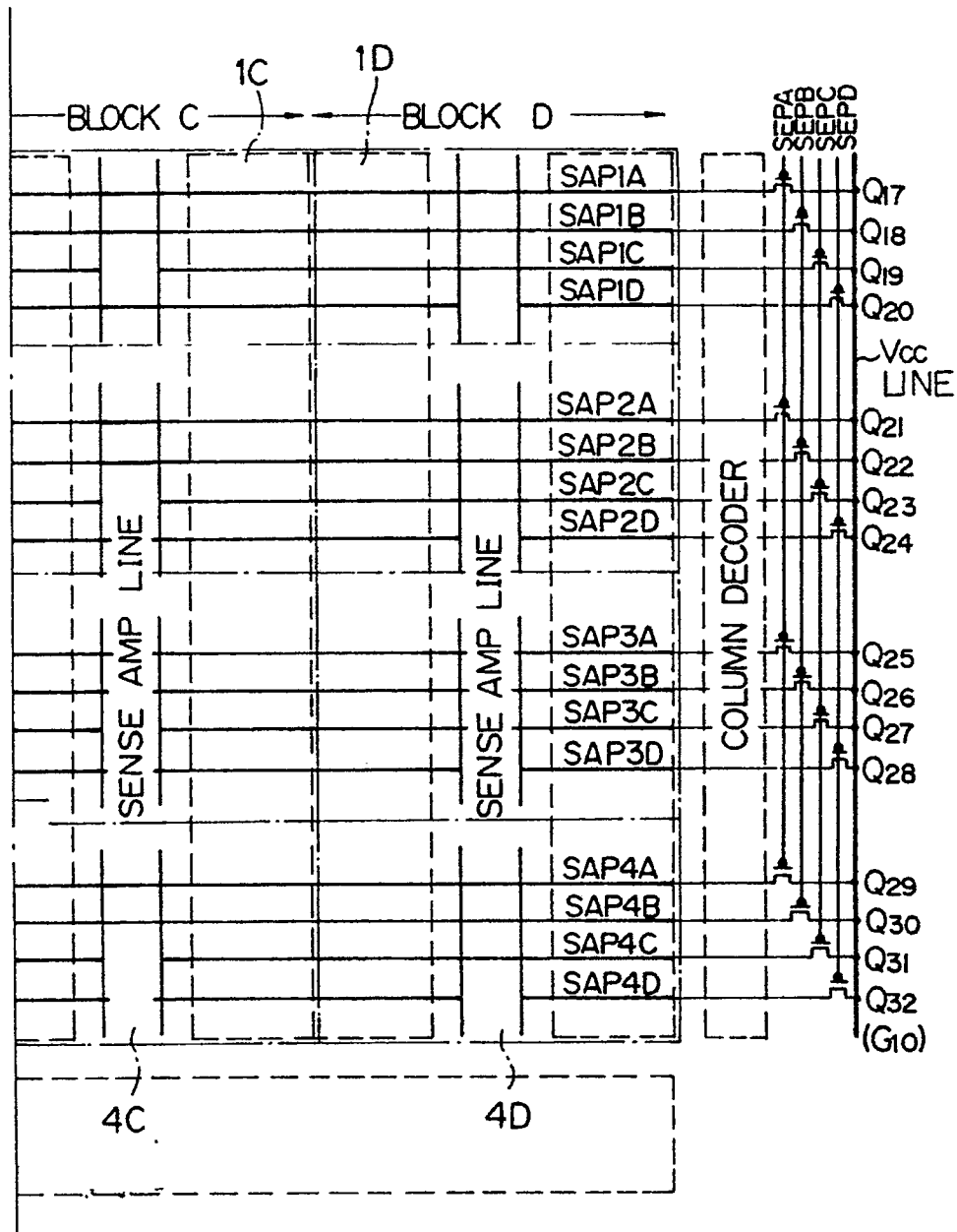
Fig.10B

Fig. 11

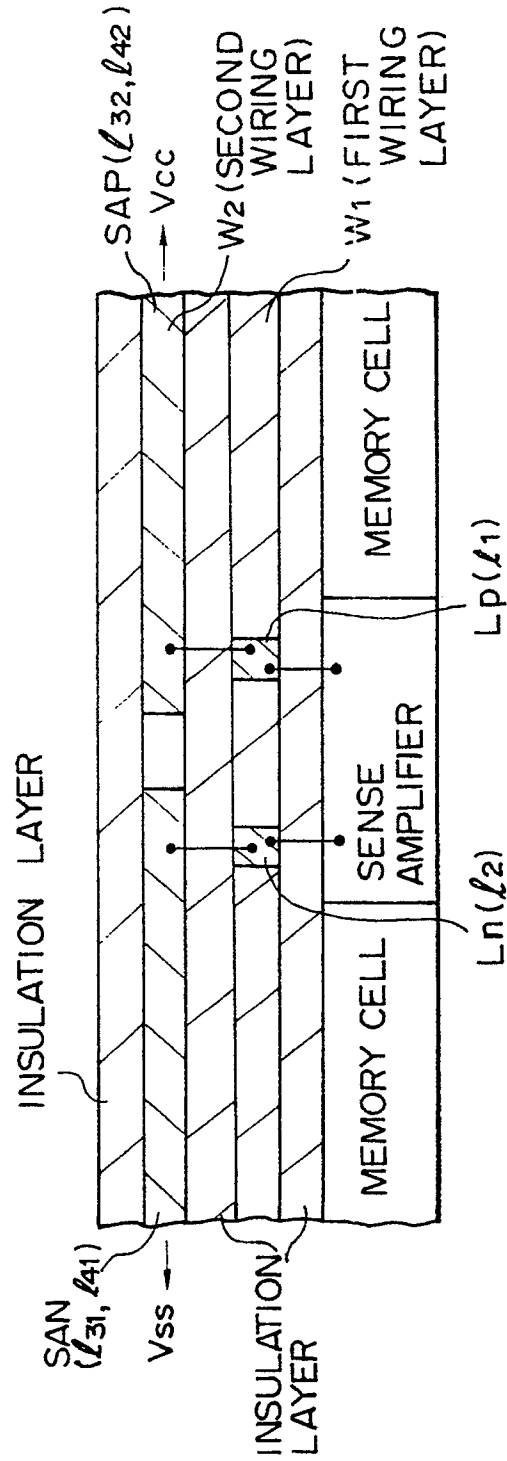


Fig.12
Fig.12A
Fig.12B

Fig.12A

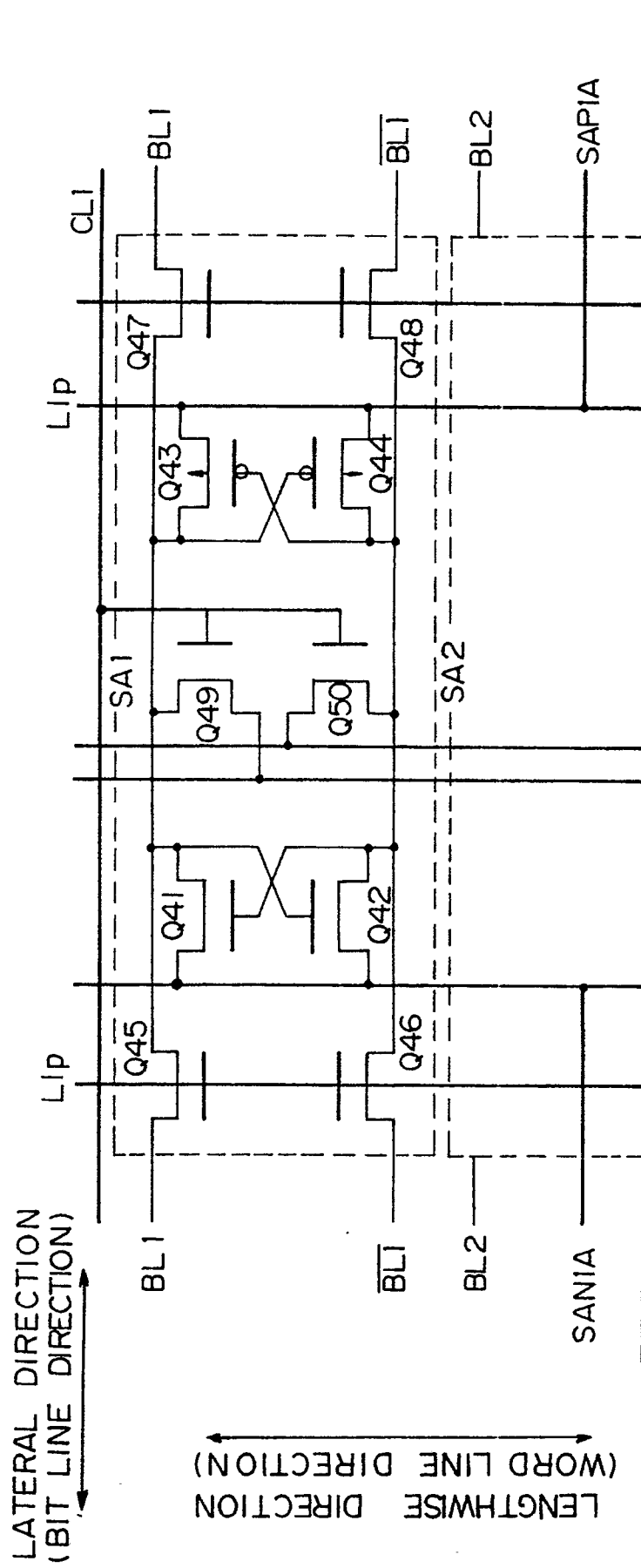


Fig. 12B

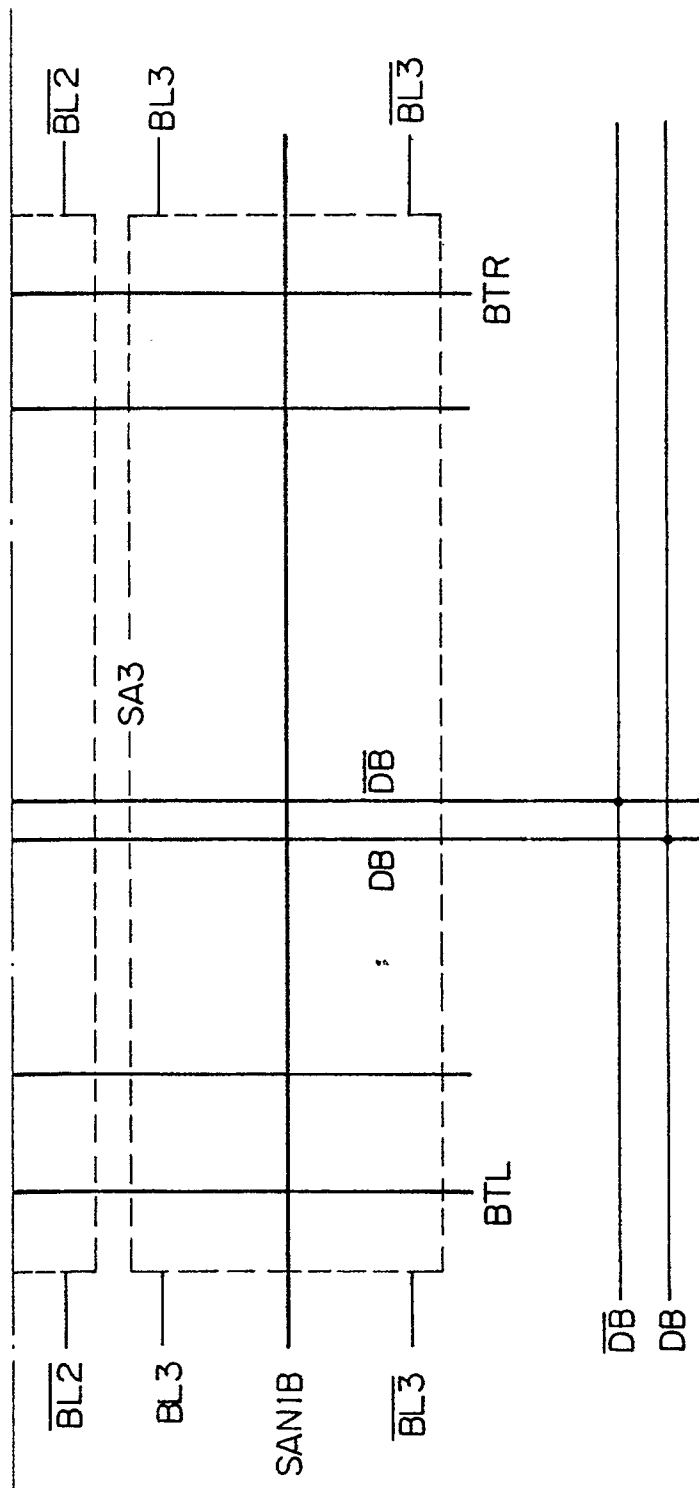


Fig. 13A

Fig. 13

Fig. 13A Fig. 13B

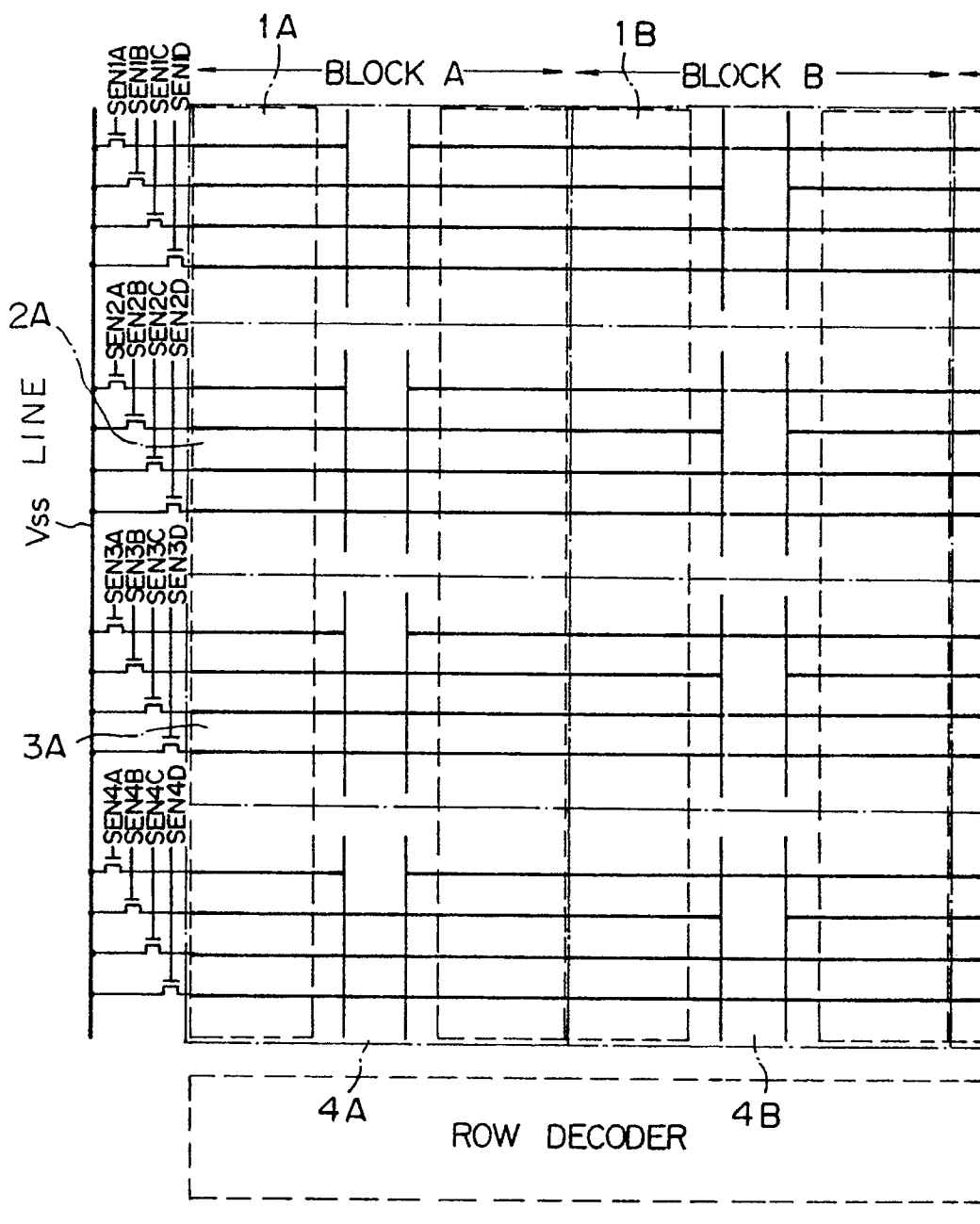


Fig. 13B

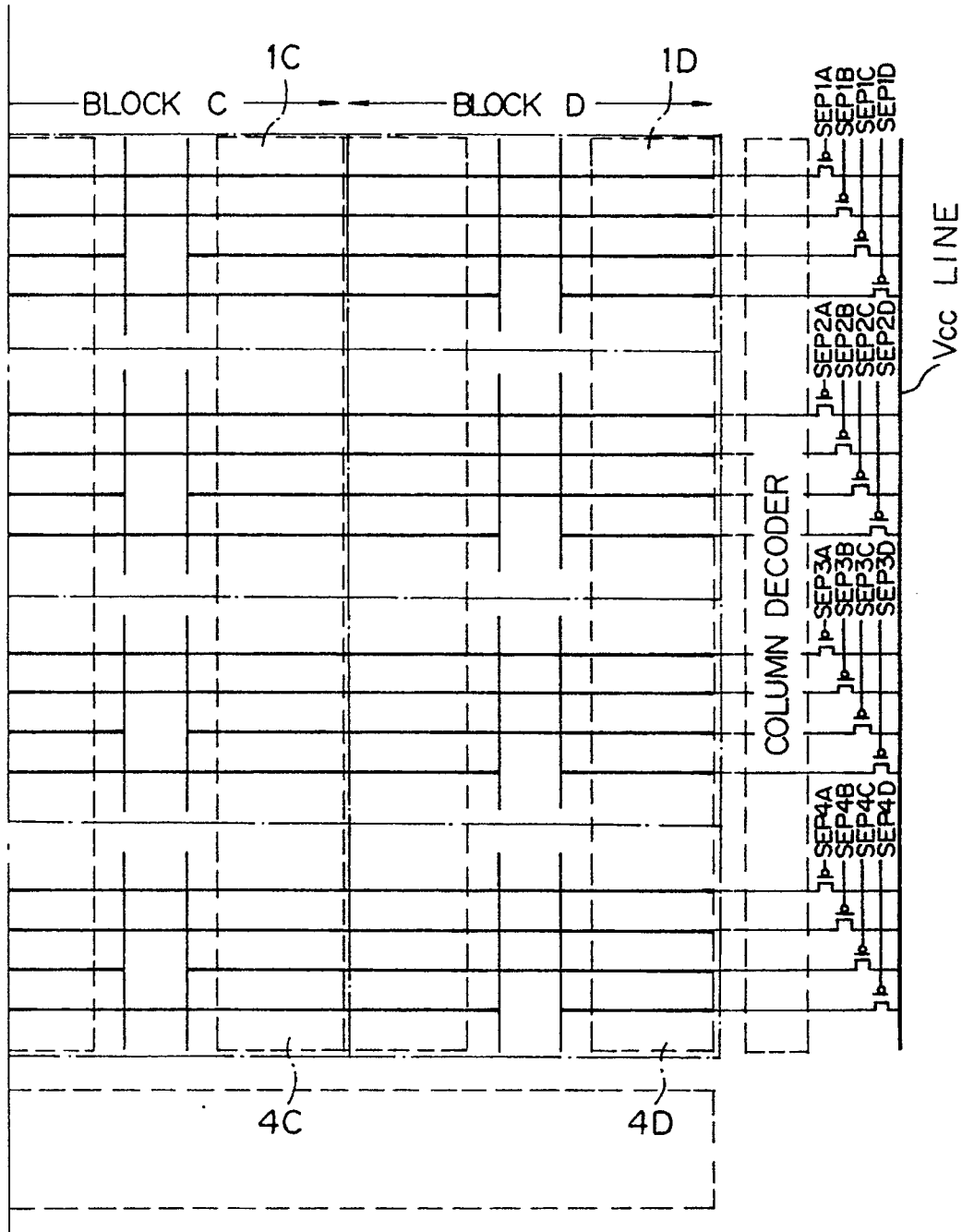
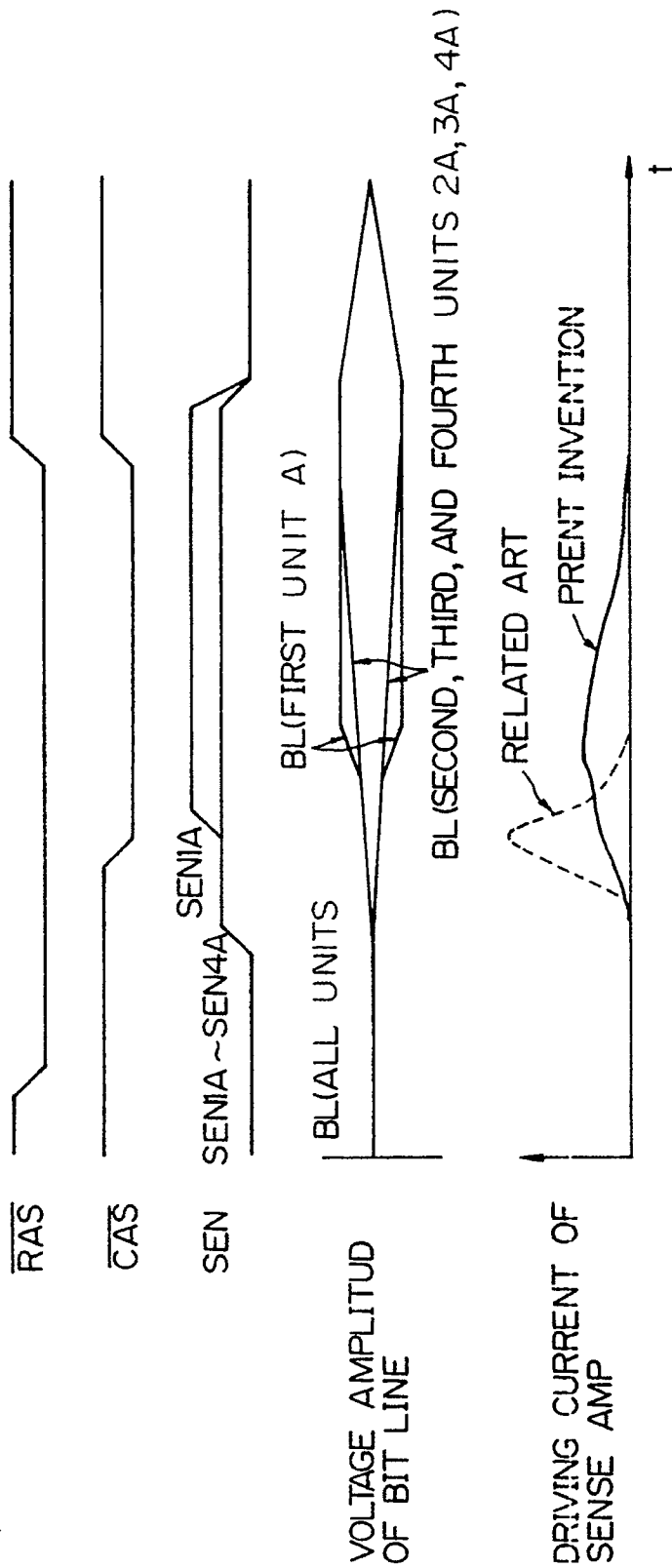


Fig. 14



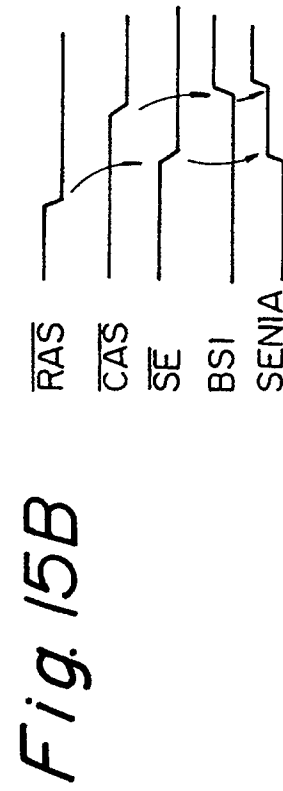
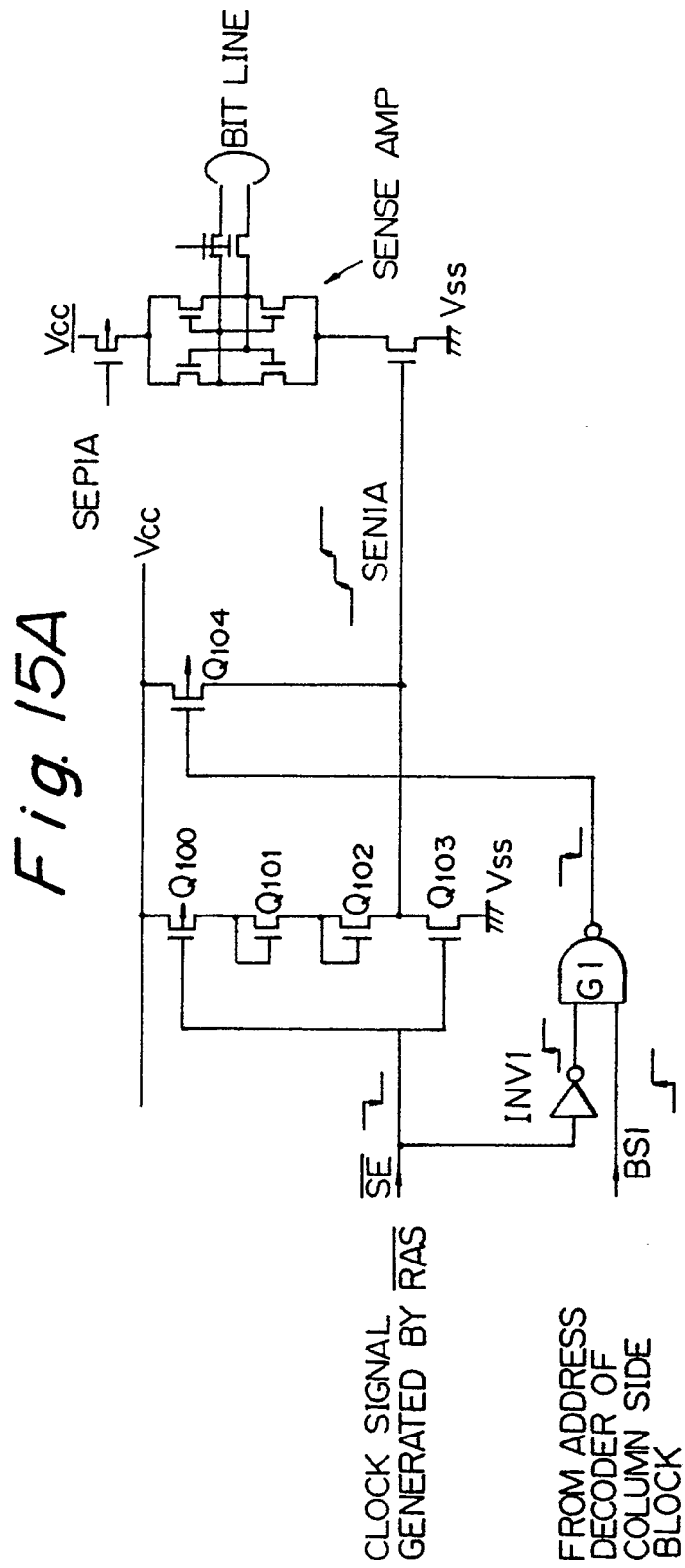


Fig. 16A

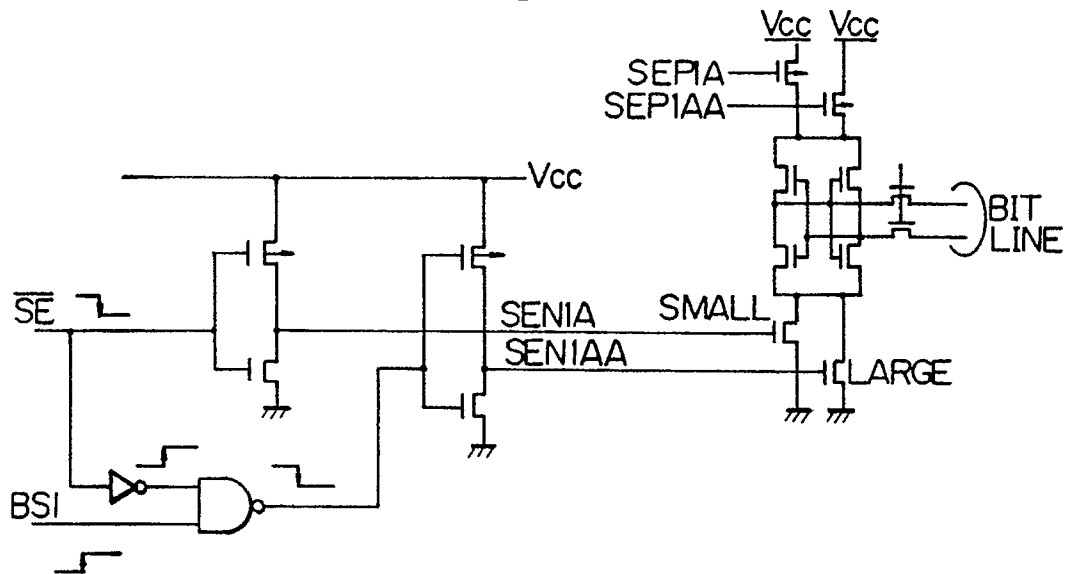


Fig. 16B

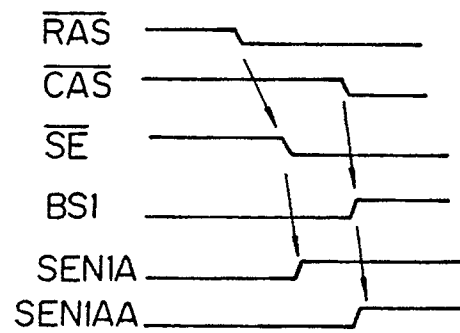


Fig. 17

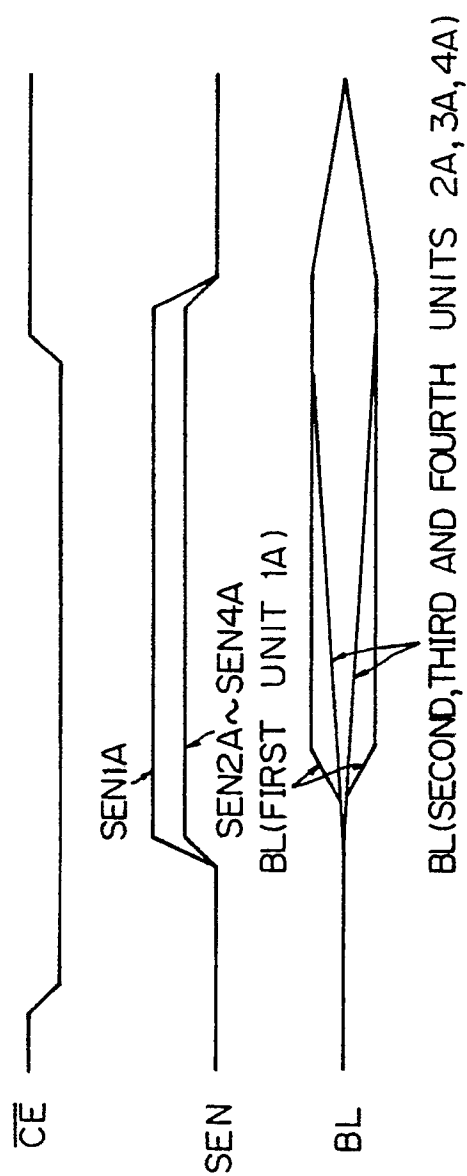


Fig. 18

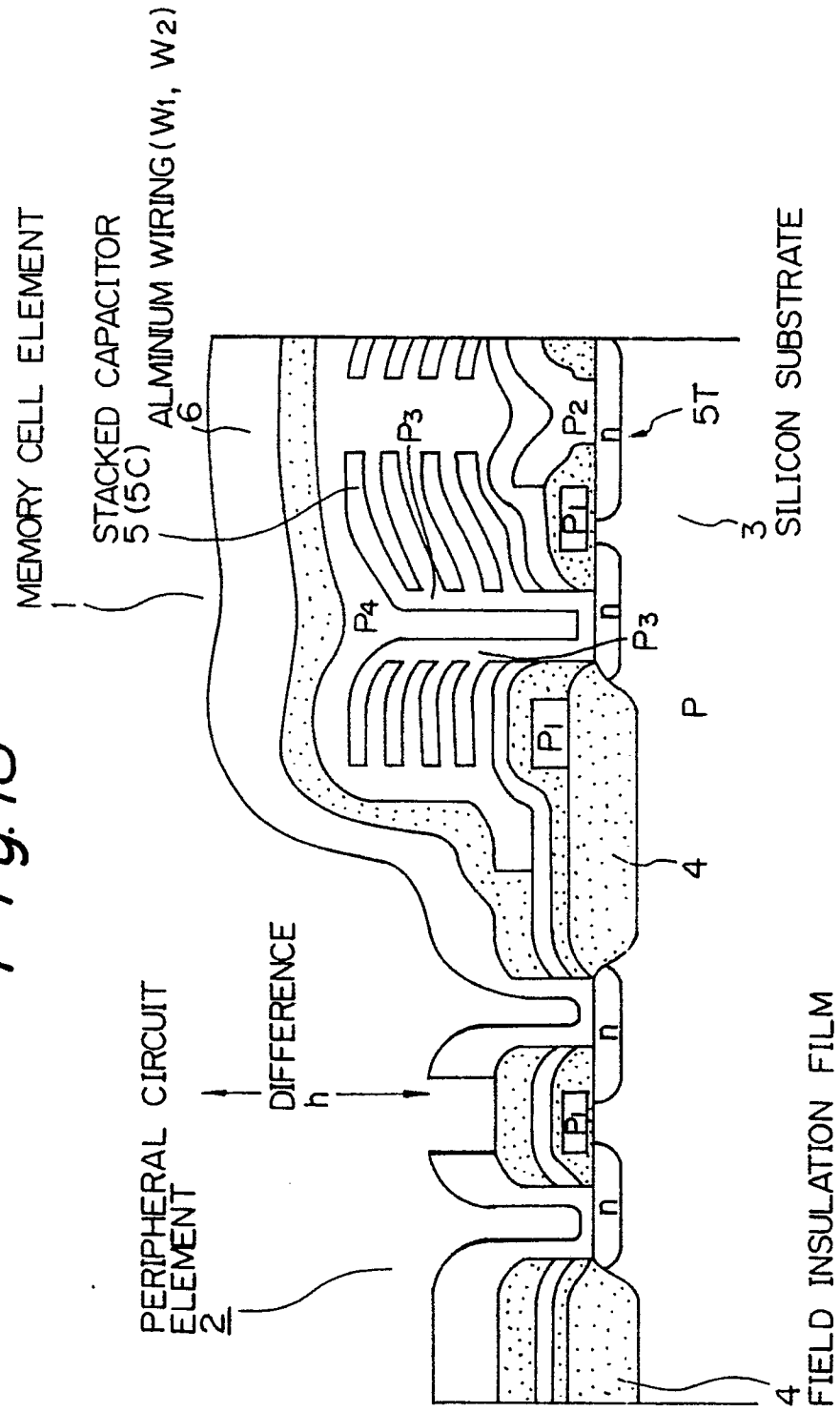


Fig. 19

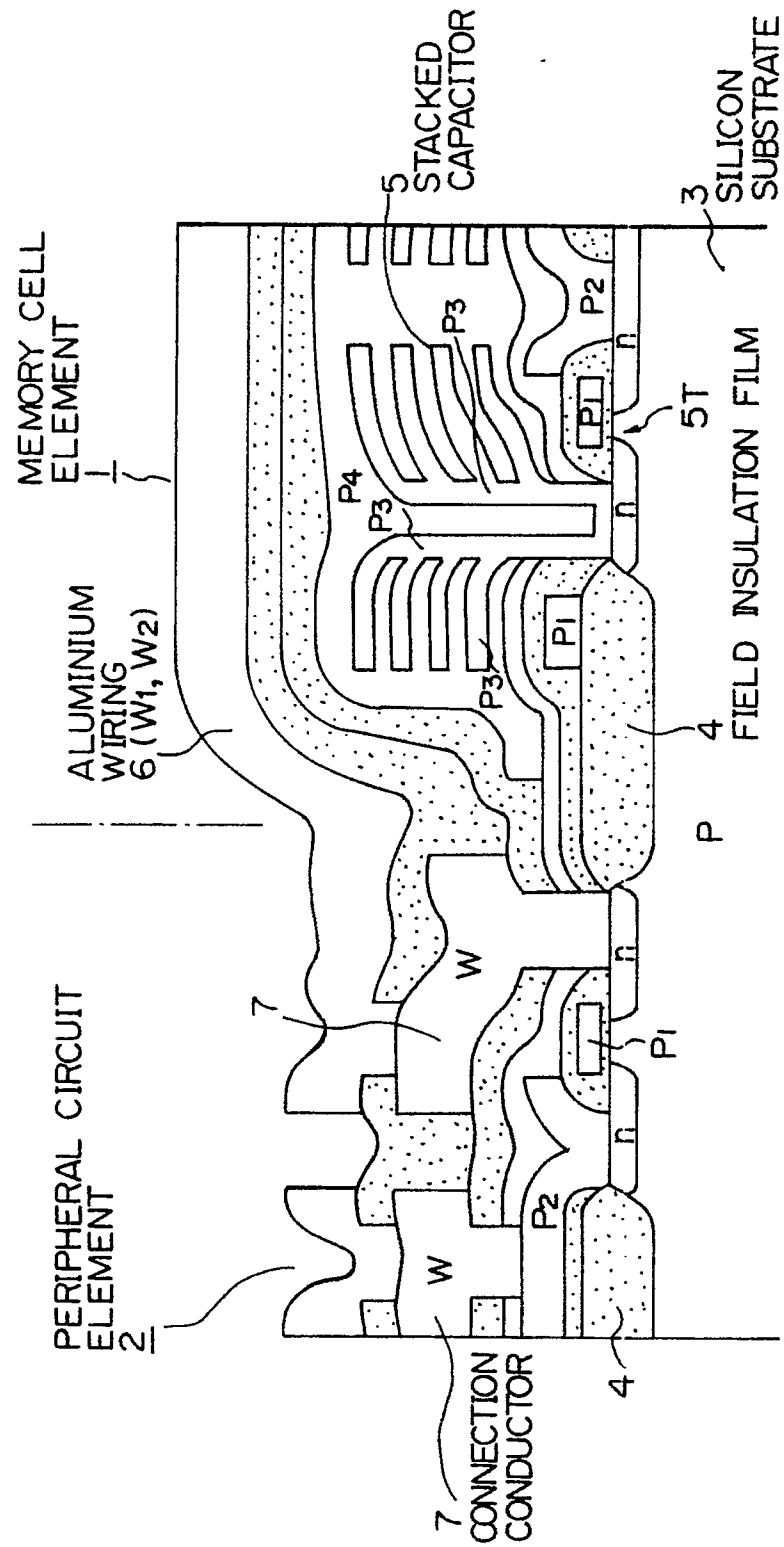


Fig. 20A

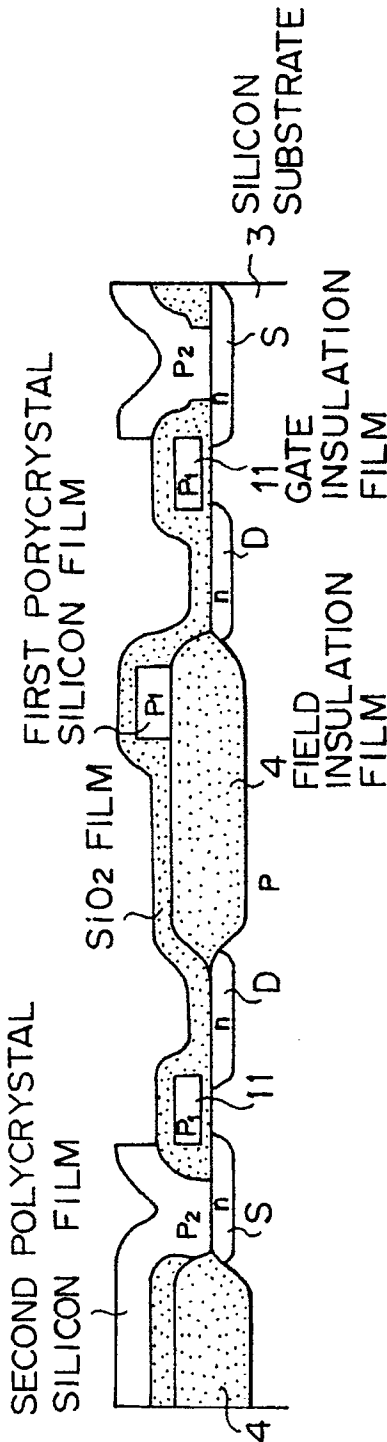


Fig. 20B

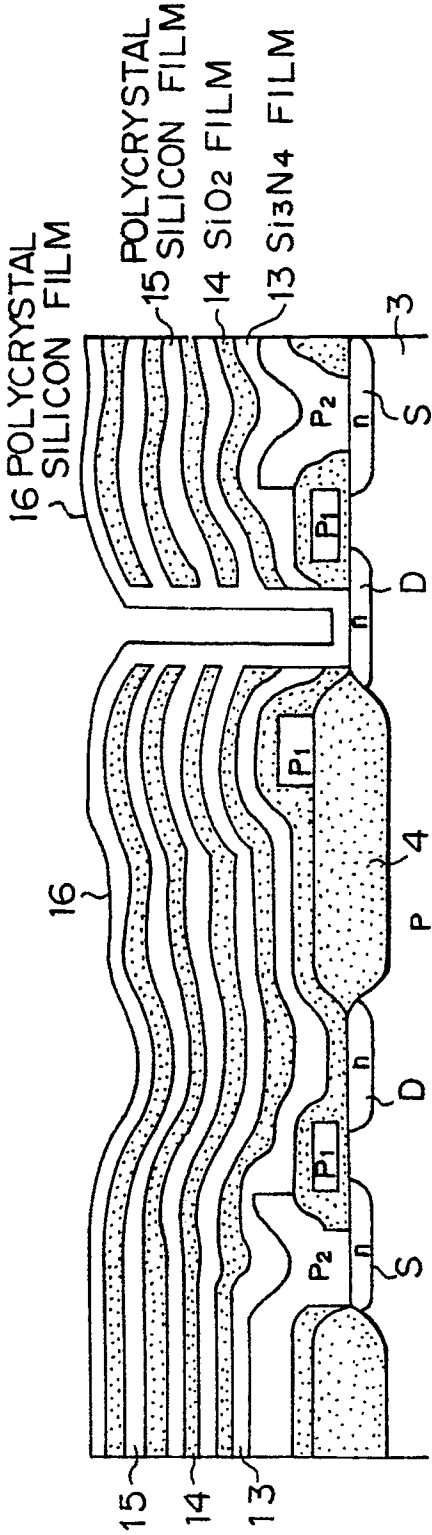


Fig. 20C

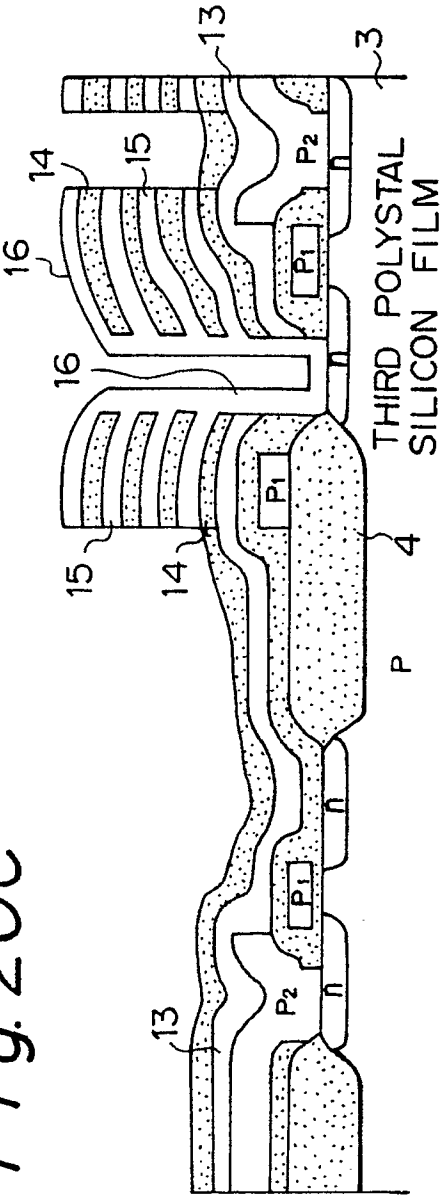


Fig. 20D

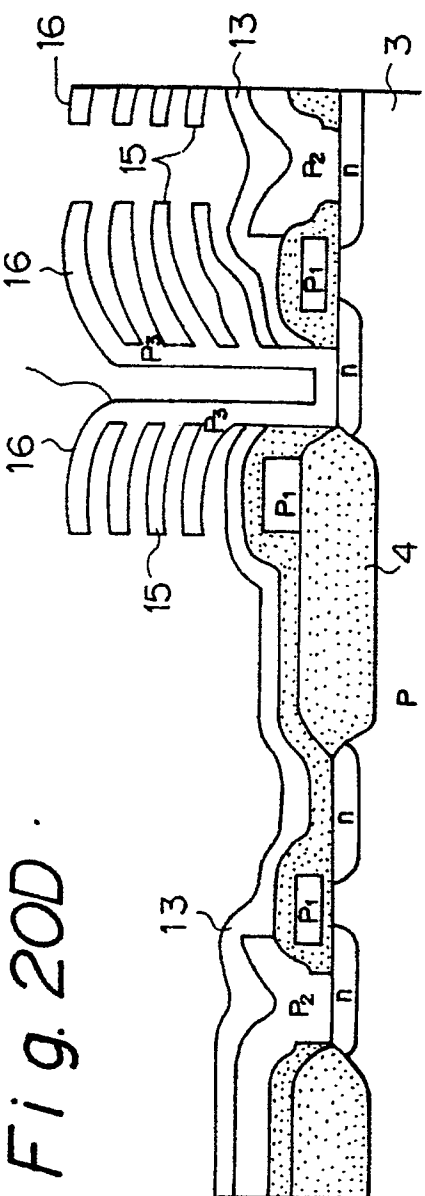


Fig. 20E

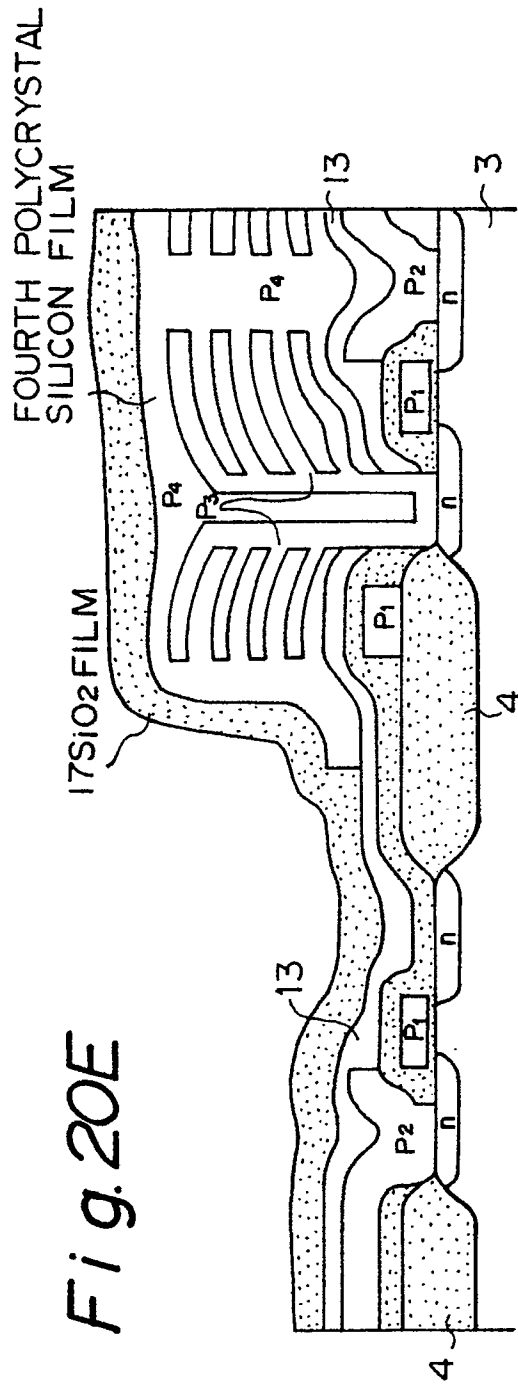


Fig. 20F

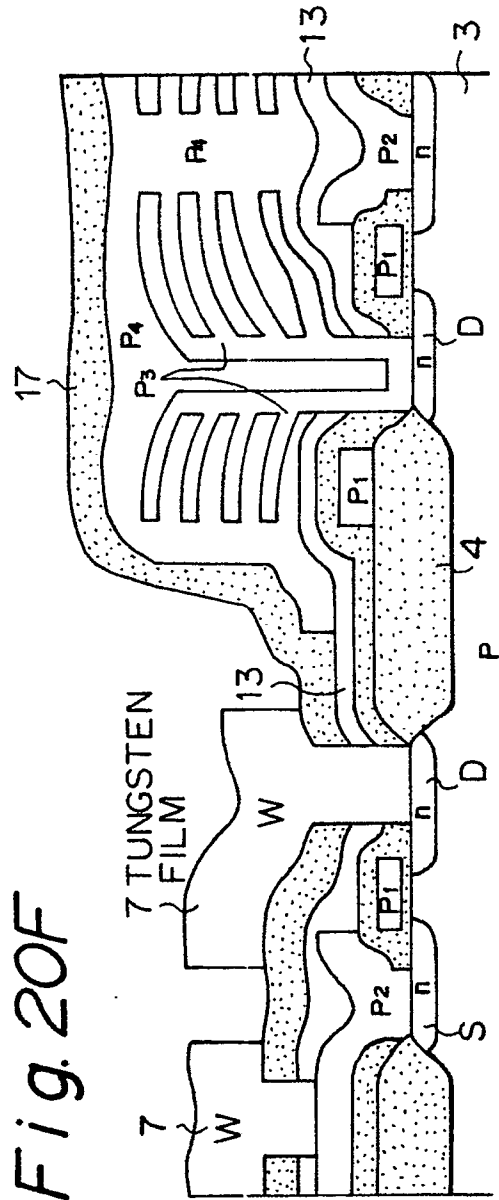
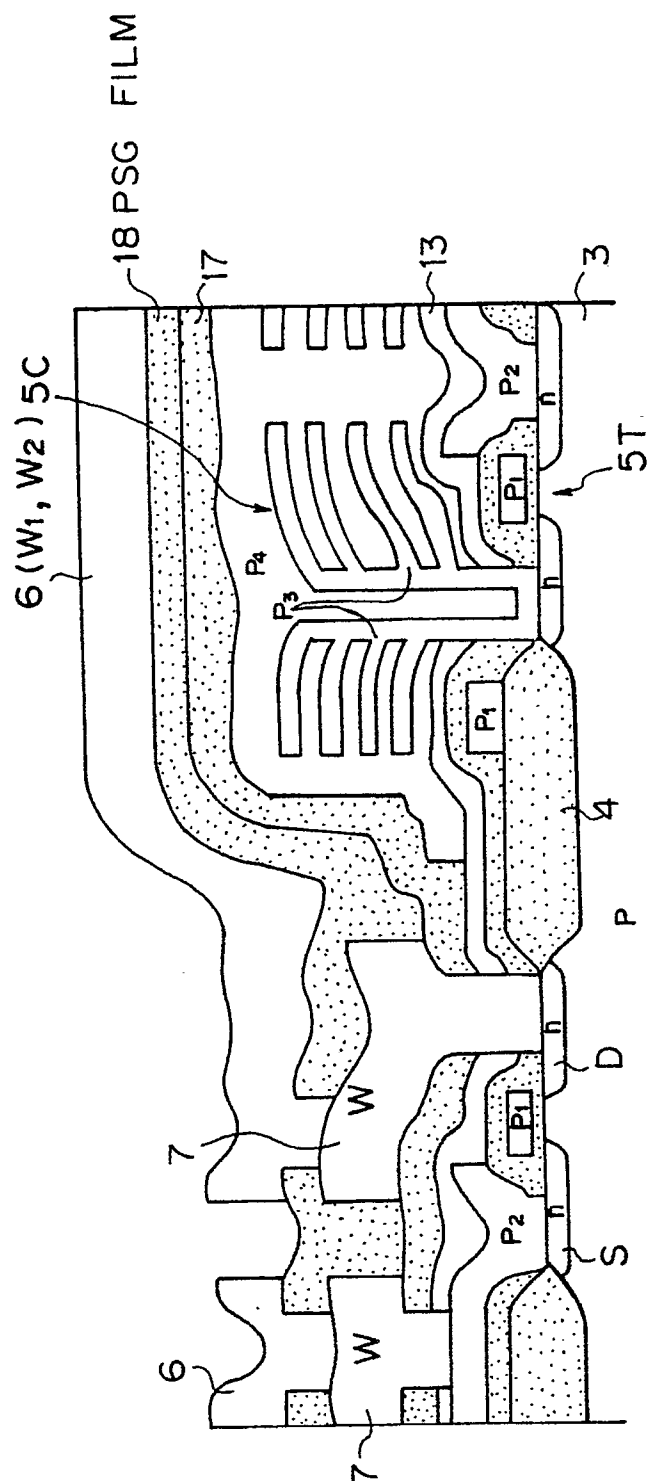


Fig. 20G





European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 30 6386

| DOCUMENTS CONSIDERED TO BE RELEVANT | | | |
|---|---|--|--|
| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
| A | EP-A-0 220 444 (IBM) * Figures 3,4; column 5, lines 3-28 * - - - | 1,21 | G 11 C 11/409 G 11 C 7/06 H 01 L 23/528 |
| A | GB-A-2 220 537 (SAMSUNG) * Figure 3; page 9, lines 11-24 * - - - | 1,2,3,5 | |
| A | IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 25, no. 1, February 1990, pages 30-35, New York, US; H. KOTANI et al.: "A 50-MHz 8-Mbit video RAM with a column direction drive sense amplifier" * Figure 2 * | 1,6,21 | |
| A | EP-A-0 115 128 (FUJITSU) * Figure 1; page 4, line 13 - page 5, line 4 * - - - - - | 4,13 | |
| | | | TECHNICAL FIELDS SEARCHED (Int. Cl.5) |
| | | | G 11 C 11/409 G 11 C 7/06 G 11 C 7/00 H 01 L 23/528 |
| The present search report has been drawn up for all claims | | | |
| Place of search The Hague | | Date of completion of search 12 February 91 | Examiner KAMSAETER K.M.S. |
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