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(54) AGC circuit for radio receiver

Automatische Verstärkungsregelung für einen Radioempfänger

Circuit de commande automatique de gain pour récepteur de radio

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The invention relates to an AGC circuit according to the preamble part of the main claim.

Such a AGC circuit is known from patent abstracts of Japan, Vol. 4, No. 117 (E-22) (599); and JP-A-55 071306.

2. Description of the Related art:

FIG. 7 of the accompanying drawings shows an equivalent circuit of a conventional AGC circuit used in a vehicle-mounted FM radio receiver. This AGC circuit, performing AGC by detecting the output signal level of a mixer, is disclosed in " '88 SANYO SEMICONDUCTOR DATA BOOK, CAR AUDIO BIPOLAR IC VOLUME (CQ PUBLISHING COMPANY)" at pages 124-136.

In FIG. 7, the numerals designate respectively: 10, a AGC circuit (AGC) integrated on an IC 12, for example; 14, an antenna circuit (ANT), the output of which is supplied to a first gate of a RF amplifier 16, and to which a pin diode 18 being an attenuator (ATT) of the ANT 14 is coupled to control the gain (attenuating amount) of the ANT 14; 20, a mixer (MIX) to which antenna signals having been amplified in the RF amplifier and local oscillating signals from a local oscillator (OSC) through a buffer 24 are input to perform a frequency conversion from the RF to the IF; 26, a level detector for detecting the level of an IF signal being the output signal from the mixer 20, the detected level signal being input to AGC 10.

The AGC 10 generates an AGC signal when the signal level becomes equal to or above a predetermined level to execute gain control of the antenna circuit 14 and the RF amplifier 16.

Namely, such a AGC is applied since the level of the signal to be input to the radio receiver greatly changes depending on the distance from the transmitting channel, propagating condition or the like, and it must be adjusted to be within the optimum range of the process in the receiver. In particular, in a vehicle-mounted receiver, since the distance from the transmitting channel changes with the passage of time, and the propagating condition is greatly different depending on the running position of the vehicle, the antenna input level would change extremely within a range of 1 μV - 3V, for example. Accordingly, such an AGC circuit would be indispensable to provide a satisfactory receiving state even in case of the signal level being low, and to provide a non-jamming signal reception suppressing the stress of the higher harmonic wave caused by a non-linear element such as a transistor, FET, or a variable capacitance diode at the time of receiving signals of high level.

The AGC signal is applied to the pin diode 18 and the second gate of the RF amplifier 16 through the 6th pin and the 13th pin of the IC 12 respectively, so as to reduce the level of the RF signal. In this manner, the AGC 10 functions to keep the output level of the mixer 20 constant by the AGC signal.

In this case, the relationship of the mixer input frequency to the AGC sensitivity will be represented as shown in FIG. 8. As shown in FIG. 8, the larger the detuning degree Δf with respect to the central frequency ($\Delta f = 0$) of a desired channel, the lower the AGC sensitivity.

If no AGC is provided, a third higher harmonic wave may be caused by non-linearity of e.g. Tr when the input levels of ANT and MIX become larger, thereby degradating the IM (intermodulation) disturbing property. Therefore, the AGC is provided to attenuate the RF signal and to suppress the generation of the stress, in order to improve the disturbing property.

As disturbances to be considered in the AGC circuit, an intermodulation disturbance (three signal property) and a adjacent channel disturbance (two signal property) can be listed.

The former is a disturbance generated by mixing the higher harmonic wave caused by the non-linearity of the element due to the level of the large signal input with a desired station frequency. For eliminating this intermodulation disturbance, the signal level at a frequency band remote from the desired channel frequency is attenuated by the AGC circuit. Therefore, it is preferable to set the AGC property to a broad band AGC.

On the contrary, the latter adjacent channel disturbance occurs when a strong electric field disturbance channel exists near the desired channel, and the desired channel is a weak electric field.

Namely, for generating an AGC signal from the mixer output in the above-mentioned prior art, if a adjacent channel having a large electric field intensity with respect to the desired channel, the AGC would emit the AGC signal to the adjacent channel due to the property represented in FIG. 8. At this time, the signal level of the desired station tends to be simultaneously attenuated, consequently, the mixer input become extremely small.

Further, when AGC signal is generated from the mixer input by improving the conventional circuit, the AGC circuit would mis-operate due to a local oscillating signal. Namely, as mentioned above, a local oscillating circuit composed of the local oscillator 22 and the buffer 24 is provided at the front end of the FM receiver, and the signal level, 300 mVrms - 1 Vrms, is quite higher than the mixer input level. In addition, the frequency of the local oscillating signal is so high as 50 MHz - 120 MHz, near the mixer input signal band. Therefore, the local oscillating signal would tend to invade the AGC circuit through the GND line, the Vcc line, or the space propagation, generating an erroneous AGC signal due to the local oscillating signal level. Such a mis-operation of the AGC circuit would reduce the gain of the RF amplifier significantly, thereby degradating the sensitivity.

Therefore, in case of applying AGC to a detected

mixer input level, the sensitivity of the AGC must be reduced. But by this reduction, an additional problem, that the disturbance (eliminating) property with respect to a frequency particularly having a small detuning degree f is degraded, would newly arise.

Conventionally, as a further improved AGC circuit, keyed AGC is well known. In this keyed AGC, the controlling level of the AGC circuit is compensated by the use of the IF section output level of the radio receiver.

Thus, in this conventional circuit, the AGC controlling amount is reduced or cut off when the output level of the IF section is low so as to prevent the sensitivity degradation.

However, in such a keyed AGC, there has occured an inconvenience that the keyed AGC would operate even in a non-signal state having no output level, thereby significantly amplifying the intermodulation disturbance.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to provide an AGC circuit which is capable of effectively suppressing both of the intermodulation disturbance and the adjacent channel disturbance, and of certainly preventing the invasion of the local oscillating frequency signal, so as to set an optimum AGC amount.

This object is solved by the features of the main claim.

Further advantages are shown in the subclaims.

Thus, according to the AGC circuit of this invention, both of the intermodulation disturbance and the adjacent channel disturbance can be certainly eliminated by providing a first and a second AGC systems detecting the output/input levels of the mixer, each having a individual detecting sensitivity different from each other. Further, according to this invention, since the first AGC system, for performing the middle band AGC in accordance with the output level of the IF section, is compensated, the inconveniences in the conventional keyed AGC can be certainly eliminated.

The above and other advantages, features and additional objects of this invention will be manifest to those versed in the art upon making reference to the following detailed description and the accompanying drawings in which a preferred structural embodiment incorporating the principles of this invention is shown by way of illustrative example.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit block diagram showing an embodiment of an AGC circuit according to this invention;

FIG. 2 is an AGC sensitivity diagram in the first level wave-detecting circuit;

FIG. 3 is an AGC sensitivity diagram in the second level wave-detecting circuit;

FIG. 4 is an synthetic AGC sensitivity diagram in this invention;

FIG. 5 is a synthetic AGC counting property diagram compensated by the output of the IF section according to this invention;

FIG. 6 is a specific diagram showing a preferred embodiment of an AGC circuit according to this invention;

FIG. 7 is an equivalent circuit block diagram showing an example of a conventional AGC circuit;

FIG. 8 is a conventional AGC sensitivity diagram.

DETAILED DESCRIPTION

The principles of this invention are particularly useful when embodied in an AGC circuit such as shown in FIG. 1 in connection with Fig. 6. In FIG. 1, the same numerals designate the same or corresponding components as those in FIG. 7.

In FIG. 1, the numeral 30 designates a band-pass-filter for shutting out signals over 50 MHz in the output signal line of the mixer 20 to eliminate local oscillating signals (50MHz - 120MHz).

The numeral 32 designates a first level wave-detecting circuit of this invention, having a detecting sensitivity which lowers in accordance with the detuning degree Δf with respect to a predetermined central frequency e.g. IF frequency f1.

The first level wave-detecting circuit 32 constitutes a first AGC system for applying AGC to the detected output signal level of the mixer 20 having been limited its frequency band by the band-pass-filter 30.

The numeral 34 designates a second level wave-detecting circuit. As shown in FIG. 3, this circuit 34 has a constant detecting sensitivity irrespective of the central frequency e.g. a detuning degree with respect to the tuning frequency. T he second level wave-detecting circuit 34 constitutes a second AGC system for detecting the input signal level of the mixer 20 in accordance with the detecting sensitivity.

Since a high-frequency such as 60MHz - 110MHZ is input to the second level wave-detecting circuit 34, the frequency property of the level wave-detecting circuit 34 must have a broad band-pass property at least approximately to 110MHz. Such a frequency band is substantially the same as that of the local oscillating signals (50MHz - 120 MHz), which would cause mis-operation of the AGC 10 by a sudden invasion of of the local oscillating signal. Therefore, in this embodiment, the AGC sensitivity (detecting sensitivity) in the second level wave-detecting circuit 34 must be restricted to be lower than that in the first level wave-detecting circuit. This AGC sensitivity is set to such a value that would not cause any mis-operation and that could eliminate the intermodulation disturbance mentioned above.

The numeral 36 designates a adding circuit for outputting AGC signal from the AGC circuit 10 by adding the first level wave-detecting signal to the second level wave-detecting signal. The adding circuit 36 includes a

offset circuit for determining the offset amount of the AGC controlling signal output from the adding circuit 36. In the two systems of the AGC circuit according to this embodiment, firstly the local oscillating signals over 50MHz (- 120MHz) are eliminated from the output signal level of the mixer 20 by the band-pass-filter, and the first level wave-detecting circuit 32 outputs the first level wave-detecting signal in accordance with the property represented in FIG. 2.

On the contrary, the second level wave-detecting circuit 34 outputs the second level wave-detecting signal from the input signal level of the mixer 20 in accordance with the property represented by FIG. 3.

The first and the second level wave-detecting signals are mutually added in the adding circuit 36, and this AGC controlling signal is supplied to the attenuator 18 of the antenna circuit 14 and the RF amplifying circuit 16.

According to the two-sytem AGC of this embodiment, the integral properties could be represented by FIG. 4 formed by superimposing FIG. 2 and 3. In FIG. 4, at an area with a detunig degree relatively close to the central frequency, namely at a middle band area with a range of F = ± 1MHz, mainly the first AGC system having the higher detecting sensitivity functions in accordance with the output signal level of the mixer 20. Meanwhile, at a broad band where the detuning degree is larger than that, the second AGC system has a priority to operate, in accordance with the input signal level of the mixer 20.

Therefore, according to this invention, it is possible to realize an AGC operation capable of most effectively coping with any type of disturbances, by dividing the bands into a middle band and a broad band on the basis of the detuning degree from the central frequency and applying individual AGC to each of them.

Namely, for the broad band, the detecting sensitivity is kept constant by the second level wave-detecting circuit 34, thereby preventing the intermodulation disturbance over a broad frequency band, and preventing the excessive suppression of the detecting sensitivity of the central frequency by an excessive AGC application.

Meanwhile, for the adjacent channel disturbance at frequencies close to the central frequency, the undesirable influences of the local oscillating signal can be eliminated by disposing a band-pass-filter capable of shutting out signals over 50MHz, and by enhancing, at the detuning time, the constant detecting sensitivity of the second level wave-detecting circuit to be higher than that of the first level wave-detecting circuit.

In the present invention, further, the disadvantages having arisen by e.g. conventional keyed AGC can be certainly eliminated by applying an AGC compensation to the first AGC system by the output level of the IF section.

In FIG. 1, the IF section for executing FM demodulation upon receiving the output from the mixer 20 at the front end, is designated by a numeral 40. In this embodiment, the output of this IF section being a multi-stage limiter is taken as a narrow band signals because of having a central frequency component. This IF signal is supplied to the S meter 42 where the signal level of a desired channel is detected. Of course, the output of the S meter (signal meter) 42 is used by the other circuits of the radio receiver, in this embodiment the output of the S meter 42 is supplied to the first level wave-detecting circuit 32 for compensating the detecting sensitivity in accordance with the output level of the IF section.

FIG. 5 shows an AGC compensating operation of the first AGC system by the output of the IF section. In the middle frequency band, the detecting sensitivity is controlled as shown by section lines from the state of the dashed line to the state of the solid line in accordance with the output level of the IF section.

The chain line in FIG. 5 stands for a detecting sensitivity for the second AGC system in substantially same manner as in FIG. 4, in the case where the output of the IF section is sufficiently large.

On the contrary, the solid line in FIG. 5 stands for a state where the output level of the IF section is lowered. In this state, the lowered control by the first AGC system acts to certainly prevent the excessive AGC application by the conventional keyed AGC, mentioned above.

FIG. 6 shows a more detailed AGC circuit diagram according to this invention, where the same components as in FIG. 1 are designated by the same numerals and omitted to be mentioned.

In FIG. 6, the band-pass-filter 30, for supplying the output signal of the mixer 20 to the first level wave-detecting circuit 32 by limiting the frequency band, is composed e.g. of a ceramic filter, which is represented equivalently by a resistor and a condenser. Alternatively, the shown band-pass-filter 30 can be installed separately from the ceramic filter as a two-staged filter. In such a case as the AGC circuit being composed of IC and having the band-pass-filter therein, a stray capacitance (parasitic capacitance) would arise as shown in dashed line. In such IC, therefore, the frequency of the band-pass-filter 30 is determined taking account of the parasitic capacitance.

The output of the band-pass-filter 30 is supplied to the base of the transistor 50 in the first level wave-detecting circuit 32, and the signals according to the property shown in FIG. 2 are supplied to the first input transistor 52 in the adder circuit 36. The condenser 53 keeps the potential according to the current flowing through the transistor 50 at its upstream side, thereby currents according to the level of the input signal to the first level circuit 34 flow through the transistor 52.

On the contrary, the input signal level of the mixer 20 is supplied to the base of the transistor 54 provided in the second level wave-detecting circuit 34, the output of which is supplied to the base of the second input transistor 56 in the adder circuit 36 as shown in FIG. 3. The condenser 55 keeps the potential according to the current flowing through the transistor 54 at its upstream side, thereby current according to the level of the input

signal to the second level circuit 34 flows through the transistor 56.

Accordingly, the adder circuit 36 receives an input made by mutually adding the both collector currents of the transistors 52, 56, thereby a synthesized AGC controlling signal is supplied from the output terminal 36a to the attenuator 18 and the RF amplifier 16 shown in FIG. 7 to perform the gain control. As mentioned above, the adder circuit 36 contains an offset circuit therein.

The both level wave-detecting circuits 32, 34 are provided with basic power source circuits 60, 62 respectively to supply predetermined collector currents to the transistors 50, 54 respectively.

In this invention, furthermore, an AGC compensating signal is supplied from the S meter 42 to the first level wave-detecting circuit 32 in accordance with the output level of the IF section, as mentioned above. In the shown embodiment, the output of the S meter 42 is supplied to the level converting circuit 64, the output of which is then supplied from the transistor 66 to the basic power source circuit 60 of the first level wave-detecting circuit 32.

Accordingly, the detecting sensitivity of the first level wave-detecting circuit 32 can be compensated by the output of the IF output level, namely, the output of the S meter 42.

Claims

1. An AGC circuit for a radio receiver which detects a receiving signal level to generate AGC signals corresponding to the detected signal level and controls the gain of an RF amplifying circuit (16) comprising:

   (a) a filter circuit (30) for allowing components of a predetermined frequency band in the output signal from a mixer (20) to pass therethrough;
   (b) a first level detecting circuit (32) forming a first AGC loop;
   (c) second level detecting circuit (34) for detecting an input signal level of the mixer (20), and forming a second AGC loop which has a detecting sensivity constant irrespective of the degree of detuning with respect to an IF frequency;
   (d) an adder circuit (36) for adding the first level detecting signal to the second level detecting signal to output an AGC signal;

   characterized in that

   (e) said first level detecting circuit (32) has a frequency band restricted by the filter circuit (30), and detects the output signal level of the mixer (20),
   (f) said first AGC loop has a detecting sensitivity varying in accordance with the degree of detuning with respect to the IF frequency;
   (g) a signal meter (42) detects the signal level of a desired channel signal output from the IF section (40) to which the mixer output is supplied;
   (h) an AGC compensating circuit (64) reduces the output of the first level detecting circuit (32) in accordance with the reduction of the IF signal level of the desired channel detected by said signal meter (42), thereby lowering the detecting sensitivity of the first AGC loop to reduce adjacent channel disturbance.

2. An AGC circuit according to claim 1, wherein the detecting sensitivity at the central frequency of said first level detecting circuit (32) is set to a value higher than that of said second level detecting circuit (34).

3. An AGC circuit according to claim 1, wherein said first (32) and second level (34) detecting circuits respectively comprise: a transistor (50, 54) through which electric current flows in accordance with the input signal level; a condenser (53, 55) disposed downstream said transistor to maintain the potential in accordance with the current flowing amount through the transistor.

4. An AGC circuit according to claim 3, wherein said adder circuit (36) comprises a pair of transistors (52, 56) the current flowing amount of which is determined in accordance with the upstream potential of the condenser of said first and second level detecting circuits, and the upstream of said pair of transistors is coupled to pass added current therethrough.

5. An AGC circuit according to claim 1, wherein said first level detecting circuit (32) further comprising:

   a transistor (50) through which electric currents flow in accordance with the input signal level;
   a condenser (53) disposed downstream said transistor for maintaining the potential in accordance with the current amount of said transistor; and
   a basic power source circuit (60) for maintaining the current amount flowing through said transistor (50).

6. An AGC circuit according to claim 5, wherein said AGC compensating circuit (64) includes a compensating transistor the current flowing amount through which is determined in accordance with the output of the S meter (42) ; and
   the output voltage of said reference power source is changed in accordance with the current value of

the compensating transistor.

Patentansprüche

1. AGC-Schaltung für einen Radioempfänger, die einen Empfangssignalpegel detektiert, um AGC-Signale entsprechend dem detektierten Signalpegel zu erzeugen, und welche die Verstärkung einer Radiofrequenzverstärkerschaltung (16) steuert, mit:

   a) einer Filterschaltung (30), um Komponenten eines vorbestimmten Frequenzbandes im Ausgangssignal von einem Mixer (20) durchzulassen;
   b) einem ersten Pegeldetektorschaltkreis (32), der eine erste AGC-Schleife bildet;
   c) einem zweiten Pegeldetektorschaltkreis (34) zum Detektieren eines Eingangssignals des Mixers (20) und zum Bilden einer zweiten AGC-Schleife, die eine konstante Detektionsempfindlichkeit hat, unabhängig vom Grad der Verstimmung bezüglich einer Zwischenfrequenz;
   d) einer Addierschaltung (36) zum Addieren des ersten Pegeldetektionssignals zum zweiten Pegeldetektionssignal, um ein AGC-Signal auszugeben;

   dadurch **gekennzeichnet,** daß

   e) der erste Pegeldetektionsschaltkreis (32) ein Frequenzband hat, das beschränkt ist durch die Filterschaltung (30) und den Ausgangssignalpegel des Mixers (20) detektiert,
   f) daß die zweite AGC-Schleife eine Detektierempfindlichkeit hat, die in Abhängigkeit mit dem Grad der Verstimmung bezüglich der Zwischenfrequenz variiert,
   g) daß ein Signalmesser (42) den Signalpegel eines gewünschten Kanalsignalausgangs vom Zwischenfrequenzabschnitt (40) detektiert, zu welchem der Mixerausgang zugeführt wird;
   h) und daß ein AGC-Kompensationsschaltkreis (64) das Ausgangssignal des ersten Pegeldetektionsschaltkreises (32) reduziert in Übereinstimmung mit der Reduktion des Zwischenfrequenzsignalpegels des gewünschten Kanals, welche durch den Signalmesser (42) detektiert wird, wodurch die Detektionsempfindlichkeit der ersten AGC-Schleife abgesenkt wird, um Nachbarkanalstörungen zu reduzieren.

2. AGC-Schaltung nach Anspruch 1,
   wobei die Detektionsempfindlichkeit bei der zentralen Frequenz des ersten Pegeldetektionsschaltkreises (32) auf einen Wert gesetzt wird, der höher ist als der des zweiten Pegeldetektionsschaltkreises (34).

3. AGC-Schaltung nach Anspruch 1,
   wobei der erste (32) und zweite (34) Pegeldetektionsschaltkreis jeweils aufweist:
   einen Transistor (50, 54) durch welchen ein elektrischer Strom fließt in Übereinstimmung mit dem Eingangssignalpegel; einem Kondensator (53, 55), der stromab von dem Transistor angeordnet ist, um das Potential zu halten in Übereinstimmung mit dem Stromfluß durch den Transistor.

4. AGC-Schaltung nach Anspruch 3,
   wobei der Addierschaltkreis (36) ein Paar von Transistoren (52, 56) aufweist, deren Stromfluß bestimmt ist in Übereinstimmung mit dem Stromlaufpotential des Kondensators des ersten und zweiten Pegeldetektionsschaltkreises, und daß stromauf von dem Paar von Transistoren gekuppelt ist, um einen zusätzlichen Strom hindurchzuführen.

5. AGC-Schaltung nach Anspruch 1,
   wobei der erste Pegeldetektionsschaltkreis (32) ferner aufweist: einen Transistor (50), durch welchen ein elektrischer Strom fließt in Übereinstimmung mit dem Eingangssignalpegel;
   einen Kondensator (53), der stromab vom Transistor angeordnet ist, um das Potential beizubehalten in Übereinstimmung mit dem Stromfluß des Transistors; und
   eine Grundspannungsversorgungsschaltung (60) zum Aufrechterhalten des Stromflusses durch den Transistor (50).

6. AGC-Schaltung nach Anspruch 5,
   wobei die AGC-Kompensationsschaltung (64) einen Kompensationstransistor aufweist, dessen Stromdurchfluß bestimmt wird in Übereinstimmung mit dem Ausgangssignal des Signalmessers (42); und
   die Ausgangsspannung der Bezugsspannungsquelle geändert wird in Übereinstimmung mit dem Stromwert des Kompensationstransistors.

Revendications

1. Circuit de commande automatique de gain AGC pour un récepteur radio, qui détecte un niveau de signal de réception pour engendrer des signaux AGC correspondant au niveau de signal détecté et qui commande le gain d'un circuit d'amplification haute fréquence (16),comprenant :

   (a) un circuit de filtrage (30) pour permettre le passage de composantes d'une bande de fréquence prédéterminée dans le signal de sortie d'un mélangeur (20) ;
   (b) un premier circuit de détection de niveau (32) formant une première boucle AGC ;

(c) un deuxième circuit de détection de niveau (34) pour détecter un niveau de signal d'entrée du mélangeur (20) et former une deuxième boucle AGC qui a une sensibilité de détection constante indépendamment du degré de désaccord par rapport à une moyenne fréquence ; et
(d) un circuit d'addition (36) pour ajouter le premier signal de détection de niveau au deuxième signal de détection de niveau afin de fournir un signal AGC ;

caractérisé en ce que :

(e) ledit premier circuit de détection de niveau (32) a une bande de fréquence limitée par le circuit de filtrage (30) et il détecte le niveau de signal de sortie du mélangeur (20) ;
(f) ladite première boucle AGC a une sensibilité de détection qui varie en fonction du degré de désaccord par rapport à la moyenne fréquence ;
(g) un signal-mètre (42) détecte le niveau de signal d'une sortie de signal de canal désiré provenant de la section de moyenne fréquence (40) à laquelle la sortie du mélangeur est fournie ; et
(h) un circuit de compensation AGC (64) réduit la sortie du premier circuit de détection de niveau (32) en fonction de la réduction du niveau de signal de moyenne fréquence du canal désiré détecté par ledit signal-mètre (42), afin. d'abaisser la sensibilité de détection de la première boucle AGC pour réduire la perturbation des canaux adjacents.

2. Circuit AGC suivant la revendication 1, dans lequel la sensibilité de détection à la fréquence centrale dudit premier circuit de détection de niveau (32) est fixée à une valeur supérieure à celle dudit deuxième circuit de détection de niveau (34).

3. Circuit AGC suivant la revendication 1, dans lequel lesdits premier (32) et deuxième (34) circuits de détection de niveau comprennent respectivement : un transistor (50,54) à travers lequel un courant électrique circule en accord avec le niveau de signal d'entrée ; et un condensateur (53,55) disposé en aval dudit transistor pour maintenir le potentiel en accord avec la grandeur du courant qui circule à travers le transistor.

4. Circuit AGC suivant la revendication 3, dans lequel ledit circuit d'addition (36) comprend deux transistors (52,56) dont la grandeur du courant encirculation est déterminée en accord avec le potentiel amont du condensateur desdits premier et deuxième circuits de détection de niveau, et l'amont desdits deux transistors est couplé pour permettre le passage du courant additionné.

5. Circuit AGC suivant la revendication 1,dans lequel ledit premier circuit de détection de niveau (32) comprend en outre :

un transistor (50) à travers lequel des courants électriques circulent en fonction du niveau de signal d'entrée ;
un condensateur (53) disposé en aval dudit transistor pour maintenir le potentiel en fonction de la grandeur du courant dudit transistor ; et
un circuit de source d'énergie de base (60) pour maintenir la grandeur du courant qui circule à travers ledit transistor (50).

6. Circuit AGC suivant la revendication 5, dans lequel ledit circuit de compensation AGC (64) comprend un transistor de compensation et la grandeur du courant qui circule à travers celui-ci est déterminée en fonction de la sortie du signal-mètre (42) : et

la tension de sortie de ladite source d'énergie de référence est modifiée en fonction de la valeur du courant du transistor de compensation.

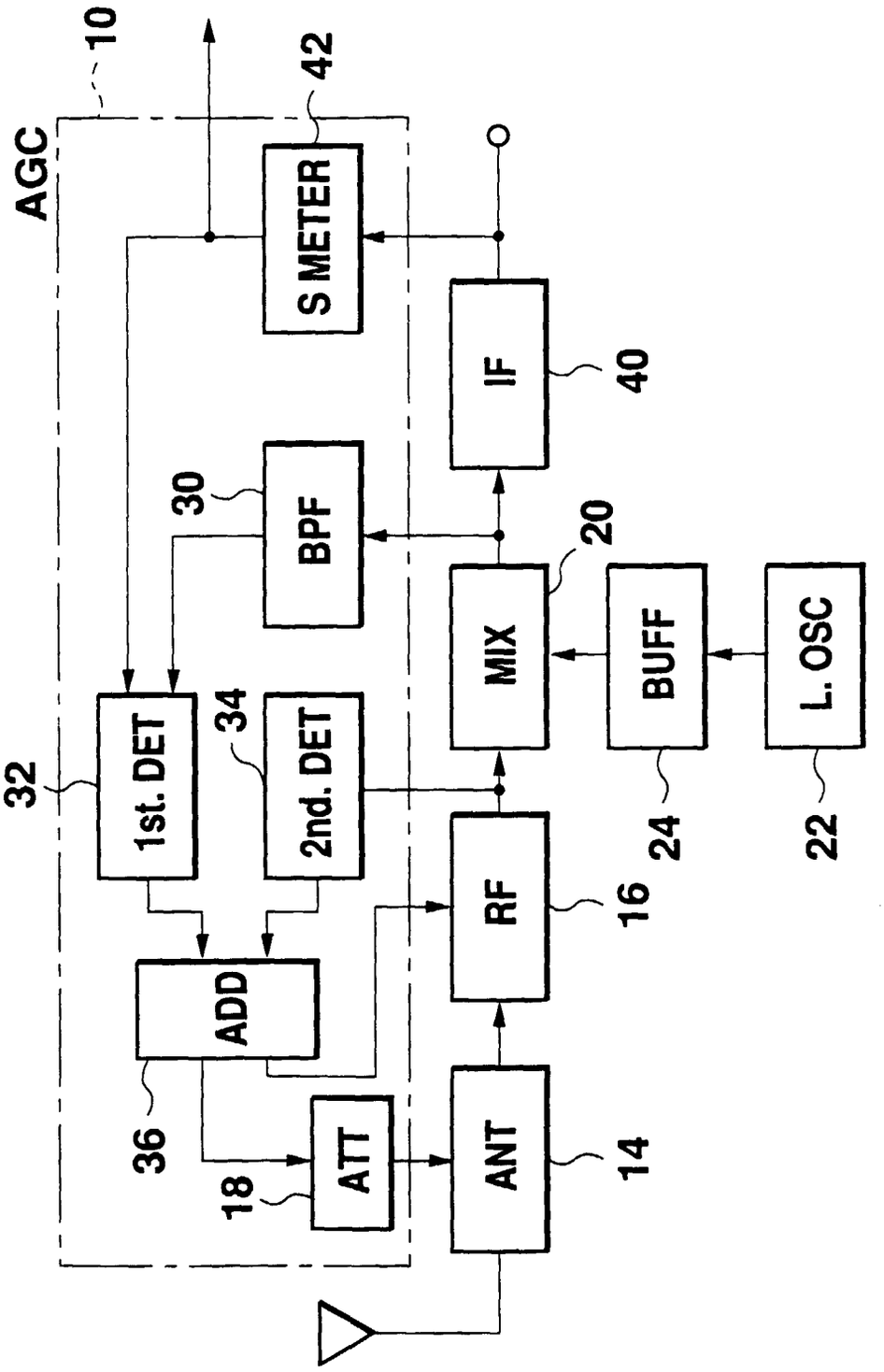

AGC
10
42
S METER
IF
40
30
BPF
20
MIX
BUFF
L. OSC
32
1st. DET
34
2nd. DET
RF
16
24
22
ADD
36
18
ATT
ANT
14

Fig. 1

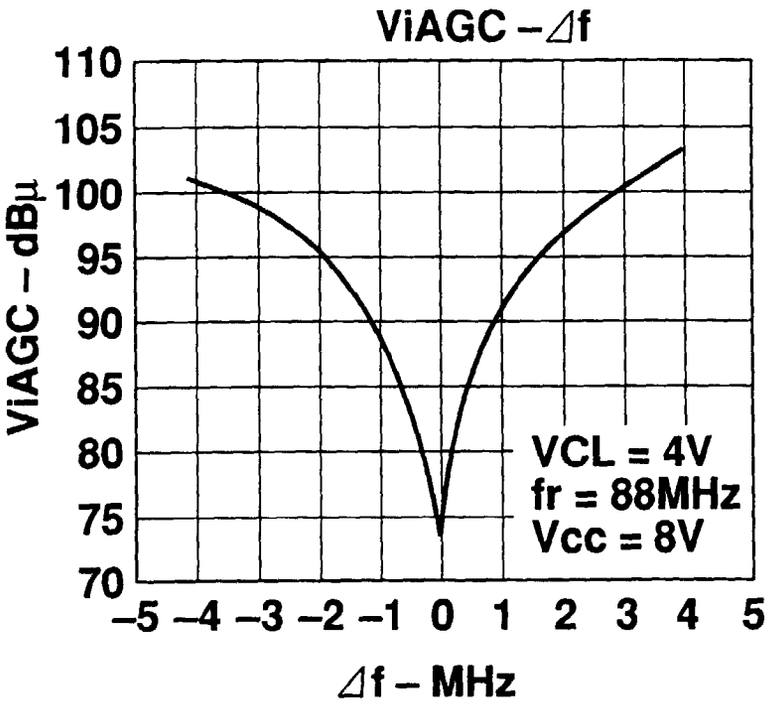

ViAGC – Δf
110
105
100
95
90
85
80
75
70
ViAGC – dBμ
VCL = 4V
fr = 88MHz
Vcc = 8V
–5 –4 –3 –2 –1 0 1 2 3 4 5
Δf – MHz

Fig. 2

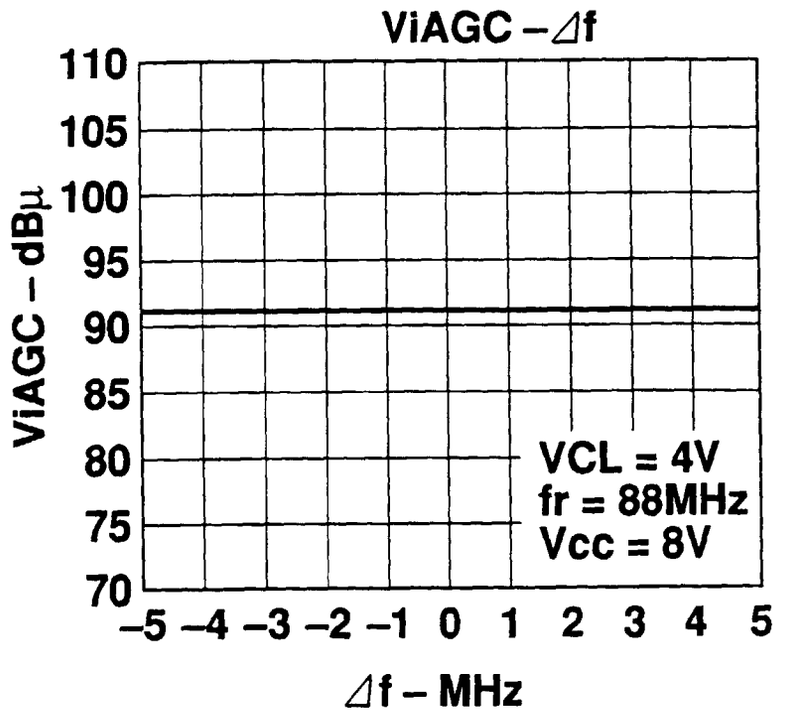

ViAGC – Δf
110
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85
80
75
70
ViAGC – dBμ
VCL = 4V
fr = 88MHz
Vcc = 8V
–5 –4 –3 –2 –1 0 1 2 3 4 5
Δf – MHz

Fig. 3

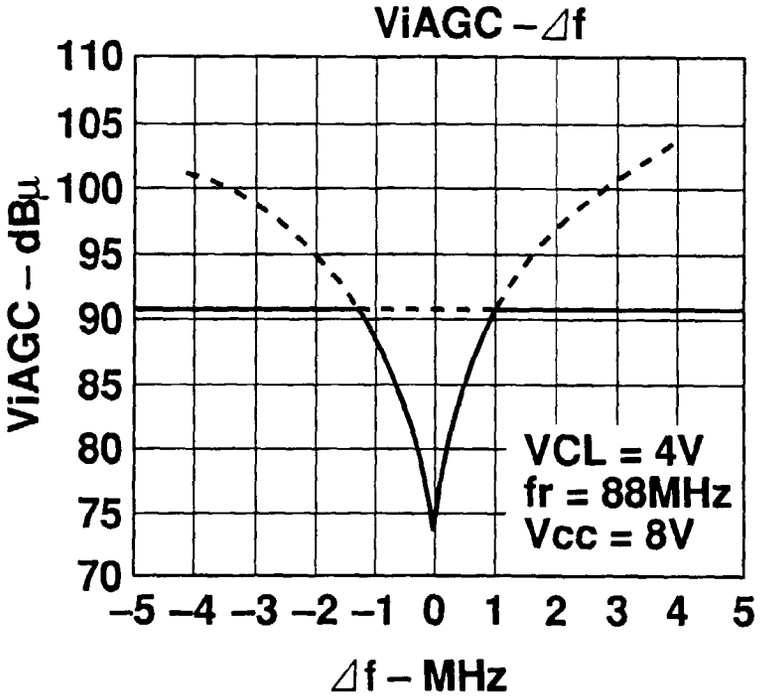

ViAGC – ⊿f
110
105
100
95
90
85
80
75
70
ViAGC – dBμ
VCL = 4V
fr = 88MHz
Vcc = 8V
–5 –4 –3 –2 –1 0 1 2 3 4 5
⊿f – MHz

Fig. 4

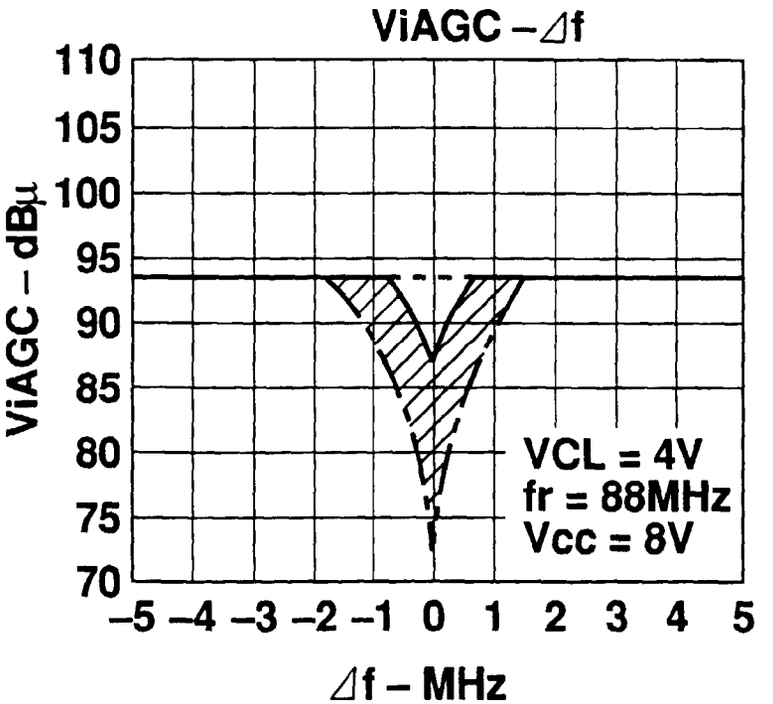

ViAGC – ⊿f
110
105
100
95
90
85
80
75
70
ViAGC – dBμ
VCL = 4V
fr = 88MHz
Vcc = 8V
–5 –4 –3 –2 –1 0 1 2 3 4 5
⊿f – MHz

Fig. 5

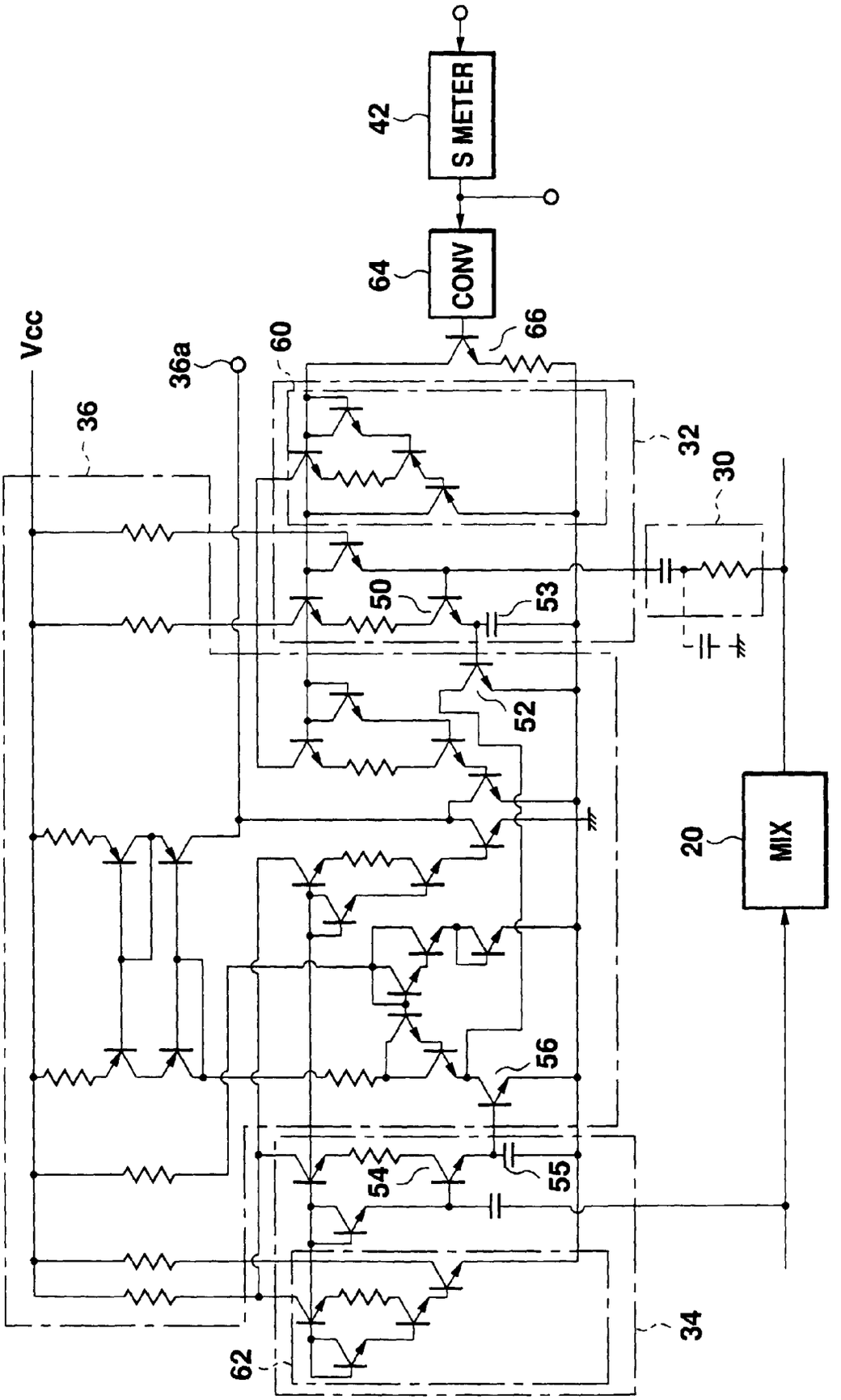

S METER
42
CONV
64
66
Vcc
36a
60
36
32
30
50
53
52
MIX
20
56
54
55
34
62

Fig. 6

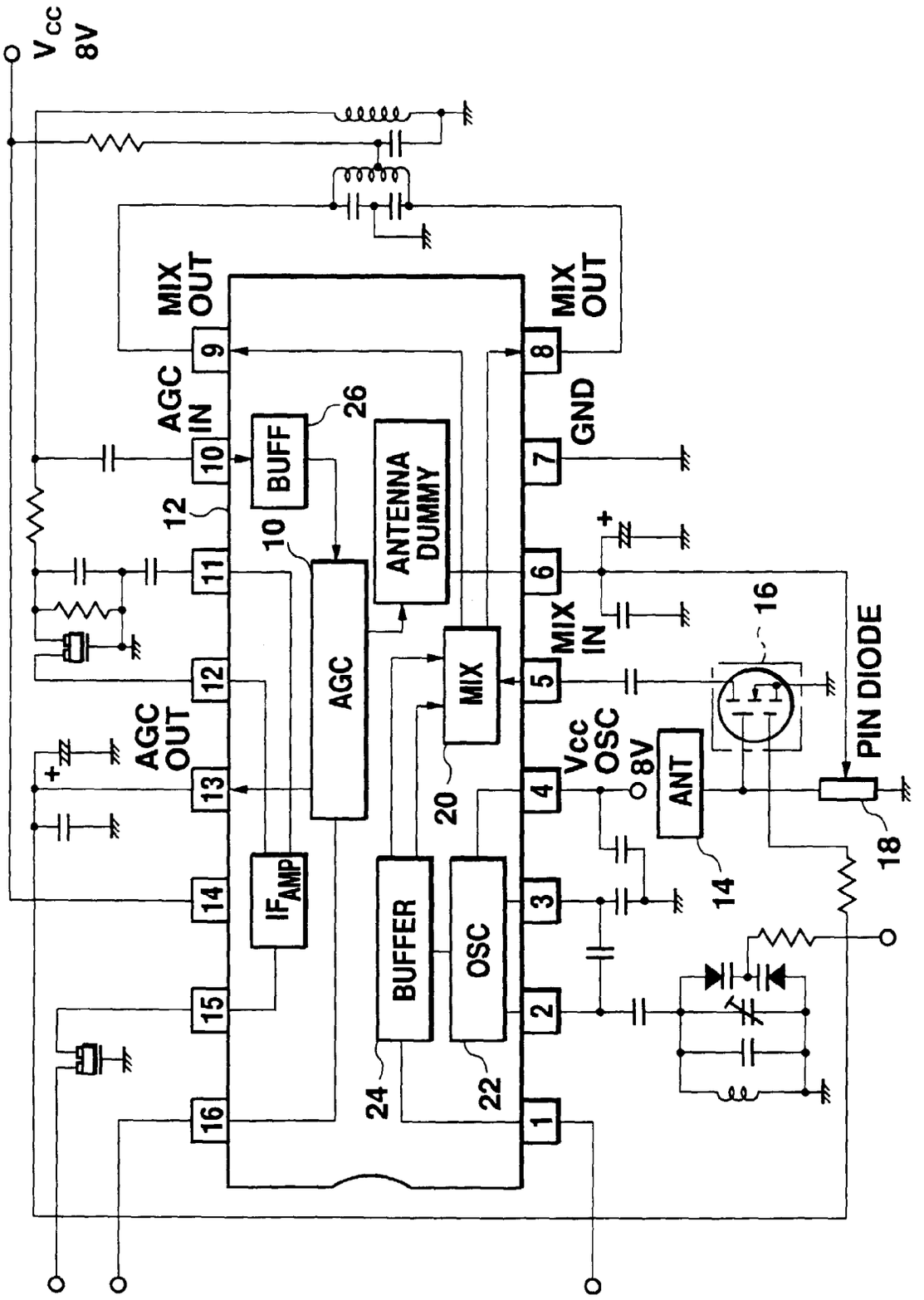

Vcc
8V
MIX OUT
MIX OUT
AGC IN
GND
BUFF
26
ANTENNA DUMMY
12
10
AGC
MIX
MIX IN
16
AGC OUT
Vcc OSC
8V
ANT
PIN DIODE
20
IFAMP
BUFFER
OSC
14
18
24
22
9
8
10
7
11
6
12
5
13
4
14
3
15
2
16
1

Fig. 7

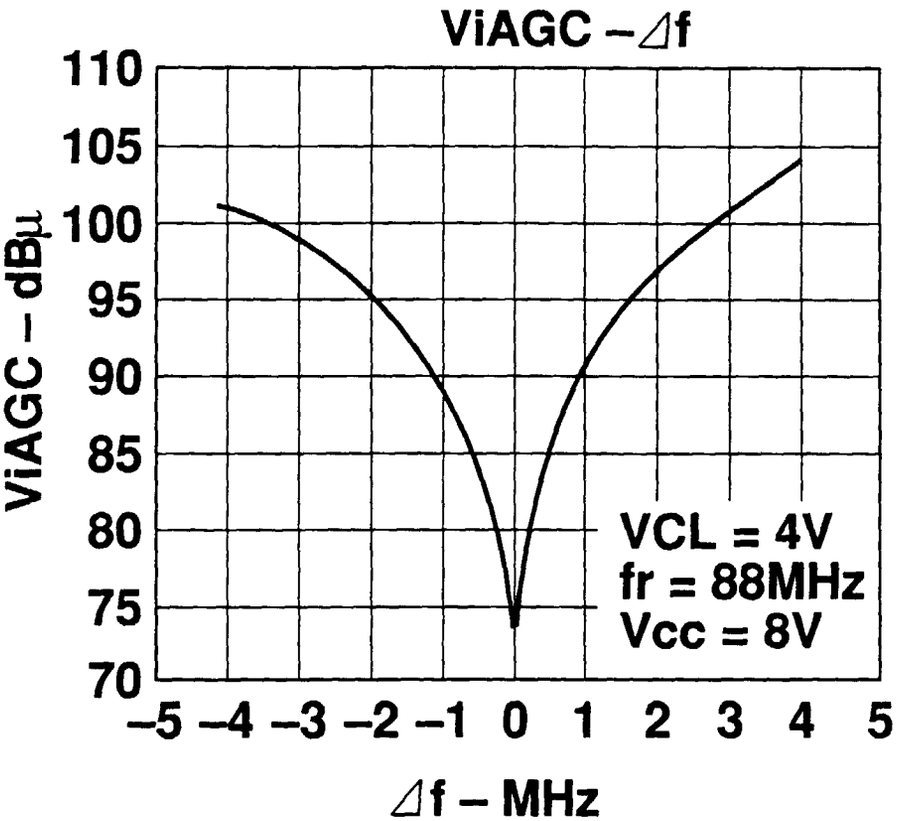

ViAGC – Δf
110
105
100
95
90
85
80
75
70
ViAGC – dBμ
–5 –4 –3 –2 –1 0 1 2 3 4 5
Δf – MHz
VCL = 4V
fr = 88MHz
Vcc = 8V

Fig. 8