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(12) # EUROPEAN PATENT APPLICATION

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(54) **Integrated circuit with co-integrated power supply reduction.**

(57) An integrated circuit has an internal supply voltage with a positive temperature coefficient, as a result of which the switching rate and the nuisance caused by "hot carrier stress" are less sensitive to temperature.

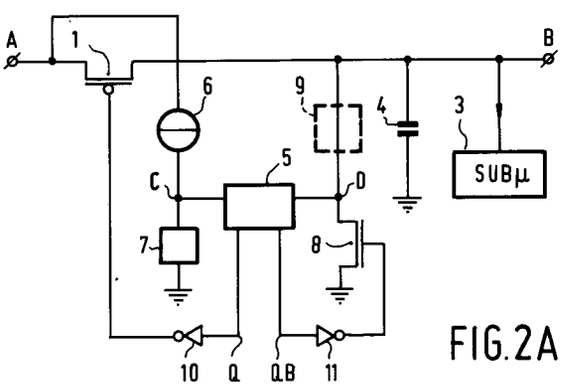

FIG.2A

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The invention relates to a circuit, having an external supply voltage junction point and an internal supply voltage junction point and a voltage converter arranged between said junction points, for connecting to the internal supply voltage junction point an internal supply voltage which is lower than the supply voltage across the external junction point.

Such a circuit is disclosed in the Netherlands patent application 8701472. Since the dimensions of transistors and other components of an integrated circuit are getting increasingly smaller, also the distances across which voltages of the order of the supply voltage occur become increasingly smaller. This results in high electric field strengths which produce *inter alia* what is commonly denoted "hot carrier stress" in, for example, field effect transistors. For reasons of reliablity it is therefore necessary to use a supply voltage lower than the standard 5V supply voltage for MOS components having, for example, channel lengths less than 1 μm (so-called submicron components). The prior art integrated circuit has an external (5 V) and an internal supply voltage junction point, between which a voltage converter is arranged which repeatedly charges a parasitic capacitance which is connected in parallel with the internal supply voltage junction point. This capacitance is used as a current supply for the integrated circuit. The voltage converter includes a detector circuit which, in dependence on the voltage across the internal supply voltage junction point and with a certain hysteresis switches an electronic switch on or off which is arranged between the internal and the external supply voltage junction point. This known integrated circuit has the drawback that the rate of the circuit and the occurring nuisance of hot carrier stress highly vary with temperature.

The invention has *inter alia* for its object to provide an integrated circuit whose mode of operation (the switching rate and the sensitivity to hot carrier stress in particular) is temperature-dependent to a lesser extent. To that end, an integrated circuit in accordance with the invention, is characterized in that the voltage converter is arranged for generating an internal supply voltage having a positive temperature coefficient.

Fundamentally, the invention is based on the recognition that the switching rate of a circuit and also the hot carrier stress decrease *versus* an increasing temperature, whilst the switching rate of a circuit and also the hot carrier stress increases *versus* an increasing internal supply voltage. An integrated circuit according to the invention, in which at an increasing temperature also the internal supply voltage increases, consequently provides, at temperature changes, a substantially constant switching rate and a substantially constant hot carrier stress. The above-mentioned effects then substantially cancel each other, whilst they actually intensify each other at a negative temperature coefficient. A temperature coefficient having a value between +1.5 mV/K and +6 mV/K proved to be advantageous.

The invention will now be described in greater detail on the basis of embodiments and with reference to the accompanying Figures, in which:

Figure 1 shows a prior art integrated circuit and

Figure 2 shows an integrated circuit of the invention.

Before the invention will be described with reference to the Figures, the background of the invention will first be described. For reasons of reliability it is necessary to use a supply voltage (for example 3.3 V) which is lower than the standard supply voltage (of 5 V) for MOS components having channel lenghts less than, for example, 1 μm. More specifically in large static random access memories from 256 kbits upwards, in which memory cells formed by six CMOS-transistors arranged in a memory matrix and having a channel length of not more than 0.7 μm are used, a co-integrated supply voltage reduction is required. Other circuit-technical solutions are not used, as then the cell surface area would become too large.

In Figure 1 A denotes the external supply voltage junction point (carrying a voltage VD of, for example, 5 V) and B denotes the internal supply voltage junction point (carrying a voltage VI of, for example, 3.3V). Interposed between them is a voltage converter, comprised of an electronic switch, in this case a PMOS- power switching transistor 1, and a detector circuit, more specifically a detector amplifier 2, which has its detection input connected to the internal supply voltage junction point B and its output to the control input of the electronic switch, in Figure 1 the control electrode of transistor 1. The integrated (parasitic) circuit capacitance 4, which may for example have a value of 3 nF in the case of a 256 kbits SRAM, is repeatedly recharged *via* transistor 1, more specifically when the detector 2 detects that voltage VI across internal supply voltage junction point B has decreased to below a predetermined threshold value. Then transistor 1 is turned on and capacitance 4 is recharged until detector 2 detects that voltage VI has increased to above a further threshold value. The difference in these threshold values corresponds to the hysteresis of detector 2. In this manner the inevitable parasitic capacitance 4 is used to supply submicron components 3 with current.

When MOS-transistors having small channel lengths (in the submicron range) or small oxide thicknesses are used in integrated circuits, there is a risk of "hot carrier stress" occurring. Namely,

when the channel length of transistors decreases, the maximum permitted voltage difference over the drain-source path gets smaller. A decrease in the supply voltage (of, for example, 5 V to 3.3 V), reduces the sensitive to hot carrier stress, but also leads to circuits with a lower operating rate.

Generally, it is desirable to have an internal supply voltage available which is as constant as possible and more specifically, is independent of temperature. At an increasing temperature the rate at which a circuit operates generally decreases, as do also the negative effects of hot carrier stress (see the article "Hot-carrier and wear-out phenomena in submicron VSLI's" by E. Takeda, Processing VSLI-Symposium 1985, pages 2-5). When the internal voltage increases, then however the rate of a circuit increases, and also the nuisance caused by hot carrier stress. If now an internal supply voltage is used having a temperature coefficient around zero or negative, then the influence of the temperature on the operating rate and the sensitivity to hot carrier stress of a circuit is not compensated for, and is even intensified for the case of a negative temperature coefficient.

The voltage converter, which is described in the Netherlands patent application 8701472, has an internal supply voltage which depends on several times the threshold voltage of the transistors plus the voltage swing. The threshold voltages decrease with increasing temperature, and this provides a negative temperature coefficient for the internal supply voltage. A circuit fed *via* this voltage converter is therefore very sensitive to temperature as regards its operating rate and the nuisance caused by hot carrier stress.

Figure 2 shows an integrated circuit in accordance with the invention. The same reference symbols are used to denote the same components shown in Figure 1. Figure 2A illustrates a reference voltage source 6, connected to the external supply voltage, which produces a constant current and is connected to ground *via* resistor 7. The current source is connected *via* junction point C to an input of a comparator circuit 5 which is known *per se* and whose other input is connected to junction point D which optionally is connected to junction point B *via* a voltage reducer 9. One (non-inverting) output Q of the comparator circuit 5 is connected *via* an inverting element 10, for example a standard CMOS inverter, to the control electrode of switch 1, the other (inverting) input QB is fed back to junction point D *via* a further inverting element 11 and hysteresis transistor 8. A differential amplifier, or, for example, an n-channel amplifier stage arranged in series with a p-channel amplifier stage can be used as the comparator circuit 5. Resistor 7 can be realised by arranging, for example, three n-channel MOS-transistors in series, their gates being connected to junction point C to which also the drain of the first transistor is connected, the source of the third transistor being connected to ground. Current source 6 is based on a PTAT (Proportional To Absolute Temperature) voltage source, as described in, for example, the article "A new CMOS current reference" by W. Sansen, F. op 't Eynde and M. Steyaert, Digest of the ESSCIRC 1987, pages 125-128. By using such a current source, which is known *per se*, a reference voltage VR having a positive temperature coefficient of, for example, 4.5 mV/K is generated at junction point C. The value of the reference voltage VR across junction point C is preferable chosen to be one threshold voltage lower than internal supply voltage VI, to have current source 6 and comparator circuit 5 function in their optimum working range. To that end also the voltage across junction point D is reduced by one threshold voltage relative to VI, using voltage reducer 9. The latter may, for example, as shown in Figure 2B, be in the form of a p-channel MOS-transistor, whose source is connected to junction point B and whose gate and drain are interconnected, this drain being connected to the drain of an n-channel MOS-transistor, whose gate is connected to the external supply voltage and whose source is connected to ground. The reference voltage VR with positive temperature coefficient is applied to the comparator circuit 5, which now, by feedback to junction point D, induces a voltage which also has a positive temperature coefficient, so that also the internal supply voltage VI across junction point B gets a positive temperature coefficient of, for example, 3.2 mV/K, with all the advantages mentioned in the foregoing.

Claims

1. A circuit, having an external supply voltage junction point and an internal supply voltage junction point and a voltage converter connected between said junction points, for connecting to the internal supply voltage junction point an internal supply voltage which is lower than the supply voltage across the external junction point, characterized in that, the voltage converter is arranged for generating an internal supply voltage having a positive temperature coefficient.

2. A circuit as claimed in Claim 1, characterized in that the voltage converter includes an electronic switch connected between the said junction points for periodically charging a circuit capacitance connected to the internal supply voltage junction point, means for generating a reference voltage having a positive temperature coefficient as well as a detector circuit for

switching the switch on or off in dependence on the internal supply voltage and the reference voltage.

3. A circuit as claimed in Claim 2, characterized in that, the means include a reference current source, in which a PTAT voltage source is employed.

4. A circuit as claimed in any one of Claims 1 to 3, characterized in that, the value of the temperature coefficient of the internal supply voltage is located between +1.5 mV/K and +6 mV/K.

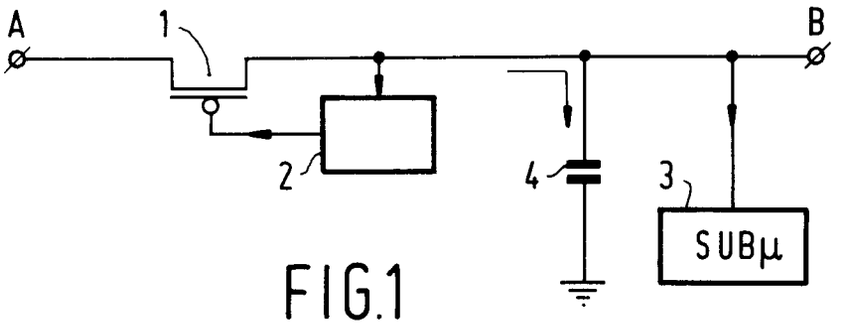

FIG.1

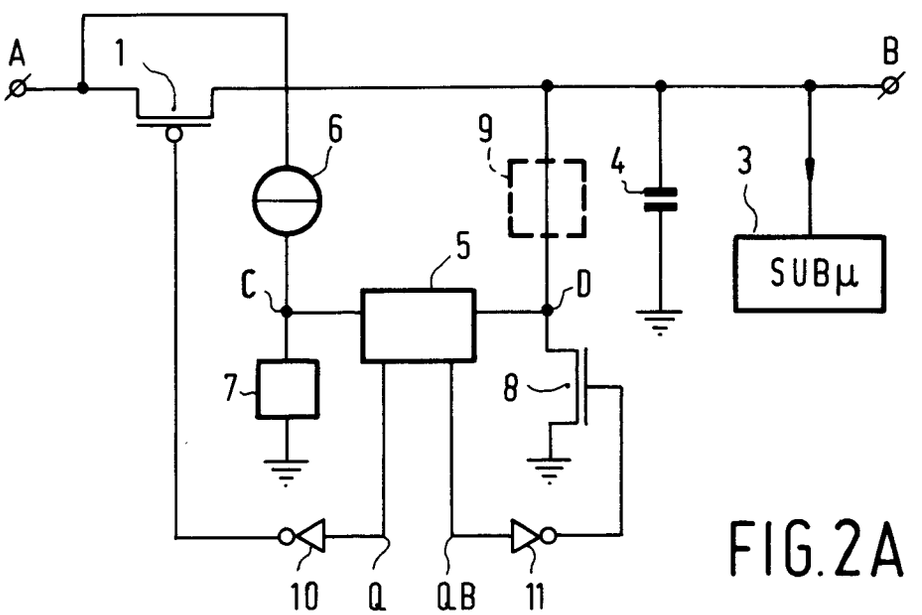

FIG.2A

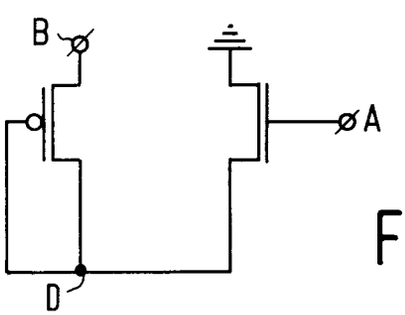

FIG.2B

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EUROPEAN SEARCH REPORT

Application Number

EP 91 20 1582

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X,Y	US-A-4 723 108 (MURPHY & PUGH) * column 1, last paragraph *	1,2,3	G 05 F 1/625
X	US-A-4 298 835 (ROWE) * column 1, lines 35 - 55; figure *	1	
D,Y	EP-A-0 296 681 (PHILIPS) * abstract; figure 1 *	2	
D,Y	Digest of the ESSCIRC 1987, & Steyaert: "A New CMOS Current Reference" * page 126, lines 13 - 32; figure 2 *	3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 05 F

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	12 September 91	VAN DEN DOEL J.C.

CATEGORY OF CITED DOCUMENTS

- X : particularly relevant if taken alone
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