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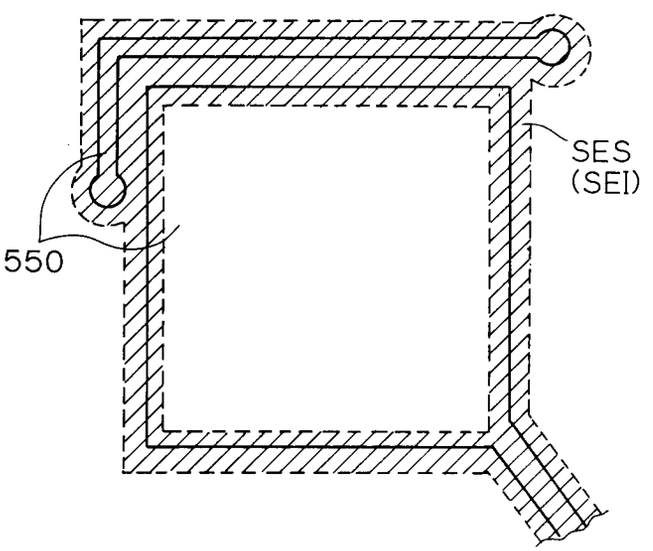
(54) Method of and device for inspecting pattern of printed circuit board.

(57) An objective printed circuit board to be inspected has a printed conductive pattern (550) thereon. The image of the objective printed board is read with an image reader to obtain an image singal. Prior to the image reading of the objective printed board, a reference printed board of the same type as the objective printed board is prepared, and the image thereof is read with the image reader. An edge image of a conductive pattern on the reference printed board is extracted and enlarged to generate an enlarged edge image (SEI). In inspection of the objective printed board, only areas belonging to the enlarged edge image are actually inspected and other areas are not subjected to the inspection.

FIG. 7C



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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of and a device for inspecting a pattern of a printed circuit board, and more particularly to a technique in which an inspection mode is selected depending on locations of pattern defects on the printed circuit board.

Description of the Background Art

Printed circuit boards are employed in the field of electronic engineering for mounting and interconnecting electronic elements, and are provided with conductive wiring patterns on one or both sides of insulating boards and with a large number of through holes piercing the insulating boards. Various types of optical visual inspection devices or pattern inspection devices have been employed in order to inspect whether or not the conductive pattern and the through holes are formed accurately within a tolerance.

Fig. 16 of the accompanying drawings is a partial plan view showing an exemplary conductive pattern which is provided on a printed board, and this conductive pattern includes wiring patterns 901, lands 902, shielding portions 903 for electrostatically shielding mounted electronic parts. Through holes (not shown) are formed in the respective lands 902. An optical pattern inspection device reads images of the conductive pattern and the through holes, to perform pattern inspection of the printed board on the basis of the images. A conductive pattern to be inspected may be a mixed pattern, which is provided with a source or grounding conductive pattern and a signal wiring pattern in a multilayer printed board, as well as an SMT (Surface Mount Technology) lead terminal pattern illustrated in Fig. 16.

A conventional pattern inspection device is so structured as to perform inspection for the entire surface of a board according to a single inspection rule. Therefore, pinholes exceeding a prescribed size, for example, are judged as "defects" regardless of their locations on the board surface.

Even if the defects on the board are of the same type, however, degrees of importance on quality control are varied with locations thereof. For example, even a fine defect is liable to become a critical defect for the printed board in a wiring area 910 of Fig. 16, while no fine defect exerts a significant influence on the quality of the printed board in a central area 911 of the shielding portion 903. Thus, printed boards which are judged as defective by a conventional pattern inspection device include those usable as nondefectives, such as that having a fine defect only in the aforementioned central area 911. Therefore, a complicated operation is required in order to confirm whether printed boards being judged as defective are non-usable defectives or usable defects which may be regarded as nondefectives, leading to a low throughput of the entire inspection processing.

SUMMARY OF THE INVENTION

The present invention is directed to a method of inspecting an objective printed board having a conductive pattern thereon.

According to the present invention, the method comprises the steps of: (a) obtaining an image of the objective printed board, wherein the image includes an image of the conductive pattern; (b) extracting an edge of the conductive pattern from the image of the conductive pattern or from an image substantially equivalent to the image of the conductive pattern, to generate an edge image; (c) enlarging the width of respective portions of the edge image to generate an enlarged edge image; (d) determining first and second areas in the image of the objective printed board, wherein the first area coincides with the enlarged edge image and the second area is an area other than the first area in the image of the objective printed board; and (e) inspecting the first area of the image of the objective printed board in a first inspection mode and inspecting the second area of the image of the objective printed board in a second inspection mode different from the first inspection mode.

In an aspect of the present invention, prepared is a reference printed board which is of the same type as the objective printed board having a conductive pattern previously judged as nondefective. The image of the reference printed board is read prior to the image reading of the objective printed board to obtain the edge image in the step (b) from the image of the reference printed board.

In a preferred embodiment of the present invention, only the first area is actually inspected and the second area is not subjected to the inspection.

Alternatively, an image of a mask film for forming the objective printed board may be utilized, or design data of the printed board may be utilized for performing edge extraction.

The term "the image substantially equivalent to the image of the conductive pattern" in the present invention is generic and encompasses these images or image data.

Preferably, regions where mini via holes exist are removed from the enlarged edge image.

The present invention also provide a device suitable for performing the present method.

The selection or switching of inspection modes in the present invention includes the following

cases:

(1) ON-OFF Switching

An inspection is actually performed in an ON-mode, while no inspection is performed in an OFF mode.

(2) Inspection Condition Switching

The degree of strictness in inspection is changed depending on whether the objective area belongs to the enlarged edge image. The Inspection Condition Switching includes switching of the maximum allowable diameters of pinholes in two ways, for example.

(3) Inspected Item Switching

Inspected items are switched depending on whether the objective area belongs to the enlarged edge image. The Inspected Item Switching includes switching of performing hole breakout inspection in enlarged edge images and alternatively performing inspection of pinholes in non-edge regions, for example.

The present invention is based on the fact that defects caused in areas around edges of a conductive pattern are important for quality control. In addition to wiring patterns, defects around edges of shielding portions etc. are liable to relate to other defects in later steps of board fabrication, and may accompany reduction of reliability. According to the present invention, such areas are grasped as "enlarged edge images" by combination of edge extraction means and edge enlarging means. In an image of the printed board, different inspection modes are selectively employed in enlarged edge regions defined by the enlarged edge images and other non-edge regions, thereby enabling suitable pattern inspection in consideration of portions causing defects.

Accordingly, an object of the present invention is is to provide pattern inspection method and device for a printed board which can detect pattern defects while distinguishing areas having high degrees of importance on quality control from other areas and improve the throughput of the entire inspection processing by omitting or simplifying a confirming operation following the detection of pattern defects.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a partially fragmented plan view showing an optical inspection device for a printed board according to a preferred embodiment of the present invention;

Fig. 1B is a partially fragmented side elevational view of the device shown in Fig. 1A;

Fig. 2 illustrates an exemplary printed board;

Fig. 3 is a typical side elevational view showing an optical head employed in the preferred embodiment;

Fig. 4 is a block diagram showing the overall electrical structure of the preferred embodiment;

Figs. 5(a) and 5(b) are explanatory diagrams for binarization of a print pattern and through holes;

Fig. 6A is an internal structural diagram of an inspection circuit unit;

Fig. 6B is an explanatory diagram for signals produced in a pre-processing circuit;

Fig. 6C illustrates an exemplary circuit structure for filling-up processing;

Fig. 6D is a block diagram showing the internal structure of an enlarged edge image generation circuit;

Figs. 7A to 7C, 8A to 8C and 9A and 9B are explanatory diagrams for processes of generating enlarged edge images;

Fig. 10 is a circuit structure diagram showing an edge extraction circuit;

Fig. 11 is a circuit structure diagram showing an edge enlarging circuit;

Figs. 12A to 12D illustrate exemplary structures for selecting an inspection mode by a control signal;

Fig. 13 is a partial diagram showing another preferred embodiment of the present invention;

Fig. 14 is an explanatory diagram of a 3 x 3 space operator;

Figs. 15A and 15B illustrate circuits corresponding to the 3 x 3 space operator shown in Fig. 14; and

Fig. 16 is a diagram for illustrating a pattern on a printed board.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

< A. Structure >

Fig. 1A is a plan view, with portions broken away, of a printed circuit board inspection device 10 according to a preferred embodiment of the present invention, and Fig. 1B is a side view thereof. The device 10 comprises a lower housing 11 and an upper housing 12. The lower housing 11 is provided with a horizontally movable table 13 in the vicinity of an opening on the top surface thereof. The movable table 13 includes a rectangular frame 14 and a glass plate 15 mounted in the rectangular

frame 14. The bottom surface 15a of the glass plate 15 is frosted or coarsely ground. A printed circuit board 20 is placed on the top surface 15b of the glass plate 15 and is supported by the glass plate 15.

With reference to Fig. 2, the printed circuit board 20 includes an insulative base plate 21 made of glass epoxy and printed patterns or conductive patterns 22 of copper formed on both surfaces thereof by means of screen printing technique or photo-etching technique. The printed pattern 22 has wiring pattern portions 23, lands 24, and a shield portion 27. Each of the lands 24 is formed therein with a through hole 25 which pierces or penetrates through the printed circuit board 20. The through holes 25 are classified into two types, normal through holes 25t and mini via holes 25m. The normal through holes 25t, having a relatively large diameter, are used for mounting electronic elements and for connecting the electronic elements to the conductive patterns 22. The mini via holes 25m, having a relatively small diameter,are used for electrical connection between the both surfaces of the insulative base plate 21. The inner wall surfaces of the through holes 25t and 25m are plated with conductive metal.

Reference is made again to Figs. 1A and 1B. The frame 14 is slidable on a pair of guide rails 16. A ball screw 17 extends in the direction parallel to the guide rails 16. A nut 19 fixed to the frame 14 is coupled with the ball screw 17. When a motor 18 turns the ball screw 17, the movable table 13 moves in the horizontal (±Y) directions.

An image reading system 50 is provided in the upper housing 12. An optical head array 100 extending in the horizontal (±X) directions is disposed in a space over the mid portion of the image reading system 50. The optical head array 100 includes eight optical heads H0 to H7, which are supported at equal intervals by a supporting member 101. The supporting member 101 is slidable on a guide member 102 in the (±X) directions. The guide member 102 is fixed to a pair of side frame members 51a and 51b. The supporting member 101 is coupled to a motor 103 through a nut (not shown) and a ball screw 104. When the motor 103 is driven, the optical heads H0 to H7 can move in the (±X) directions together with the supporting member 101.

A light source 120 for "transmitted illumination" is disposed under the optical heads H0 to H7, where "transmitted illumination" is defined as illumination applied to an object and transmitting through holes formed in the object. The light source 120 is composed of a large number of infrared LEDs arranged in the (±X) directions, and serves substantially as a linear light source. The light source 120 is supported from the side frames 51 through supporting rods 121 and 122. Each of the optical heads H0 to H7 has a light source 110 for "reflected illumination", which light source 110 is attached to the bottom thereof. "Reflected illumination" is defined as illumination applied to an object and reflected at the surface of the object. The light source 110 includes three pairs of one-dimensional arrays of red LEDs extending in the (±X) directions.

Presser roller mechanisms 200A and 200B are provided on opposite sides of the optical head array 100 in order to press the printed circuit board 20 fed thereunder. The presser roller mechanisms 200A and 200B are operable to prevent the out-of-position and flexure of the printed circuit board 20.

A data processor 300 for performing various data processings and operation controls is disposed in the upper housing 12.

< B. Overall Operation >

Prior to the description of the detailed structure of the inspection device 10, the overall operation of the device 10 will be discussed hereinafter. Initially, the printed circuit board 20 is placed on the glass plate 15 as shown in Figs. 1A and 1B. When an operation switch is manually operated, the motor 18 is forwardly rotated so that the printed circuit board 20 moves in the (+Y) direction together with the movable table 13. The light sources 110 and 120 light up.

Then, the printed circuit board 20 reaches the position of the image reading system 50 with the movement of the table 13. The optical heads H0 to H7 read the images of the printed patterns 22 (of Fig. 2) illuminated by the reflected illumination from the light source 110, while reading the images of the through holes 25 illuminated by the transmitted illumination from the light source 120.. Respective image readings are conducted for each scanning line schematically defined on the printed circuit board 20.

Since there are gaps between the visual fields of the respective optical heads H0 to H7 arranged in line, the whole image on the surface of the printed circuit board 20 cannot be read through a movement of the printed circuit board 20 in the (+Y) direction. After the movement of the printed circuit board 20 in the (+Y) direction, the motor 103 is driven to move the optical heads H0 to H7 in the (+X) direction. The distance of the movement in the (+X) direction is the half of the mutual arrangement pitch of the optical heads H0 to H7. After this movement, the motor 18 is reversely rotated. Accordingly, the printed circuit board 20 moves in the (-Y) direction, while the optical heads H0 to H7 read the remaining parts of the images of the wiring patterns 22 and the through holes 25.

As a result, both scans indicated by the solid arrows A1 and the the broken arrows A2 of Fig. 1A are carried out, whereby the image reading throughout the surface of the printed circuit board 20 can be accomplished. The images detected are given to the data processor 300, in which whether the printed patterns 22 and the through holes 25 are defective or not is decided on predetermined criteria.

< C. Details of Optical Heads >

Fig. 3 is a schematic side view of the internal structure of the optical head H0. Although Fig. 3 shows only the optical head H0, the other optical heads H1 to H7 have the same structure.

The light source 110 for reflected illumination is composed of a light source 111 for regular reflection and light sources 112 and 113 for irregular reflection. Each of the light sources 111, 112 and 113 is substantially a linear light source composed of a one-dimensional array of red LEDs which generate red light of wavelength λ_1 (= 600 to 700 nm).

Light from the light sources 111, 112 and 113 are applied to an area-to-be-inspected or objective area AR of the top surface of the printed circuit board 20 which is currently located just under the optical head H0.

The light source 120 for transmitted illumination is composed of a one-dimensional array of infrared LEDs which generate infrared light of wavelength λ_2 (= 700 to 1000 nm). The light source 120 projects the infrared light in the (+Z) direction toward an area corresponding to the reverse side of the area AR in the printed circuit board 20.

Part of the red light generated in the light sources 111, 112 and 113 for reflected illumination reaches the area AR and is reflected at the area AR. Part of the infrared light from the light source 120 for transmitted illumination reaches the through holes 25 and passes through the through holes 25. The reflected light and the transmitted light thus obtained are directed to the optical head H0 as a spatially superposed compound light.

As shown in Fig. 3, the compound light passes through an image-formation lens system 140 and impinges on a cold mirror 150. The cold mirror 150 transmits only infrared rays. The red light (i.e., the reflected light LR from the surface of the printed circuit board 20) included in the compound light is reflected at the mirror 150 to the (+Y) direction so that an image is formed on a photo-detecting surface of a first CCD linear image sensor 161. The infrared light (i.e., the transmitted light LT through the through hole 25) included in the compound light passes through the mirror 150 so that an image is formed on a photo-detecting surface of a second CCD linear image sensor 162.

Each of the CCD linear image sensors 161 and 162 has CCD photo-electric cells arranged one-dimensionally in the (±X) directions. The first linear image sensor 161 detects the one-dimensional image of the surface of the printed circuit board 20 illuminated by the reflected illumination. The second linear image sensor 162 detects the one-dimensional image of the through hole 25 illuminated by the transmitted illumination. The movement mechanism shown in Figs. 1A and 1B moves the printed circuit board 20 and the optical head array 100 relatively, thereby each area of the printed circuit board 20 being scanned. The two-dimensional images of the wiring pattern 22 and the through hole 25 for each area can be obtained.

< D. Electric Structure and Operation >

< D-1. Overall Structure >

Fig. 4 is a block diagram of the overall electric structure of the preferred embodiment. A/D converters 301 receive wiring pattern image signals PS_0 - PS_7 and through hole image signals HS_0 - HS_7 from the optical heads H0 to H7, respectively, to convert them into digital signals. The digital signals are transmitted to circuits 304 each composed of binarizing circuits 302 and 303.

The binarizing circuits 302 and 303 compare the digitized image signals PS_0 and HS_0 with predetermined threshold values TH1 and TH2 (see Fig. 5) to output binarized signals, respectively. The binarized signals are at a logical "H" level when the levels of the signals PS_0 and HS_0 are higher than the threshold values TH1 and TH2, while they are at a logical "L" level when the levels of the signals PS_0 and HS_0 are lower than the threshold values TH1 and TH2, respectively. The binarizing circuits 302 and 303 corresponding to the other optical heads H1 to H7 have the same structure.

The binarized image signals thus obtained are transmitted to a pattern inspection system 400. The pattern inspection system 400 includes eight inspection circuit units 400a to 400h corresponding to the optical heads H0 to H7. The units 400a to 400h construct the two-dimensional images of the printed patterns 22 and the through holes 25 based on the image signals which are supplied from the optical heads H0 to H7 and digitalized in the circuits 302 or 303. The units 400a to 400h are operable to decide whether the printed patterns 22 and the through holes 25 are defective or not on predetermined criteria.

The data processor 300 further comprises a control circuit 310. The control circuit 310 applies

turn on/off commands to the light sources 110 and 120 through lighting circuits 311 and 312, and outputs drive control signals to the motors 18 and 103. The motor 18 is equipped with a rotary encoder 18E, which detects a motor rotation angle signal. The motor rotation angle signal for ruling data processing timing is given to the control circuit 310.

The control circuit 310 includes a synchronization control circuit 314 for controlling the read timing of the linear image sensors 161 and 162 and the synchronization of the motors 18 and 103.

< D-2. Pre-processor >

Fig. 6A is a block diagram of the internal structure of the inspection circuit unit 400a. The other inspection circuit units 400b to 400h have the same structure.

The image signals PS and HS outputted from the binarizing circuits 302 and 303 are given to a pre-processor 500 as a pattern signal PS and a hole signal HS indicative of the two-dimensional images of the printed pattern 22 and the through hole 25, respectively. The pre-processor 500 generates various signals based on the pattern signal PS and the hole signal HS. Major ones among the various signals are as follows (see Fig. 6B):

(1) Corrected hole signal CHS

This signal CHS represents a corrected hole image having a diameter obtained by slightly enlarging the diameter of the through hole 25. The corrected hole signal CHS is generated in connection with detection of the inner wall of the through hole 25. Namely, the inner wall of the through holes 25 is plated with metal, and the inner wall is sometimes detected neither in the pattern signal PS nor in the hole signal HS. Hence, the hole signal HS is enlarged or corrected to close or compensate a gap caused between the signals PS and HS due to such an undetected portion. The corrected hole signal CHS includes a signal CHSt corresponding to the normal through hole 25t and a signal CHSm corresponding to the mini via hole 25m.

(2) Enlarged hole signal SHS

This signal SHS represents an image obtained by further enlarging the hole diameter represented by the corrected hole signal CHS. The enlarged hole signal SHS includes an enlarged normal through hole signal SHSt and an enlarged mini via hole signal SHSm.

(3) Compensated pattern signal CPS

This is a signal in which a blank portion (or the center portion of Fig. 5(a)) corresponding to the through hole 25 in the pattern signal PS is filled in with a logical level "H". The signal CPS is the logical summation of the corrected hole signal CHS and the pattern signal PS (see Fig. 6C). The signal CPS is also referred to as a "corrected pattern signal" hereinafter.

These signals are used for various purposes. There are shown in Fig. 6A only some of the signals outputted from the pre-processor 500 which are necessary for the following description.

<D-3. Inspection Circuit>

The inspection circuit unit 400a shown in Fig. 6A comprises the following two types of inspection circuits for pattern inspection:

(1) A DRC (design rule check) circuit 420

This circuit 420 is adapted to determine whether the printed board 20 is defective or nondefective by extracting characteristics of the pattern on the printed board 20 such as line widths, pattern angles and continuity, for example, and by determining whether or not these are out of designed values. Such a DRC method or a characteristic extraction method is disclosed in Japanese Patent Laying-Open Gazette No. 57-149905 (1982), for example.

(2) A comparative check circuit 430

This circuit 430 is adapted to compare image signals obtained from a previously prepared reference printed board with the image signals obtained from the printed board 20 to be inspected, and to specify different portions as defectives. The reference printed board is of the same type as the printed board 20 to be inspected and is previously determined as nondefective. This comparative method is disclosed in Japanese Patent Laying-Open Gazette No. 60-263807 (1985), for example.

Thus, since the device of the preferred embodiment requires information as to the reference printed board, the reference printed board is placed on the table 13 and its image is read before image reading is performed on the printed board 20 to be inspected. The signal CPS produced in the pre-processing circuit 500 in reading of the reference printed board is supplied to and stored in an image memory 410. Address generation timing control for this image memory 410 and a region memory 630 (Fig. 6D), which is described later, is performed by the synchronization control circuit 314 shown in Fig. 4.

<D-4. Extraction and Enlargement of Edge>

Among the signals obtained in the pre-processing circuit 500 (Fig. 6A), the compensated pattern signal CPS is supplied also to an enlarged edge image generating circuit 600. As shown in Fig. 6D, the circuit 600 comprises an edge extraction circuit 610, an edge enlarging circuit 620 and the region memory 630.

In connection with the operation of this circuit 600, Fig. 7A shows an exemplary print pattern on the reference printed board in the form of a partial plan view. This print pattern 550 has relatively narrow wiring patterns 552 and 553, in addition to a shielding portion or a copper solid portion 551. Through holes 555 are formed in lands 554. The corrected pattern signal CPS obtained by reading such a pattern is supplied to a flip-flop circuit 611 (Fig. 10) provided in the edge extraction circuit 610, and delayed in this circuit 611 by a time period corresponding to one pixel, to become a signal CPS_a. Then, the signals CPS and CPS_a are supplied to an exclusive OR (Ex. OR) gate 612. Fig. 8A is an enlarged view of a portion 560 of Fig. 7A. Regions expressed in solid and broken lines in Fig. 8A correspond to image regions represented by the signals CPS and CPS_a which are supplied to the Ex. OR gate 612 at the same point of time, respectively. "MAIN SCANNING" and "SUBSCANNING" indicate image scanning operations along the (±X) direction and the (±Y) direction in Fig. 1A respectively, and whether the directions are of "+" or "-" depends on the pixel reading directions of the CCD linear image sensors 161 and 162 and the direction of movement of the table 13. Oblique line portions in Fig. 8A represent deviation areas between the images expressed by the signals CPS and CPS_a. An output signal ES_a of the Ex. OR gate 612 expresses the deviation areas.

The corrected pattern signal CPS is also supplied to a one-scanning-line delay circuit 613 shown in Fig. 10, and delayed by this circuit 613 by a time period corresponding to one scanning line, to become a signal CPS_b. Then, the signals CPS and CPS_b are supplied to another Ex. OR gate 614. As shown in Fig. 8B, an output signal ES_b from this Ex. OR gate 614 expresses deviation areas between the signals CPS and CPS_b which are inputted in the Ex. OR gate 614 at the current point of time.

The respective output signals ES_a and ES_b of the two Ex. OR gates 612 and 614 are supplied to an OR gate 615, which in turn outputs a signal ES indicating the logical sum thereof. As shown in Figs. 8C and 7B, the signal ES is an edge signal expressing each edge or contour line of the print pattern 550. An edge image EI expressed by this edge signal ES has a finite width. As shown in Figs. 8A to 8C, the edge image IE may have a width of two or more pixels due to combination of the signals ES_a and ES_b as to an edge obliquely extending with respect to each scanning direction, while the edge image EI has a width of one pixel in other edges.

The edge signal ES thus obtained is supplied to multistage connection of one-line delay circuits 621 which are provided in the edge enlarging circuit 620 (Fig. 11). Assuming that n represents a prescribed positive integer, the number of the one-line delay circuits 621 is (2n - 1). Respective delay outputs of these (2n - 1) one-line delay circuits 621 and the edge signal ES are supplied to an OR gate 622, which obtains a logical sum signal ESL thereof. As shown in Fig. 9A, this logical sum signal ESL expresses an image obtained by enlarging the edge image EL by 2n pixels in the subscanning direction.

This signal ESL is supplied to (2n-1) multistage connection of flip-flop circuits 623, where each circuit 623 has a delay function for one pixel. Respective outputs of these flip-flop circuits 623 and the signal ESL are supplied to an OR gate 624. As shown in Fig. 9B, an output signal SES of the OR gate 624 expresses an image SEI which is obtained by enlarging the edge image EI by 2n pixels in both the main scanning direction and the subscanning direction respectively. The enlarged edge signal SES is supplied to the region memory 630 (Fig. 6D), so that the enlarged edge image SEI expressed by this signal SES is stored in this region memory 630. The center of the line width of the enlarged edge image SEI is deviated from the center of the edge image EL by n pixels in both of the main scanning direction and the subscanning direction. However, it is possible to compensate for this deviation by delaying read timing by n pixels in reading of the enlarged edge image SEI from the image memory 630. Fig. 7C shows the entire enlarged edge image SES as to the print pattern 550 shown in Fig. 7A.

<D-5. Inspecting Operation>

After the aforementioned processing for the reference printed board is completed, the reference printed board provided on the table 13 is replaced by the printed board 20 to be inspected, and image reading is started as to this board 20. The signal CPS outputted from the preparation circuit 500 of Fig. 6A is supplied to the DRC inspection circuit 420 and the comparative check circuit 430. In synchronization with this operation, the corrected pattern signal CPS as to the reference printed board, which has been stored in the image memory 410, is read and supplied to the comparative check circuit 430.

The DRC inspection circuit 420 and the comparative check circuit 430 execute respective inspection processing on the basis of respective input signals, and output inspection result signals INS_a and INS_b.

On the other hand, the enlarged mini via hole signal SHS_m from the pre-processing circuit 500 is supplied to a logical composite circuit 450. In synchronization with this operation, the enlarged edge signals SES are read from the region memory 630 (Fig. 6D) sequentially along scanning lines, and supplied to the logical composite circuit 450. The logical composite circuit 450 obtains the logical sum of the enlarged mini via hole signal SHS_m and the enlarged edge signals SES, thereby generating an inspection control signal CONT. The inspection control signal CONT goes "H" in areas (hereinafter referred to as "important inspection areas") on the enlarged edge images SEI having no mini via holes 25m while going "L" in other areas. This inspection control signal CONT is supplied to inspection circuits 420 and 430, thereby selecting one inspection mode for the important inspection areas and selecting another inspection mode for other areas. Such elimination of the mini via holes 25m from the important inspection areas is related to the fact that no electronic components are mounted in the mini via holes 25m. Namely, the mini via holes 25m are provided in order to electrically connect the upper side and the lower side of the board 20 with each other by the plating layers formed on inner wall portions thereof, and hole breakout is allowed to some extent so far as such connection is maintained. Therefore, the mini via holes 25m may be elimiated from the important inspection areas.

Figs. 12A to 12D show exemplary structures for such selection of respective inspection modes. Figs. 12A to 12D representively express both of the inspection circuits 420 and 430, and contents of "processors" and "input image signals" in Figs. 12A to 12D are different between the inspection circuits 420 and 430. Further, while Figs. 12A to 12D show hardware type "processors" in order to facilitate understanding, it is also possible to implement functions substantially equivalent thereto with software programs. The control signal CONT is used as an enable signal for a processor 421 in the example shown in Fig. 12A, so that the processor 421 is enabled only on the important inspection areas. Therefore, the device enters an inspection inhibiting mode in areas other than the important inspection areas. As the result, signal levels indicating "no defects" are given to inspection result signals INS_a (INS_b) in the areas other than the important inspection areas.

Fig. 12B shows such an example that selection of an inspection executing mode or the inspection inhibiting mode depending on the type of areas is performed using an OR gate 422. The result of the inspection meaning "no defects" is indicated when inspection result signals INS_a (INS_b) are at a logical "H" level. The control signal CONT is at a logical "H" level on important inspection areas, while the same is at a logical "L" level on the areas other than the important inspection areas.

In the structure shown in Fig. 12C, a plurality of inspecting condition data defining different inspecting conditions are previously registered in a condition register 423. The different inspecting conditions include a relatively strict inspecting condition and a relatively loose inspecting condition. The relatively strict inspecting condition is a criterion such that printed boards having even small defects are regarded as defective ones, while the relatively loose inspecting condition is such that printed boards having only large defects are regarded as defective ones. In the important inspection areas, the data representing the relatively strict inspecting condition is read from the register 423 in response to the control signal CONT, and supplied to the processor 421. In areas other than the important inspection areas, on the other hand, the data representing the loose inspection condition is read from the register 423 and supplied to the processor 421. The processor 421 performs pattern inspection under an inspection mode defined by the inspecting condition thus supplied. Through this operation, a plurality of inspection modes defined by the respective inspection conditions are selectively employed for each area to be inspected.

In an example shown in Fig. 12D, provided are a plurality of processors 421a and 421b operable to conduct inspections corresponding to different inspection items respectively. One of the processors 421a and 421b is selectively enabled depending on the level of the inspection signal CONT. Therefore, one of the inspection items is selected depending on whether the area to be inspected belongs to the important inspection areas or not.

As described above, one of the inspection modes is selectively employed for the important inspection areas and other areas in respective examples according to the preferred embodiment. Thus, it is possible to selectively inspect in detail peripheral areas of pattern edges, which are important on quality control. Therefore, defects having low degrees of importance, such as pinholes in central regions of shielding patterns of a print pattern, are automatically neglected. Thus, it is possible to omit or simplify an operation for confirming the defects in a later step, whereby the throughput of the overall inspection processing is improved.

<Other Embodiments>

(1) The enlarged edge images SEI can also be

obtained from a pattern image of the printed board 20 to be inspected. While the print pattern 22 on the printed board 20 may have defects, regions or areas requiring detailed inspection can be covered with the enlarged edge images so far as the edge enlarge width 2n is set at a relatively large value. Preferably, the edge enlarge width 2n is set at about 1 to 2 mm in real size on the printed board 20, for example.

In the device of this preferred embodiment having a transmitted light source, it is also possible to read the pattern on a mask film employed for forming the printed board 20 and to obtain enlarged edge images SEI on the basis of the pattern image.

(2) When the pattern on the printed board 20 is designed with a CAD, it is also possible to obtain enlarged edge images SEI using the CAD data. In this case, the CAD data are inputted using an input unit 671, as shown in Fig. 13. A selector 672 is adapted to switch the input thereof between respective output signals CPS_0 and CPS of the input unit 671 and a pre-processing circuit 500, and output the selected one to an image memory 410, an enlarged edge image producing circuit 600 and the like. Before the image of the printed board 20 to be inspected is read, a filled-up pattern image signal CPS_0 produced from the CAD data is supplied to the image memory 410 and the enlarged edge image generating circuit 600. The enlarged edge image generating circuit 600 generates an enlarged edge signal SEI on the basis of this signal CPS_0, thereby defining important inspection areas.

(3) The edge extraction circuit 610 can also be structured using a space operator. For example, a 3 x 3 space operator OP shown in Fig. 14 is made to act on respective pixels while sequentially matching its center OP_{22} with respective centers of pixels on the printed board. When a logical level which is different from the logical level at the central operator OP_{22} is obtained in at least one of other operators OP_{11} to OP_{21} and OP_{23} to OP_{33} as a result of applying the space operator to respective pixels, the pixel of the central operator OP_{22} is recognized as one of edge pixels.

More particularly, signals S_{11} to S_{33} are produced by combination of one-line delay circuits 166 and flip-flop circuits 167 as shown in Fig. 15A. Then, the signals S_{11} to S_{33} are inputted in a combined circuit of an Ex. OR gate 168 and an OR gate 169 shown in Fig. 15B, to obtain an output signal ES of the OR gate 169 as an edge signal.

(4) The enlarged edge images SEI may be produced on the basis of the pattern image signal PS whose blank part is not yet filled up. Further, two image reading systems may be provided so that respective images of the printed board 20 to be inspected and the reference printed board can be simultaneously read.

The DRC inspection circuit 420 has such an advantage that defect contents can be specified, while the comparative check circuit 430 has such an advantage that a printed board having an arbitrary pattern can be inspected. Therefore, it is preferable to use both of these inspection circuits as in the aforementioned preferred embodiment, while the present invention is applicable with no dependence on the types of inspection circuits employed.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

The features disclosed in the foregoing description, in the claims and/or in the accompanying drawings may, both, separately and in any combination thereof, be material for realising the invention in diverse forms thereof.

Claims

1. A method of inspecting an objective printed board having a conductive pattern thereon, said method comprising the steps of:

(a) obtaining an image of said objective printed board, wherein said image includes an image of said conductive pattern;

(b) extracting an edge of said conductive pattern from said image of said conductive pattern or from an image substantially equivalent to said image of said conductive pattern, to generate an edge image;

(c) enlarging the width of respective portions of said edge image to generate an enlarged edge image;

(d) determining first and second areas in said image of said objective printed board, wherein said first area coincides with said enlarged edge image and said second area is an area other than said first area in said image of said objective printed board; and

(e) inspecting said first area of said image of said objective printed board in a first inspection mode and inspecting said second area of said image of said objective printed board in a second inspection mode different from said first inspection mode.

2. The method of claim 1, wherein

said conductive pattern of said objective

printed board is a first conductive pattern;

said edge of said conductive pattern is an edge of said first conductive pattern; and

the step (b) comprises the steps of:

(b-1) receiving an image of a reference printed board which is of the same type as said objective printed board and having a second conductive pattern previously judged as nondefective; and

(b-2) obtaining said edge of said first conductive pattern as a function of said image of the reference printed board, to generate said edge image.

3. The method of claim 1, wherein

a mask film is used to form said conductive pattern of said objective printed board; and

the step (b) comprises the steps of:

(b-3) obtaining said edge of said conductive pattern from data representing a mask pattern on said mask film.

4. The method of claim 1, wherein

said conductive pattern of said objective printed board is determined in accordance with pattern design data; and

the step (b) comprises the steps of:

(b-4) obtaining said edge of said conductive pattern from said pattern design data.

5. The method of claim 2, wherein:

the step (a) comprises the steps of:

(a-1) setting said reference printed board in an image reader;

(a-2) photoelectrically reading said image of said reference printed board with said image reader;

(a-3) replacing said reference printed board with said objective printed board in said image reader; and

(a-4) photoelectrically reading said image of said objective printed board with said image reader.

6. The method of claim 2, wherein:

the step (c) comprises the step of:

(c-1) storing said enlarged edge image in memory means; and

the step (d) comprises the step of:

(d-1) reading said enlarged edge image from said memory means to generate a signal indicative of said first area, which signal is employed in the step (e) to switch said first and second inspection modes.

7. The method of claim 6, wherein:

said objective printed board is provided with through holes having openings in said first conductive pattern;

said through holes are classified into first type through holes having a first diameter and second type through holes having a second diameter smaller than said first diameter; and

the step (a) further comprises the step of:

(a-5) obtaining first hole images representing said first through holes and second hole images representing said second through holes;

the step (d) further comprises the step of:

(d-2) obtaining logical summation of said enlarged edge image and said images of said second hole images to thereby generate said signal.

8. The method of claim 7, wherein:

the step (a-5) comprises the steps of:

(a-5-1) obtaining images of said first through holes and said second through holes; and

(a-5-2) enlarging said images of said first and second through holes to obtain said first and second hole images, respectively.

9. The method of claim 2, wherein:

the step (b-2) comprises the steps of:

(b-2-1) shifting said image of said reference board in a first direction to obtain a first shifted image;

(b-2-2) shifting said image of said reference board in a second direction to obtain a second shifted image; and

(b-2-3) obtaining a logical summation of said first and second shifted images to generate said edge image.

10. The method of claim 9, wherein:

the step (c) comprises the steps of:

(c-2) enlarging said edge image in said first direction to obtain a first enlarged image; and

(c-3) enlarging said first enlarged image in said second direction to obtain said enlarged edge image.

11. The method of claim 1, wherein:

said first inspection mode is such that said first area is inspected according to a predetermined inspection procedure; and

said second inspection mode is such that inspection of said second area is inhibited.

12. The method of claim 1, wherein:

said first inspection mode is such that said first area is inspected in relatively strict con-

dition for determining that said objective printed board is defective; and

said second inspection mode is such that said second area is inspected in relatively loose condition for determining that said objective printed board is defective.

13. The method of claim 1, wherein:

said first inspection mode is such that said first area is inspected for a first inspection item for determining that said objective printed board is defective; and

said second inspection mode is such that said second area is inspected for a second inspection item for determining that said objective printed board is defective.

14. A device for inspecting an objective printed board having a conductive pattern thereon, said device comprising:

(a) means for obtaining an image of said objective printed board, wherein said image includes an image of said conductive pattern;

(b) means for extracting an edge of said conductive pattern from said image of said conductive pattern or from an image substantially equivalent to said image of said conductive pattern, to generate an edge image;

(c) means for, enlarging the width of respective portions of said edge image to generate an enlarged edge image;

(d) means for determining first and second areas in said image of said objective printed board, wherein said first area coincides with said enlarged edge image and said second area is an area other than said first area in said image of said objective printed board; and

(e) means for inspecting said first area of said image of said objective printed board in a first inspection mode and inspecting said second area of said image of said objective printed board in a second inspection mode different from said first inspection mode.

15. The device of claim 14, wherein

said conductive pattern of said objective printed board is a first conductive pattern;

said edge of said conductive pattern is an edge of said first conductive pattern; and

said means (b) comprises:

(b-1) means for receiving an image of a reference printed board which is of the same type as said objective printed board and having a second conductive pattern previously judged as nondefective; and

(b-2) means for obtaining said edge of said first conductive pattern as a function of said image of the reference printed board, to generate said edge image.

16. The device of claim 14, wherein

a mask film is used to form said conductive pattern of said objective printed board; and

said means (b) comprises:

(b-3) means for obtaining said edge of said conductive pattern from data representing a mask pattern on said mask film.

17. The device of claim 15, wherein

said conductive pattern of said objective printed board is determined in accordance with pattern design data; and

said means (b) comprises:

(b-4) means for obtaining said edge of said conductive pattern from said pattern design data.

18. The device of claim 15, wherein:

said objective printed board is provided with through holes having openings in said first conductive pattern; and

said means (a) comprises:

(a-1) a horizontal transparent plate capable of holding said objective printed board thereon with a bottom surface of said objective printed board in contact with said transparent plate;

(a-2) first light source means provided above said transparent plate for illuminating a top surface of said objective printed board;

(a-3) second light source means provided under said transparent plate for illuminating said bottom surface of said objective printed board through said transparent plate; and

(a-4) means for photoelectrically reading said image of said reference printed board illuminated by said first and second light source means;

wherein a first light emitted from said first light source means is reflected at said top surface and is received by said means (a-4); and a second light emitted from said second light source means transmits through said through holes and is received by said means (a-4).

19. The device of claim 15, wherein:

said means (c) comprises:

(c-1) memory means for storing said enlarged edge image; and

said means (d) comprises:

(d-1) means for reading said enlarged edge image from said memory means to generate a signal indicative of said first area, which signal is employed in said means (e) to switch said first and second inspection modes.

20. The device of claim 19, wherein:

said objective printed board is provided with through holes having openings in said first conductive pattern;

said through holes are classified into first type through holes having a first diameter and second type through holes having a second diameter smaller than said first diameter; and

said means (a) further comprises:

(a-5) means for obtaining first hole images representing said first through holes and second hole images representing said second through holes;

said means (d) further comprises:

(d-2) means for obtaining logical summation of said enlarged edge image and said images of said second hole images to thereby generate said signal.

21. The device of claim 20, wherein:

said means (a-5) comprises:

(a-5-1) means for obtaining images of said first through holes and said second through holes; and

(a-5-2) means for enlarging said images of said first and second through holes to obtain said first and second hole images, respectively.

22. The device of claim 15, wherein:

said means (b-2) comprises:

(b-2-1) means for shifting said image of said reference board in a first direction to obtain a first shifted image;

(b-2-2) means for shifting said image of said reference board in a second direction to obtain a second shifted image; and

(b-2-3) means for obtaining a logical summation of said first and second shifted images to generate said edge image.

23. The device of claim 22, wherein:

said means (c) comprises:

(c-2) means for enlarging said edge image in said first direction to obtain a first enlarged image; and

(c-3) means for enlarging said first enlarged image in said second direction to obtain said enlarged edge image.

24. The device of claim 14, wherein:

said first inspection mode is such that said first area is inspected according to a predetermined inspection procedure; and

said second inspection mode is such that inspection of said second area is inhibited.

25. The device of claim 15, wherein:

said first inspection mode is such that said first area is inspected in relatively strict condition for determining that said objective printed board is defective; and

said second inspection mode is such that said second area is inspected in relatively loose condition for determining that said objective printed board is defective.

26. The device of claim 15, wherein:

said first inspection mode is such that said first area is inspected for a first inspection item for determining that said objective printed board is defective; and

said second inspection mode is such that said second area is inspected for a second inspection item for determining that said objective printed board is defective.

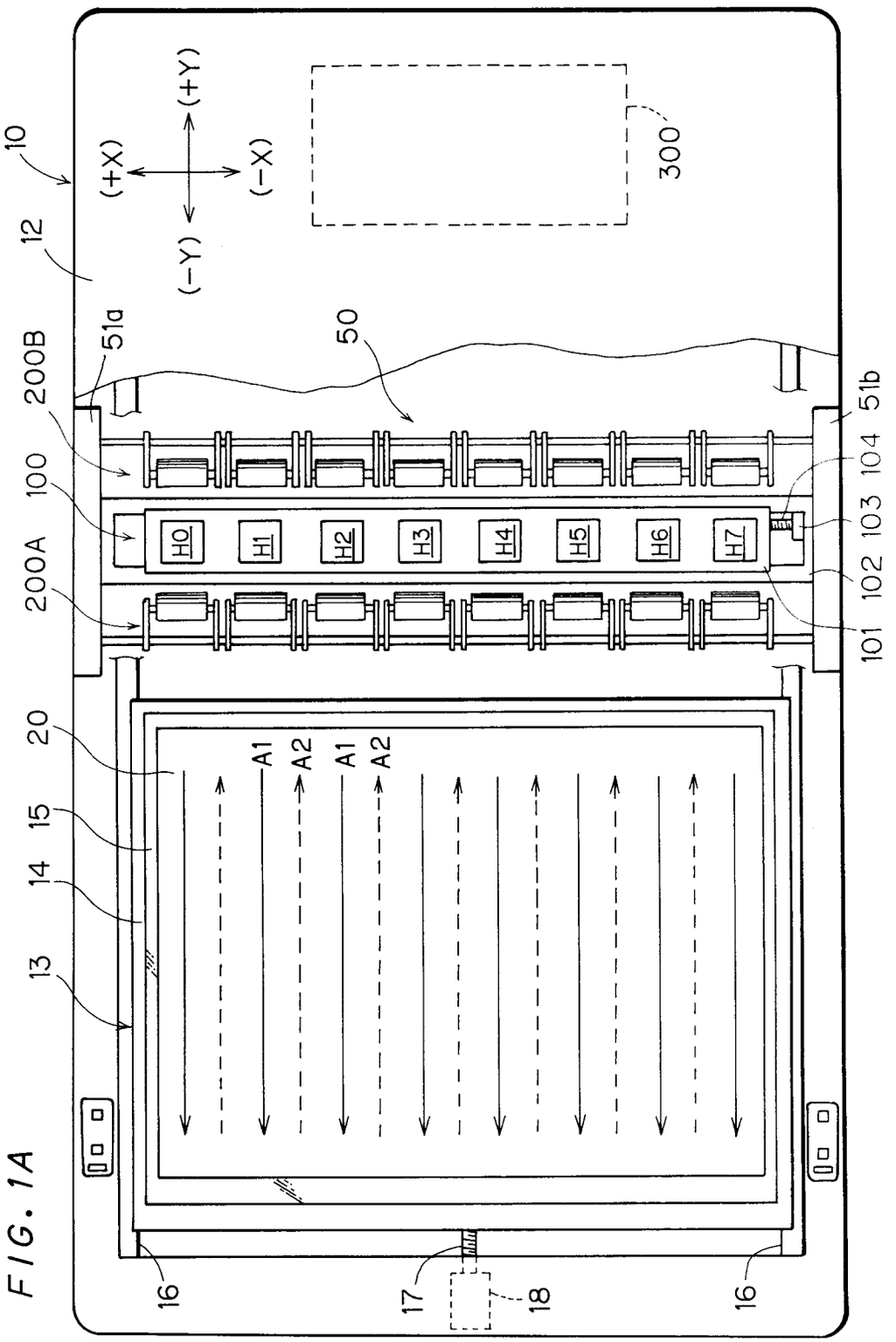
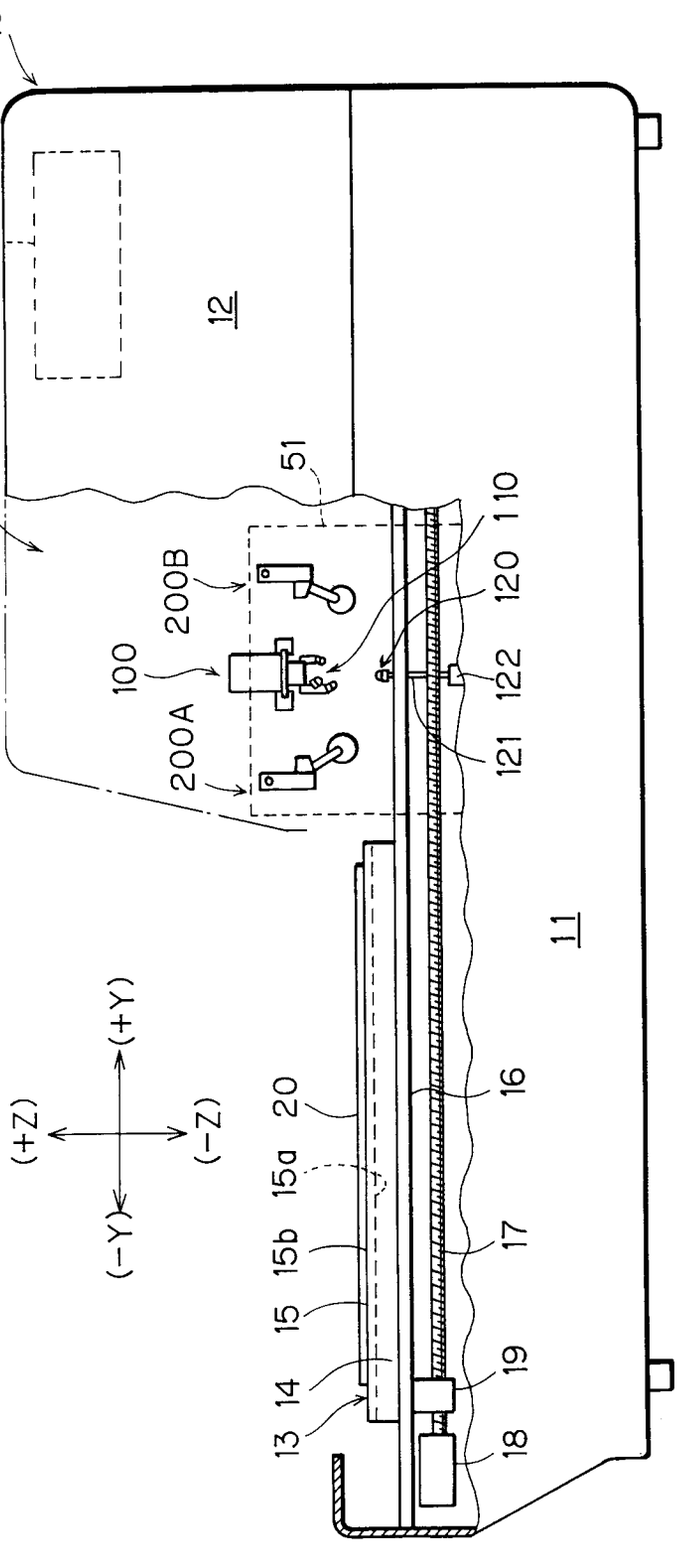

10
12
(+X)
(+Y)
(-X)
(-Y)
300
50
51a
51b
200B
200A
100
H0
H1
H2
H3
H4
H5
H6
H7
101
102
103
104
20
15
14
13
A1
A2
A1
A2
16
17
18
16

FIG. 1A

FIG. 1B


10
300
12
50
51
110
120
122
121
200B
100
200A
11
(+Y)
(+Z)
(-Z)
(-Y)
20
16
15a
15b
17
15
19
14
18
13

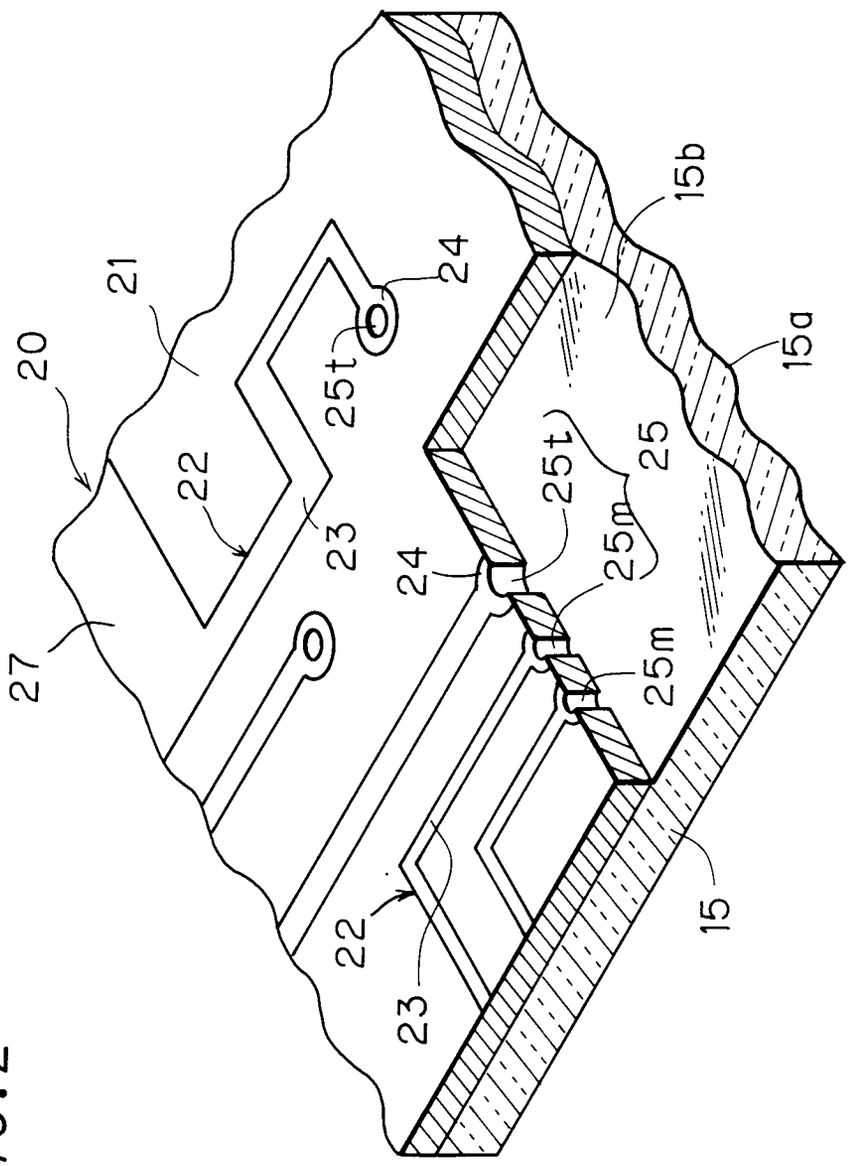
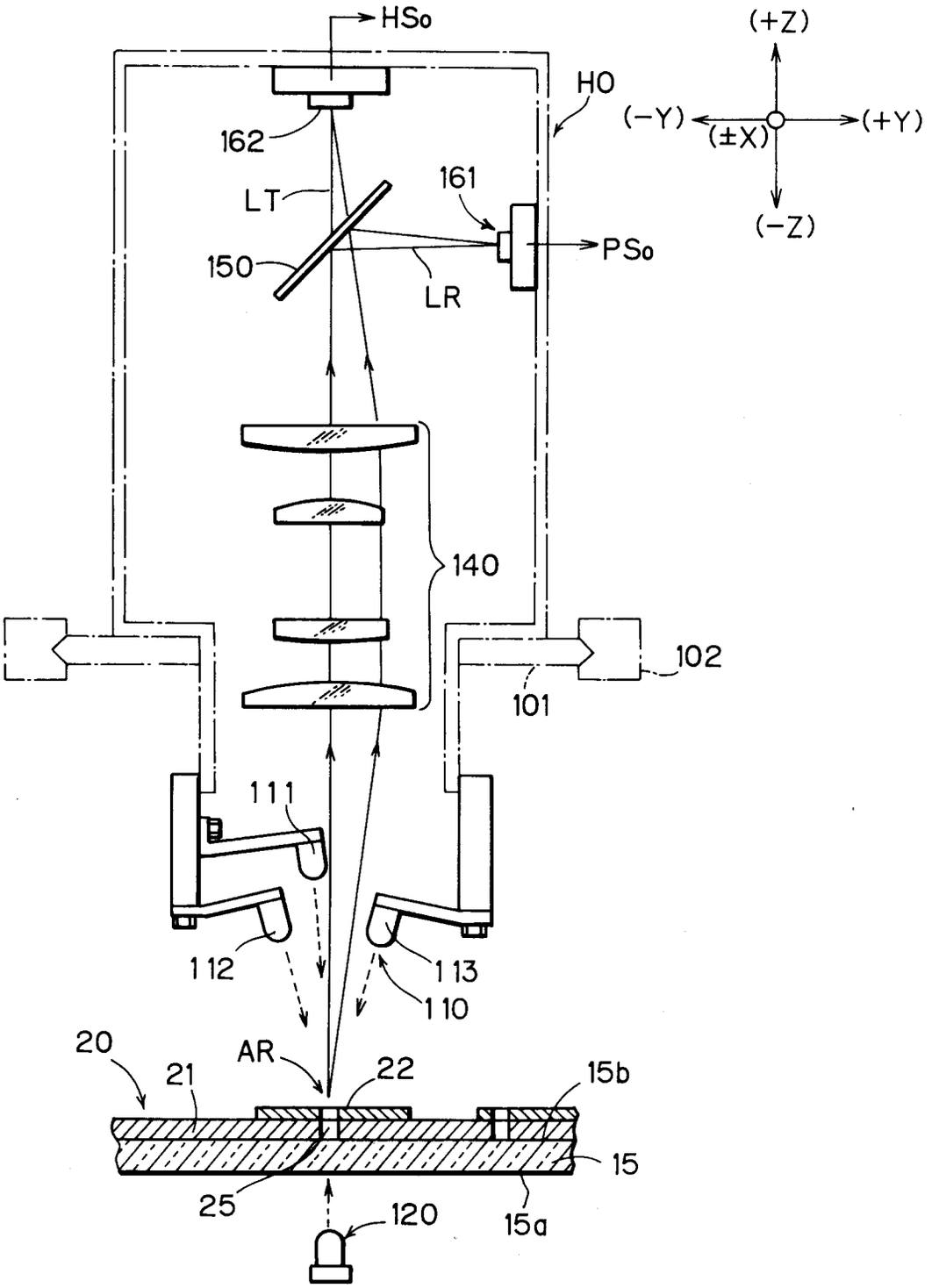


FIG.2

FIG. 3


HSo
HO
(+Z)
(-Y)
(±X)
(+Y)
(-Z)
162
161
LT
150
LR
PSo
140
102
101
111
112
113
110
20
21
AR
22
15b
15
25
120
15a

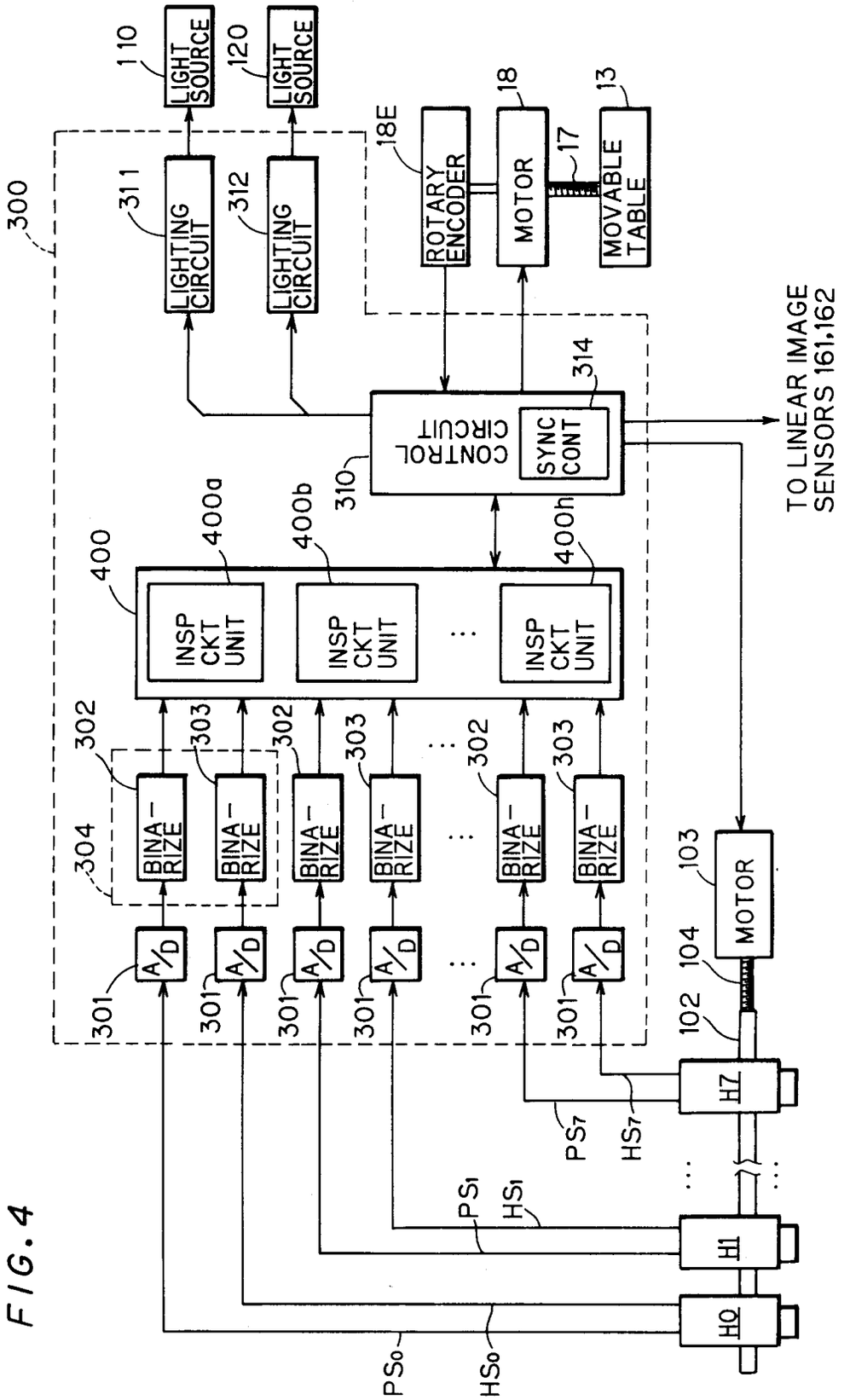

300
110
LIGHT SOURCE
120
LIGHT SOURCE
311
LIGHTING CIRCUIT
312
LIGHTING CIRCUIT
18E
ROTARY ENCODER
18
MOTOR
17
13
MOVABLE TABLE
314
SYNC CONT
CONTROL CIRCUIT
310
TO LINEAR IMAGE SENSORS 161,162
400
400a
400b
400h
INSP CKT UNIT
302
303
304
BINA-RIZE
301
A/D
103
MOTOR
104
102
H7
H1
H0
PS7
HS7
PS1
HS1
PS0
HS0

FIG. 4

FIG.5(a)

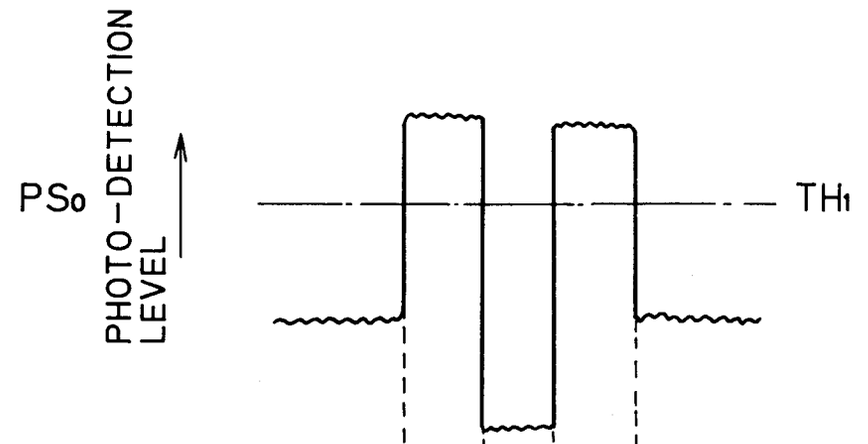

PSo
PHOTO-DETECTION LEVEL
TH1

FIG.5(b)

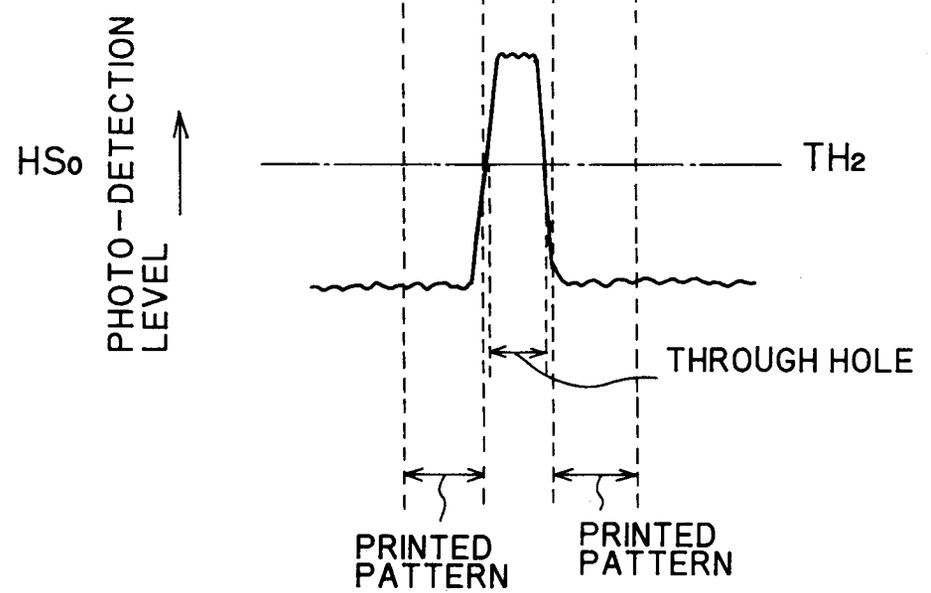

HSo
PHOTO-DETECTION LEVEL
TH2
THROUGH HOLE
PRINTED PATTERN
PRINTED PATTERN

FIG. 6A

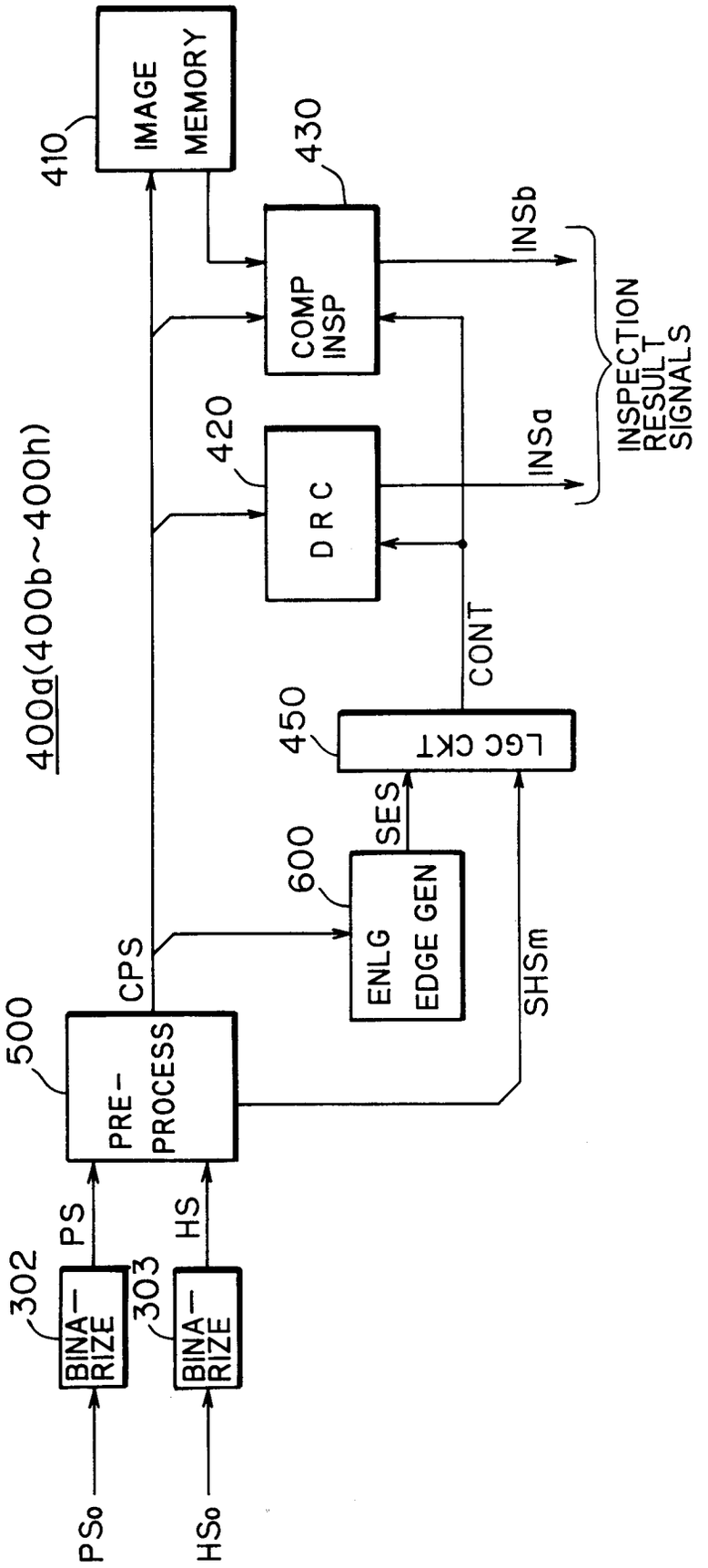

400a(400b~400h)
410
IMAGE MEMORY
430
COMP INSP
INSb
INSPECTION RESULT SIGNALS
420
D R C
INSa
CONT
450
LOGIC CKT
SES
600
ENLG EDGE GEN
SHSm
CPS
500
PRE-PROCESS
PS
HS
302
BINA-RIZE
303
BINA-RIZE
PSo
HSo

FIG. 6B

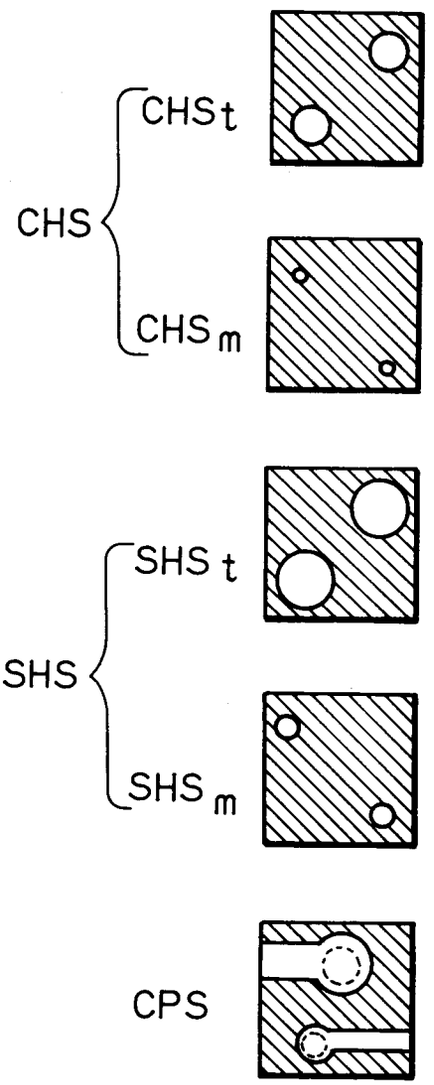


FIG. 6C

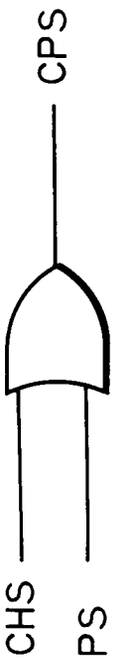

CPS
CHS
PS

FIG. 6D

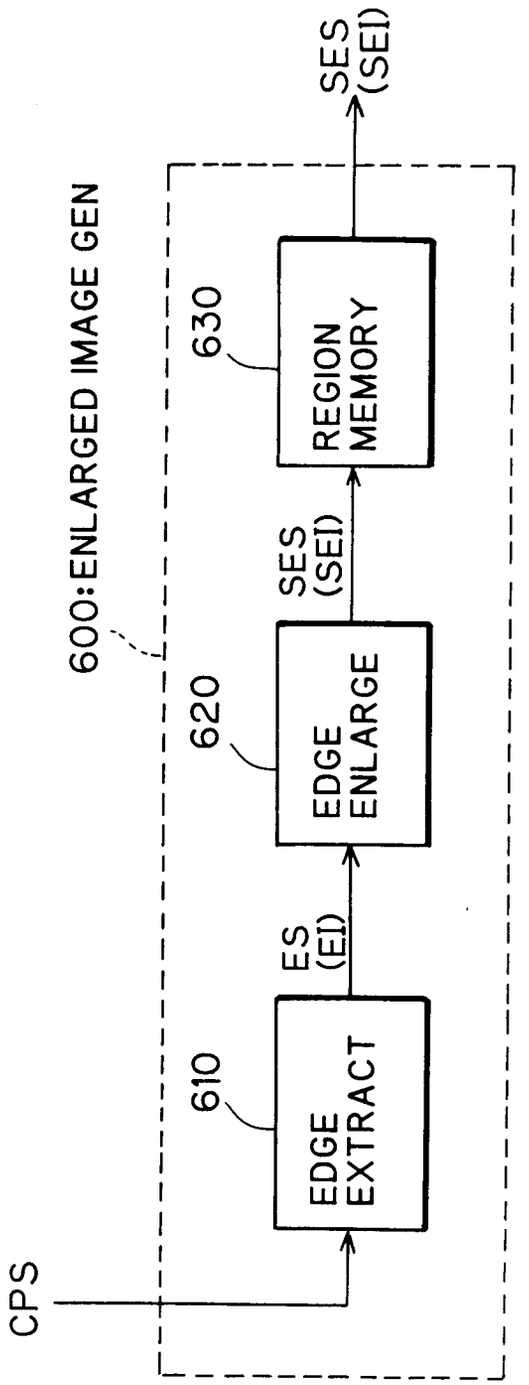

600:ENLARGED IMAGE GEN
CPS
610
EDGE EXTRACT
ES (EI)
620
EDGE ENLARGE
SES (SEI)
630
REGION MEMORY
SES (SEI)

FIG. 7A

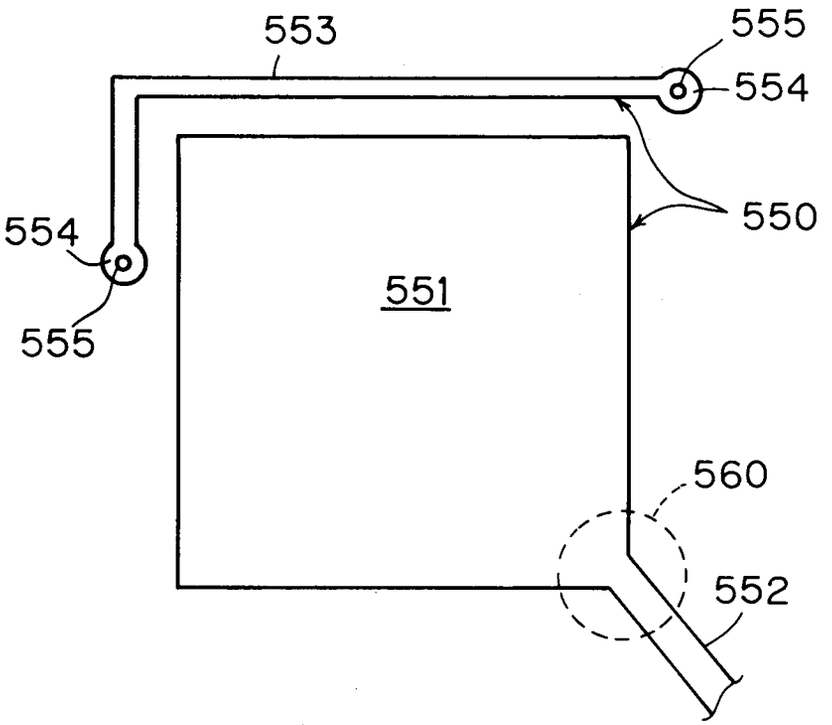


FIG. 7B

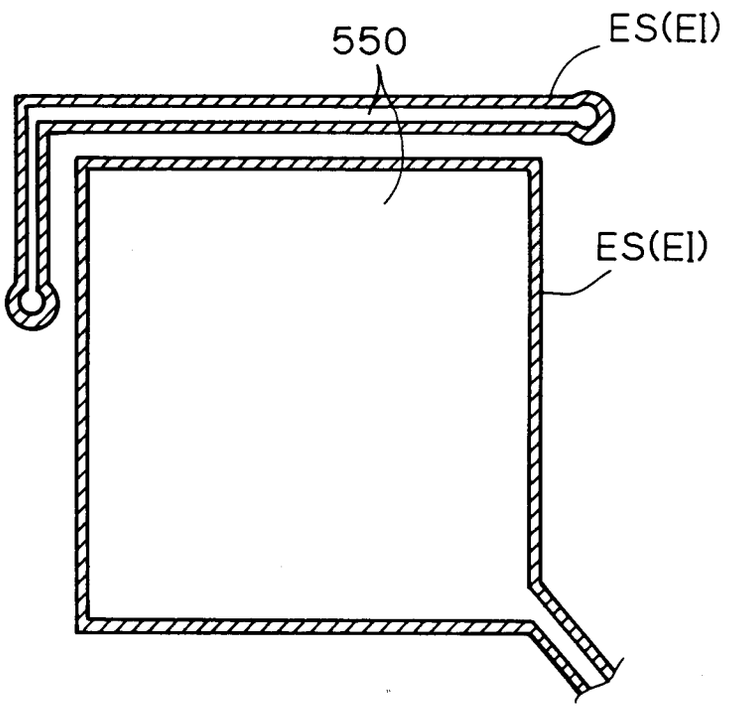


FIG. 7C

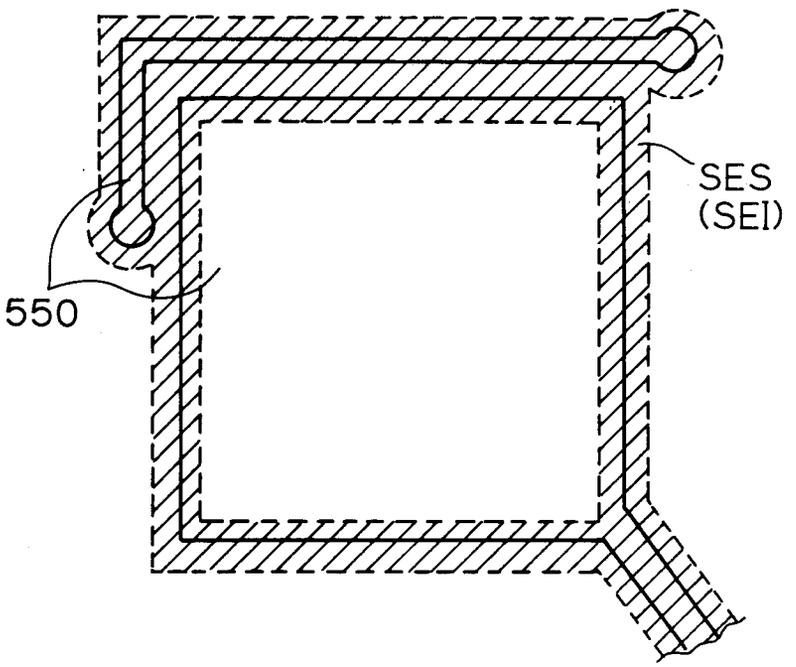


FIG. 16

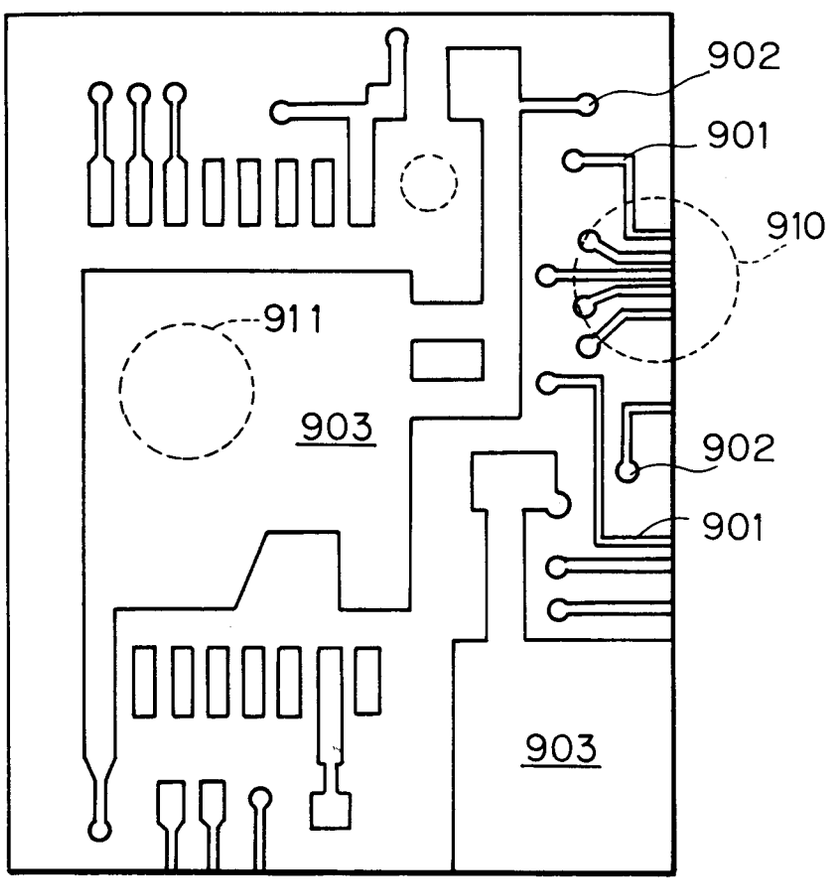


FIG. 8A

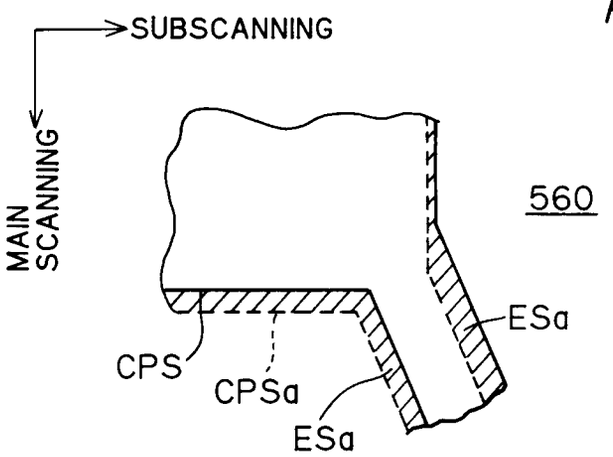


FIG. 8B

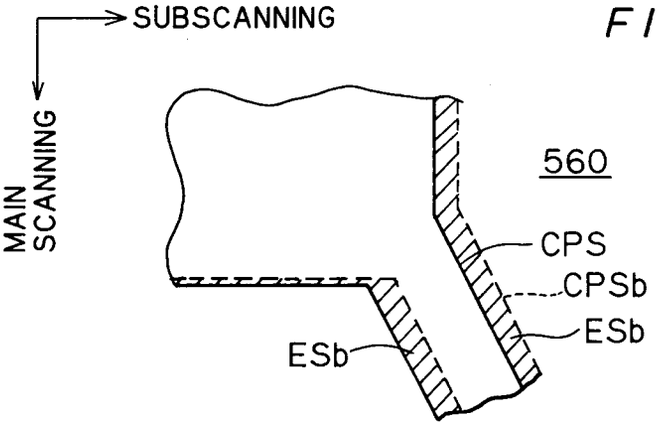


FIG. 8C

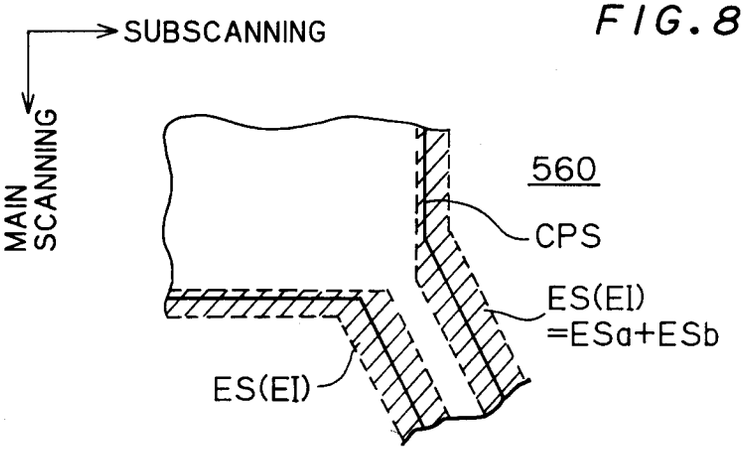


FIG. 9A

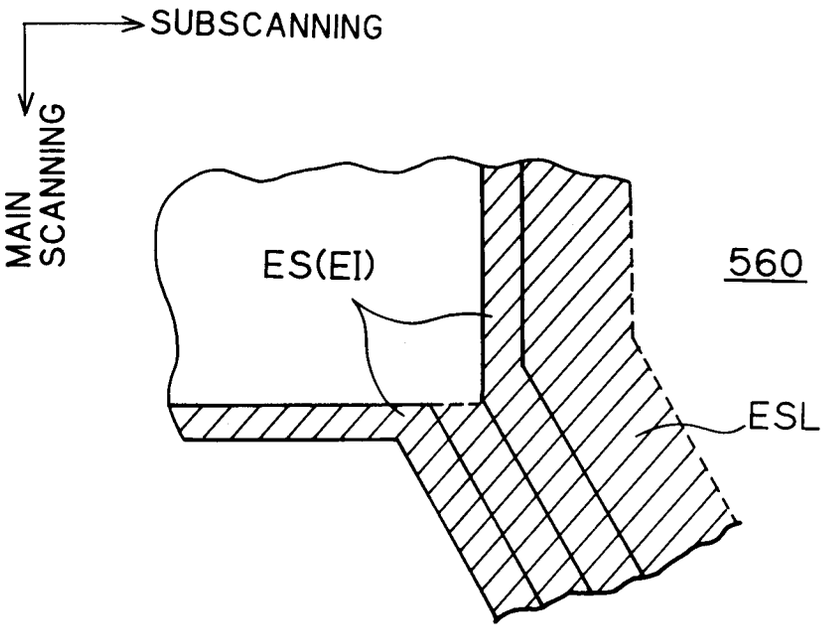

SUBSCANNING
MAIN SCANNING
ES(EI)
560
ESL

FIG. 9B

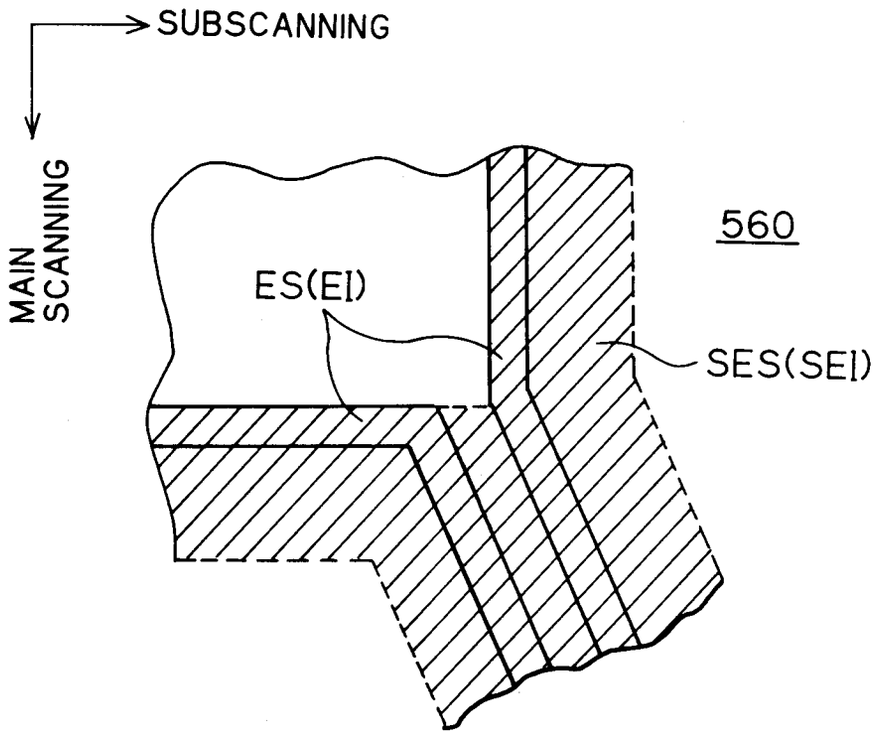

SUBSCANNING
MAIN SCANNING
ES(EI)
560
SES(SEI)

FIG. 10

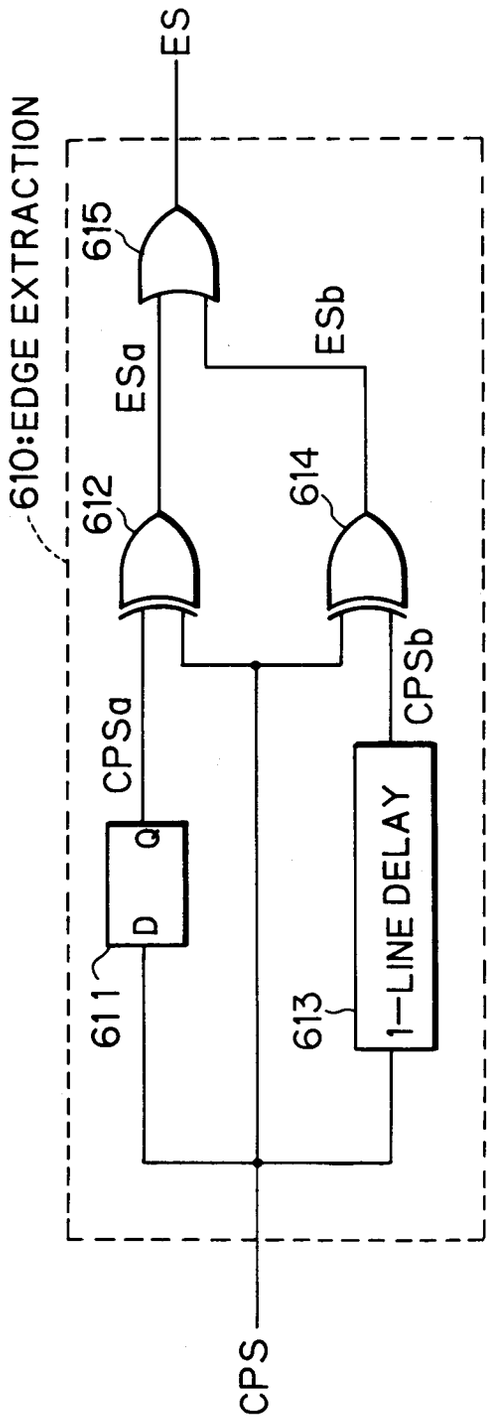

ES
610:EDGE EXTRACTION
615
ESa
ESb
612
614
CPSa
CPSb
D
Q
611
613
1-LINE DELAY
CPS

FIG. 11

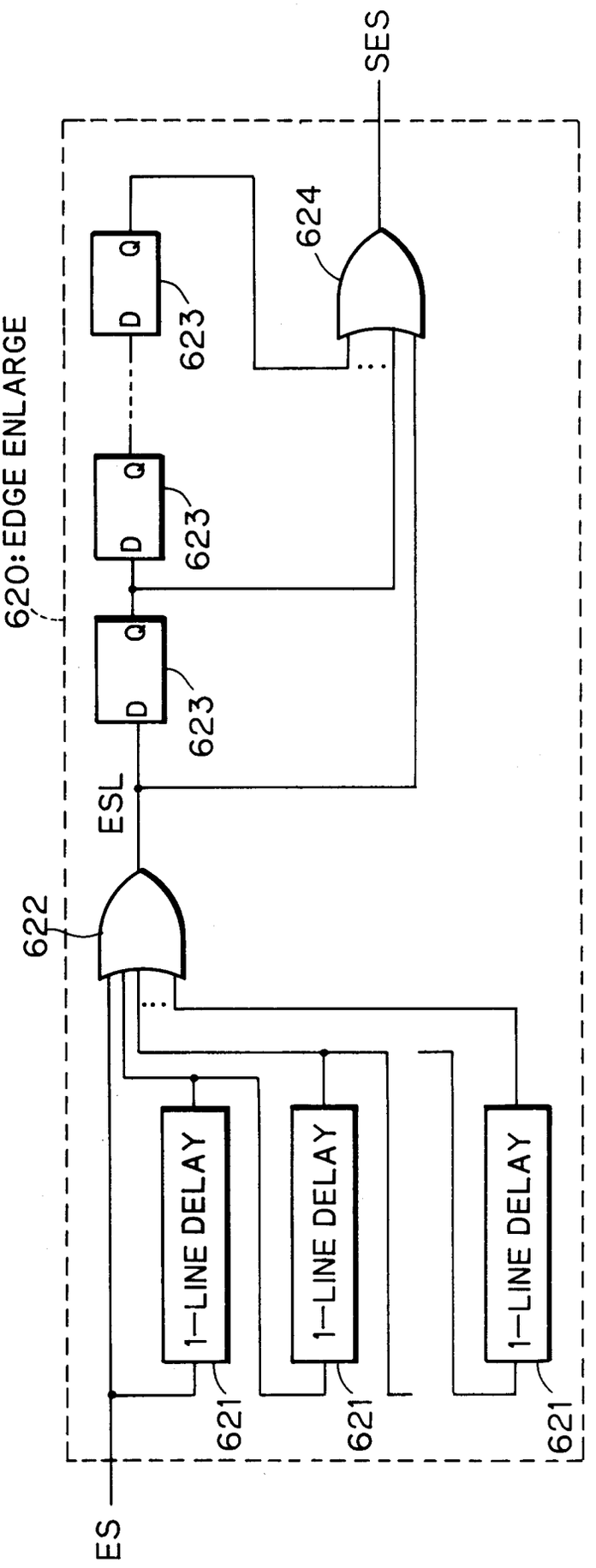

SES
624
620: EDGE ENLARGE
623
623
623
D
Q
ESL
622
1-LINE DELAY
1-LINE DELAY
1-LINE DELAY
621
621
621
ES

FIG. 12A

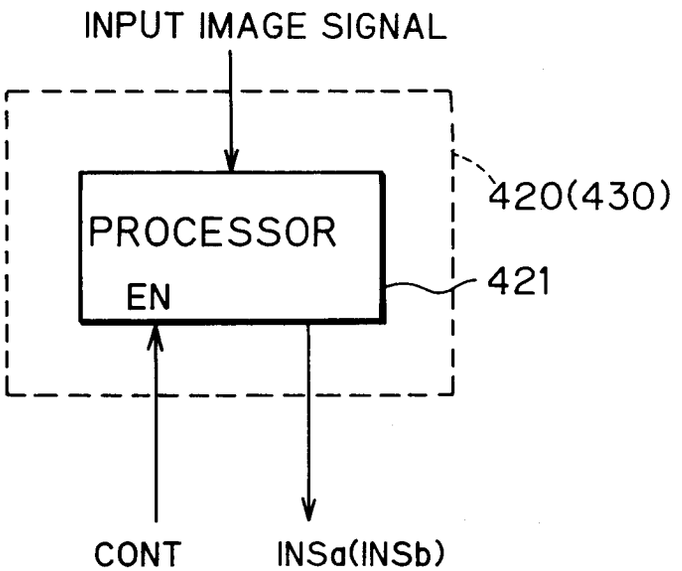


FIG. 12B

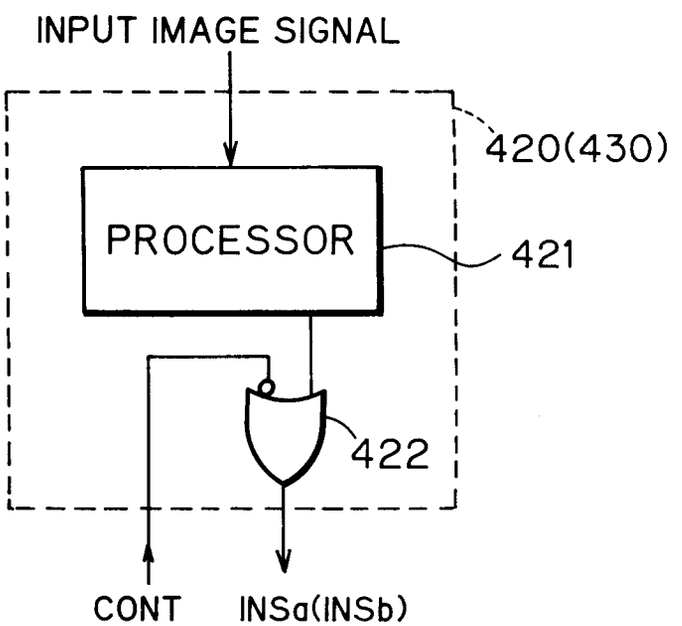


FIG. 12C

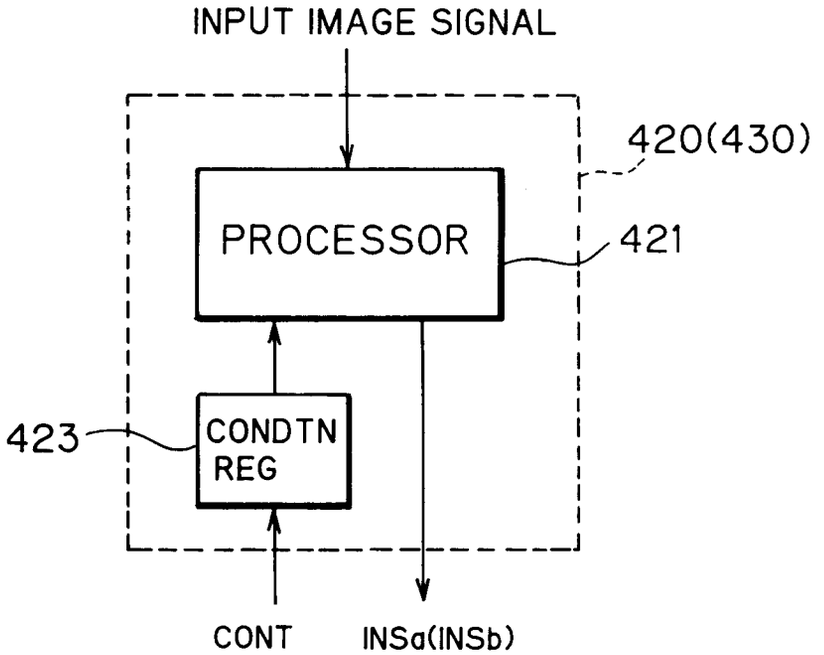


FIG. 12D

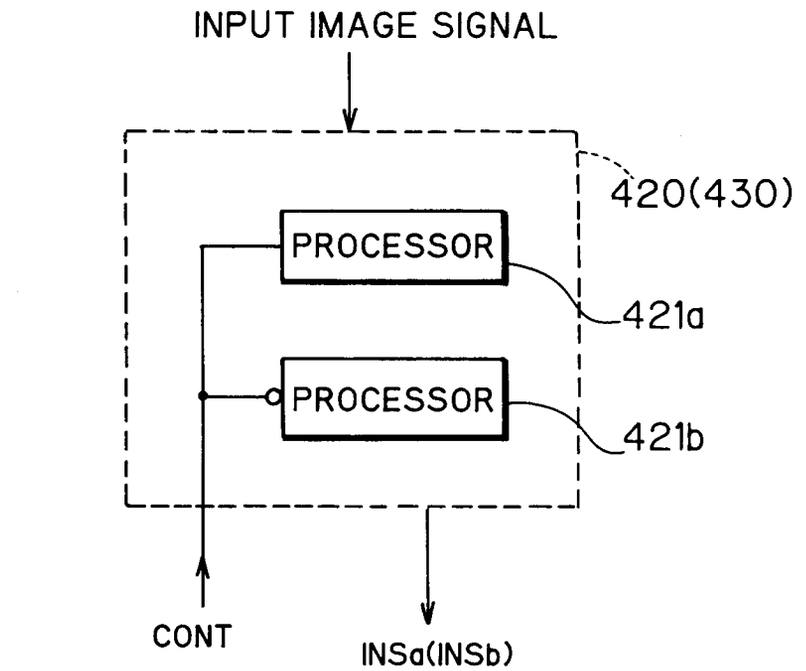


FIG. 13

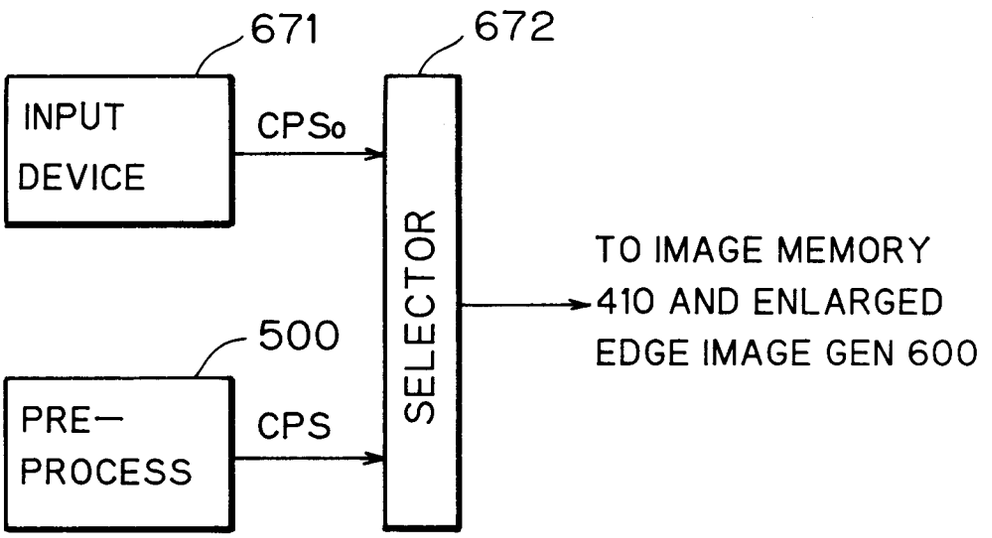

671
672
INPUT DEVICE
CPSo
SELECTOR
TO IMAGE MEMORY 410 AND ENLARGED EDGE IMAGE GEN 600
500
PRE-PROCESS
CPS

FIG. 14

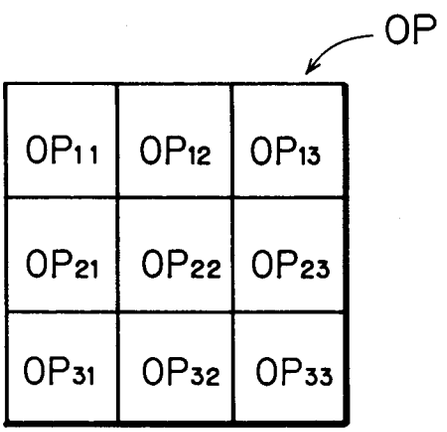

OP
OP11
OP12
OP13
OP21
OP22
OP23
OP31
OP32
OP33

FIG. 15A

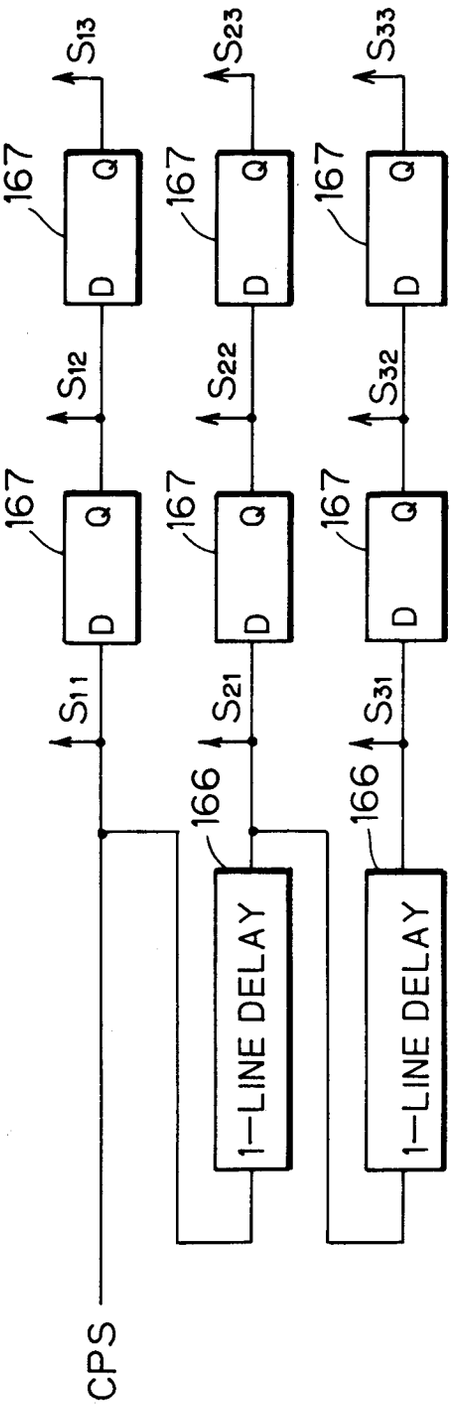

CPS
S11
S12
S13
S21
S22
S23
S31
S32
S33
166
166
167
167
167
167
167
167
167
D
Q
1-LINE DELAY
1-LINE DELAY

FIG. 15B