

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

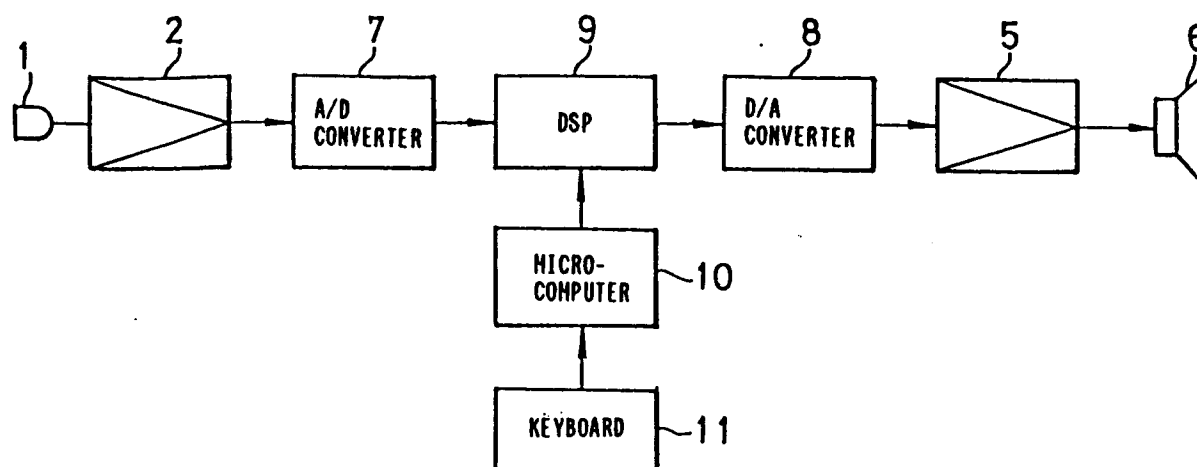
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EUROPEAN PATENT APPLICATION(21) Application number: **91301941.0**(51) Int. Cl.⁵: **H04R 3/02**(22) Date of filing: **08.03.91**(30) Priority: **16.07.90 JP 187676/90**(43) Date of publication of application:
22.01.92 Bulletin 92/04(84) Designated Contracting States:
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London WC2A 3LS(GB)(54) **Audio apparatus with anti-howl function.**

(57) An audio apparatus is arranged to eliminate howls. The apparatus is provided with at least one notch filter (9) arranged across a transmission line of audio signals from a microphone (1), wherein the

band-rejection center frequency of the notch filter (9) varies with time, so that generation of howls is prevented without deteriorating the sound quality.

FIG. 4

The present invention relates to an audio apparatus provided with an anti-howl function.

Audio apparatuses provided with an anti-howl system have widely been introduced and among them is an apparatus which has both a pitch converter and a band-rejection filter interposed between a microphone and a loudspeaker, as disclosed in Japanese Patent Application Laid Open No. 60-28399 (1975). As shown in Fig. 1, that apparatus is arranged such that an audio signal from a microphone 1 is supplied via a microphone amplifier 2 to a pitch converter circuit 3. The pitch converter circuit 3 is provided for varying the frequency of an input audio signal. An output signal from the pitch converter circuit 3 is then fed to a band-rejection filter 4 which actually is a comb filter exhibiting a filter effect in which band-rejection center frequencies are allocated at approximately equal intervals as shown in Fig. 2. Then, an output signal from the band-rejection filter 4 is amplified by a power amplifier 5 for activating a is transmitted to the pitch converter 3 where it is varied in frequency response. The audio signal varied in the frequency passes the band-rejection filter 4 and then, supplied through the power amplifier 5 to the loudspeaker 6 where it is turned to an acoustic output. When a portion of the acoustic output is picked up by the microphone 1, a loop causing a howl is established. The frequency of a feedback audio signal derived from an acoustic input is also varied by the pitch converter 3. It is now assumed that the audio signal from the microphone 1, which has a frequency of f_a as shown in Fig. 3A, is converted by the pitch converter 3 to a feedback audio signal having a frequency of f_b (Fig. 3B) after a duration τ of traveling once throughout the loop. After another duration of τ traveling once more throughout the loop, it is further converted to a re-feedback audio signal having a frequency of f_c (Fig. 3C). If the frequency f_c is identical to a band-rejection center frequency in the band-rejection filter 4, the audio signal of f_c frequency is blocked by the band-rejection filter 4 and thus, howling will be prevented.

For enhancement in the antihowl effect with the prior art audio apparatus provided with such an antihowl system, it is however necessary to have the band-rejection center frequencies allocated at intervals of a smaller distance in the band-rejection filter 4 for rejecting unwanted howl generating signals. A problem then arises that when a distance between the two adjacent band-rejection center frequencies is reduced, the gain of a frequency band between the same becomes attenuated and thus, the quality of a reproduced sound will be degraded.

It is an object of the present invention to provide an audio apparatus capable of eliminating

howls without deterioration in the quality of reproduced sounds.

An audio apparatus according to the present invention is provided with an antihowl system for input of audio signals from a microphone, in which at least one notch filter in which the band-rejection center frequency varies with time is provided in a transmission line of the audio signals.

In the drawings :-

Fig. 1 is a block diagram showing a prior art audio apparatus provided with an antihowl system;

Fig. 2 is a characteristic diagram showing a frequency rejection response in the prior art apparatus illustrated in Fig. 1;

Figs. 3A to 3C are diagrams showing variations of the frequency of an audio signal when a loop is established in the prior art apparatus of Fig. 1; Fig. 4 is a block diagram showing one embodiment of the present invention;

Fig. 5 is a block diagram showing the arrangement of a DSP provided in the apparatus of the present invention portrayed in Fig. 4;

Fig. 6 is a diagram of an equivalent circuit provided for performing the same function as of the DSP;

Fig. 7 illustrates a table showing the storage of coefficient data in a RAM of the DSP;

Fig. 8 shows a table of the band-rejection center frequencies of first to fifth notch filters;

Fig. 9 is a characteristic diagram showing frequency rejection actions in the first to fifth notch filters; and

Figs. 10 and 11 are block diagrams showing two more embodiments of the present invention.

Preferred embodiments of the present invention will be described in detail referring to the accompanying drawings.

Fig. 4 illustrates an improved audio apparatus of the present invention in which an output signal from a microphone 1 is at first fed to a microphone amplifier 2 of which output port is connected to an A/D converter 7. The A/D converter 7 is coupled at output to a DSP (digital signal processor) 9 which is controlled by a microcomputer 10 as will be described later in more detail. The DSP 9 is also coupled at output to a D/A converter 8 where a digital audio signal from the DSP 9 is converted into an analog audio signal. The output of the D/A converter 8 is connected via a power amplifier 5 to a loudspeaker 6 in the same manner as of the prior art.

Fig. 5 schematically illustrates an arrangement of the DSP 9. In operation, a digital signal from the A/D converter 7 is fed to an input interface 13 in the DSP 9. The input interface 13 is coupled to a data bus 14 which in turn is connected to a data memory 12 provided for temporary storage of sig-

nal data and also, to one of the two outputs of a multiplier 15. The other output of the multiplier 15 is coupled to a buffer memory 16 provided for storage of coefficient data. The buffer memory 16 is coupled to a coefficient RAM 17 which holds a plurality of coefficient data. In response to a timing signal from a sequence controller 20, described later, one of the coefficient data stored in the RAM 17 is retrieved and transferred to the buffer memory 16 for storage. The coefficient data retained in the buffer memory 16 is then supplied to the multiplier 15. There is also provided an ALU (arithmetic logic unit) 18 for accumulating calculated outputs of the multiplier 15. The ALU 18 has a couple of inputs; one for receiving a calculated output from the multiplier 15 and the other for communicating to the data bus 14. The output of the ALU 18 is coupled to an accumulator 19 which is in turn connected at output to the data bus 14. The data bus 14 is also connected to a memory controller circuit 22 provided for control on writing and reading of data into and from an external memory 21 for producing delay data.

The data bus 14 is further connected to an output interface 23 which delivers a digital audio signal, i.e. the output of the DSP 9, to the D/A converter 7.

The operational timing in the two interfaces 13 and 23, the multiplier 15, the coefficient RAM 17, the ALU 1, the accumulator 19, and the memory controller circuit 22 is controlled by the sequence controller 20 which is driven according to a processing program loaded in a program memory 24 and also, in response to a command from the microcomputer 10. A keyboard 11 is also connected to the microcomputer 10 for providing various commands through manipulation to the same and keyboard entry will direct the microcomputer 10 for control over the writing of coefficient data into RAM 17.

In operation, a microphone signal fed to the A/D converter 7 is converted in each predetermined sampling period into a digital audio signal form and then, transmitted via the interface 13 to the data memory 12 for storage. A coefficient data read out from the RAM 17 is fed to the buffer memory 16 for temporary storage. The sequence controller 20 is then activated for determining the timing of: reading data from the interface 13, transferring data from the data memory 12 to the multiplier 15 selectively, issuing coefficient data from the RAM 17, triggering the multiplication on the multiplier 15 and the summing on the ALU 18, releasing an output from the accumulator 19, issuing data of calculated results from the interface 23, and so on. For example, the appropriate timing for operation allows both coefficient data α_1 from the buffer memory 16 and data d_1 from the data

memory 12 to be simultaneously fed into the multiplier 15 where they are multiplied to $\alpha_1 \cdot d_1$. Subsequently, $\alpha_1 \cdot d_1$ is calculated by the ALU 18 to $0 + \alpha_1 \cdot d_1$ which is in turn stored in the accumulator 19.

Similarly, coefficient data α_2 from the buffer memory 16 and data d_2 from the data memory 12 are multiplied in the multiplier 15 to $\alpha_2 \cdot d_2$. The input of $\alpha_2 \cdot d_1$ is then combined by the ALU 18 with $\alpha_1 \cdot d_1$ fetched from the accumulator 19 to $\alpha_1 \cdot d_1 + \alpha_2 \cdot d_2$ which is also stored in the accumulator 19. By repeating this procedure, a sum total from $\Sigma \alpha_i \cdot d_i$ is obtained.

For producing a delay data associated with e.g. a reflected sound, corresponding data is read out from the data memory 12 and transmitted via the data bus 14 to the memory controller circuit 22. The memory controller circuit 22 is then activated to write a series of the supplied data into the external memory 21 in sequence so that after completion of the writing, the data can be retrieved in the form of a delay data at the end of a predetermined delay time data interval. The delay data is then fed via the data bus 14 to the data memory 12 for storage and will be ready for use in the foregoing calculation.

The DSP 9 in the audio apparatus of the present invention is also embodied in the form of an equivalent circuit, as shown in Fig. 6, which serves as a secondary IIR filter.

In this filter, a coefficient multiplier 31 and a delay device 32 are coupled in combination to the input terminal which receives an audio data signal. The delay device 32 is then connected at output to another coefficient multiplier 33 and to another delay device 34 which is in turn coupled at output to a further coefficient multiplier 35. The outputs of their respective coefficient multipliers 31, 33, and 35 are all communicated to an adder 36. The adder 36 is then coupled at output to a delay device 37. Similarly, the delay device 37 is connected at output to a coefficient multiplier 38 and also, to another delay device 39. The delay device 39 is coupled at output to another coefficient multiplier 40 and both the coefficient multipliers 38 and 40 are communicated at output to the adder 36.

The delay time of each delay device 32, 34, 37, or 39 is equal to one sampling period. Accordingly, data fed to the multiplier 33 comes one sampling period earlier than that fed to the multiplier 31 and data fed to the multiplier 35 comes two sampling periods earlier than the same.

Simultaneously, similar data inputs are supplied to the multipliers 38 and 40.

Assuming that the multiplier 31 has a coefficient of a_0 , the multiplier 33 a_1 , the multiplier 35 a_2 , the multiplier 38 b_1 , and the multiplier 40 b_2 , the equivalent circuit acts as a notch filter when

$a_0 = a_2 = A$, $a_1 = -b_1 = B$, and $b_2 =$ an arbitrary value. More particularly, the band-rejection center frequency is varied with and thus, defined by A , B , and b_2 .

For developing a single notch filter with the use of digital processing, the DSP 9 is actuated in the following manner.

At the first step, input audio signal data d_n is read out from an n -th location in the data memory 12 and simultaneously, the coefficient data a_2 is retrieved from the RAM 17. Both data are transferred to the buffer memory 16 and multiplied in the multiplier 15. The multiplication $a_1 \cdot d_n$ is then added to 0 by the ALU 18 at the third step-two steps after the first step. And, the resultant sum is stored in the accumulator 19.

At the second step, signal data d_{n-1} is read out from an $(n-1)$ -th location in the data memory 12 and multiplied by the coefficient data a_1 from the RAM 17 in the multiplier 15. The multiplication $a_1 \cdot d_{n-1}$ is then added, at the fourth step, by the ALU 18 to a stored value (the sum calculated at the third step) from the accumulator 19 and the resultant sum is also stored in the accumulator 19. At the third step, an input signal data IN is transferred to an $(n-2)$ -th location in the data memory 12 and also, to the multiplier 15 where it is multiplied by the coefficient data a_0 . The multiplication $a_0 \cdot IN$ is added, at the fifth step, by the ALU 18 to a stored value (the sum at the fourth step) from the accumulator 19 and the resultant sum is stored in the accumulator 19.

Similarly, at the fourth step, signal data d_{n+2} is read out from an $(n+2)$ -th location in the data memory 12 and multiplied by the coefficient data b_2 from the RAM 17 in the multiplier 15. The multiplication $b_2 \cdot d_{n+2}$ is then added, at the sixth step, by the ALU 18 to a stored value (the sum at the fifth step) from the accumulator 19 and the resultant sum is also stored in the accumulator 19. At the fifth step, signal data d_{n+1} is read out from an $(n+1)$ -th location in the data memory 12 and multiplied by the coefficient data b_1 from the RAM 17 in the multiplier 15. The multiplication $b_1 \cdot d_{n+1}$ is then added, at the seventh step, by the ALU 18 to a stored value (the sum calculated at the sixth step) from the accumulator 19 and the resultant sum is also stored as an output data in the accumulator 19.

The coefficient data a_0 , a_1 , a_2 , b_1 , and b_2 have been read from an internal memory (not shown) in the microcomputer 10 and transferred to a pre-determined coefficient data area in the RAM 17. The coefficient data area contains a plurality of coefficient data groups; each data group consisting of the coefficient data a_0 , a_1 , a_2 , b_1 , and b_2 and having different values of A and B , in which the data are stored in the order of a_2 , a_1 , a_0 , b_2 , and

b_1 from the first storage location in the address space.

For forming a plurality-namely five (5)-of the (first to fifth) notch filters which are different in the band-rejection center frequency, the coefficient data groups having a_2 , a_1 , a_0 , b_2 , and b_1 allocated in one group are retrieved and stored in a sequence of F_1 , $F_2, \dots, F_5$, $F_1 + \Delta F_1$, $F_2 + \Delta F_2, \dots, F_4 + 5\Delta F_4$, and $F_5 + 5\Delta F_5$ as shown in Fig. 7. The data groups F_1 to F_5 are provided for determining the band-rejection center frequencies f_1 to f_5 of the first to fifth notch filters respectively. The center frequencies f_1 to f_5 are also designated as reference frequencies, in which $f_1 < f_2 < f_3 < f_4 < f_5$. The data group $F_1 + \Delta F_1$ is prepared for providing a band-rejection center frequency of $f_1 + \Delta f_1$ where f_1 is the reference frequency and Δf_1 is a unit frequency shift. The data group $F_1 + 2\Delta F_1$ is prepared for providing a band-rejection center frequency of f_1 plus $2 \times \Delta f_1$. Similarly, the data groups $F_1 + 3\Delta F_1$, $F_1 + 4\Delta F_1$, and $F_1 + 5\Delta F_1$ are adopted for providing band-rejection center frequencies obtained by adding $3 \times \Delta f_1$, $4 \times \Delta f_1$, and $5 \times \Delta f_1$ to f_1 respectively. The other data groups F_2 , F_3 , F_4 , and F_5 are provided for similar purpose. The frequency shifts Δf_1 , Δf_2 , Δf_3 , Δf_4 , and Δf_5 in a unit time need not be the same and can be determined independently. In the operation of reading, the coefficient data are retrieved from the first location in the address space by a timing signal given from the sequence controller 20; for example, a_2 , a_1 , a_0 , b_2 , and b_1 of the data group F_1 , a_2 , a_1 , a_0 , b_2 , and b_1 of the data group F_2 , and so on in sequence. When the reading of a_2 , a_1 , a_0 , b_2 , and b_1 of the last data group $F_5 + 5\Delta F_5$ is completed, a second reading operation will start with the data group F_1 from the first location of the address space.

The coefficient data groups F_1 to F_5 retrieved are then multiplied by sampling signal data of the first timing respectively and $F_1 + \Delta F_1$ to $F_5 + \Delta F_5$ are multiplied by sampling signal data of the second timing respectively. In similar manner, the coefficient data groups $F_1 + 2\Delta F_1$ to $F_5 + 2\Delta F_5$, $F_1 + 3\Delta F_1$ to $F_5 + 3\Delta F_5$, $F_1 + 4\Delta F_1$ to $F_5 + 4\Delta F_5$, and $F_1 + 5\Delta F_1$ to $F_5 + 5\Delta F_5$ are multiplied and these steps will be repeated.

Accordingly, the band-rejection center frequencies of the first to fifth notch filters are determined, as shown in Fig. 8, f_1 to f_5 for the coefficient data groups F_1 to F_5 respectively, $f_1 + \Delta f_1$ to $f_5 + \Delta f_5$ for $F_1 + \Delta F_1$ to $F_5 + \Delta F_5$, $f_1 + 2\Delta f_1$ to $f_5 + 2\Delta f_5$ for $F_1 + 2\Delta F_1$ to $F_5 + 2\Delta F_5$, $f_1 + 3\Delta f_1$ to $f_5 + 3\Delta f_5$ for $F_1 + 3\Delta F_1$ to $F_5 + 3\Delta F_5$, $f_1 + 4\Delta f_1$ to $f_5 + 4\Delta f_5$ for $F_1 + 4\Delta F_1$ to $F_5 + 4\Delta F_5$, and $f_1 + 5\Delta f_1$ to $f_5 + 5\Delta f_5$ for $F_1 + 5\Delta F_1$ to $F_5 + 5\Delta F_5$. As this procedure is repeated, the band-rejection center frequency of each notch filter will vary with time. For example, the first notch filter shifts the band-rejection center

frequency from f_1 which is the reference frequency denoted by the numeral 1 to $f_1 + \Delta f_1$ denoted by 2, to $f_1 + 2\Delta f_1$ denoted by 3, to $f_1 + 3\Delta f_1$ denoted by 4, to $f_1 + 4\Delta f_1$ denoted by 5, and to $f_1 + 5\Delta f_1$ denoted by 6, as shown in Fig. 9. Like the first notch filter, the second to fifth notch filters change with time their respective band-rejection center frequencies f_2 , f_3 , f_4 , and f_5 , shown in Fig. 9, in the same manner.

In the aforementioned embodiment, the first to fifth notch filters are intended to be not always equal in the size of frequency shift. It is a common practice in a particular range (namely 1 kHz to 4 kHz) of frequencies which involves more howls to provide an increased number of notch filters as compared with the other band of frequencies, in which the frequency shift of a band-rejection center frequency may be minimized and also, the shifting speed per unit time may be increased. It is preferred that for example, the shift of the band-rejection center frequency ranging from 1 kHz and 4 kHz is 2 Hz and the shifting speed is 1 Hz per unit time.

Although the DSP 9 is chiefly provided in the arrangement of the embodiment according to the present invention, it may be replaced with another device(s). For example, a plurality of notch filters of secondary IIR type 41_1 , $41_2, \dots, 41_n$ may be interposed between the A/D converter 7 and the D/A converter 8 as shown in Fig. 10. Each of the notch filters 41_1 , $41_2, \dots, 41_n$ which are different in the band-rejection center frequency is arranged so that its band-rejection center frequency is varied by changing a coefficient for multiplication with the controller circuit 42. Those notch filters may also be arranged for constituting an analog circuit.

Fig. 11 illustrates another embodiment of the present invention in the form of an audio apparatus which is constructed by adding a frequency modulation circuit 43 to the arrangement portrayed in Fig. 10. The frequency modulation circuit 43 is provided with a memory (not shown) for varying the frequency of a digital audio signal by writing the signal into the memory and reading it out from the same at a different speed from the writing speed. The frequency modulation circuit 43 is well known, for example, as a tone controller disclosed in Japanese Patent Application Laid-Open No. 61-118797(1986) or 61-121096(1986). So, the details of the circuit will not be described. Such a frequency modulation circuit may be formed with the DSP, in which the writing and reading of data into and from the external RAM 21 shown in Fig. 5 is controlled by the memory controller circuit 22. Also, the frequency modulation circuit may incorporate a known analog circuit. As above described, the audio apparatus provided with an antihowl system according to the present invention has notch

filters arranged across the transmission line of an audio signal from a microphone for varying with time the band-rejection center frequency. Accordingly, the notch filters having different band-rejection center frequencies can closely be aligned throughout a particular band of frequencies which tends to cause formidable howls and thus, block unwanted audio signals which are bound to develop a loop causing a howl. Consequently, howls will be eliminated without deterioration in the quality of a reproduced sound.

Claims

1. An audio apparatus comprising an audio signal transmission line for transmission of audio signals supplied from a microphone, and at least one notch filter provided across the audio signal transmission line, wherein said at least one notch filter has a band-rejection center frequency which varies with time.
2. An audio apparatus according to Claim 1, wherein a frequency modulation circuit is provided in said audio signal transmission line.
3. An audio apparatus according to Claim 1, wherein the notch filter is an IIR type filter.
4. An audio apparatus according to Claim 3, further comprising a digital signal processor and said IIR filter is formed by said digital signal processor performing predetermined operating processes.

FIG. 1

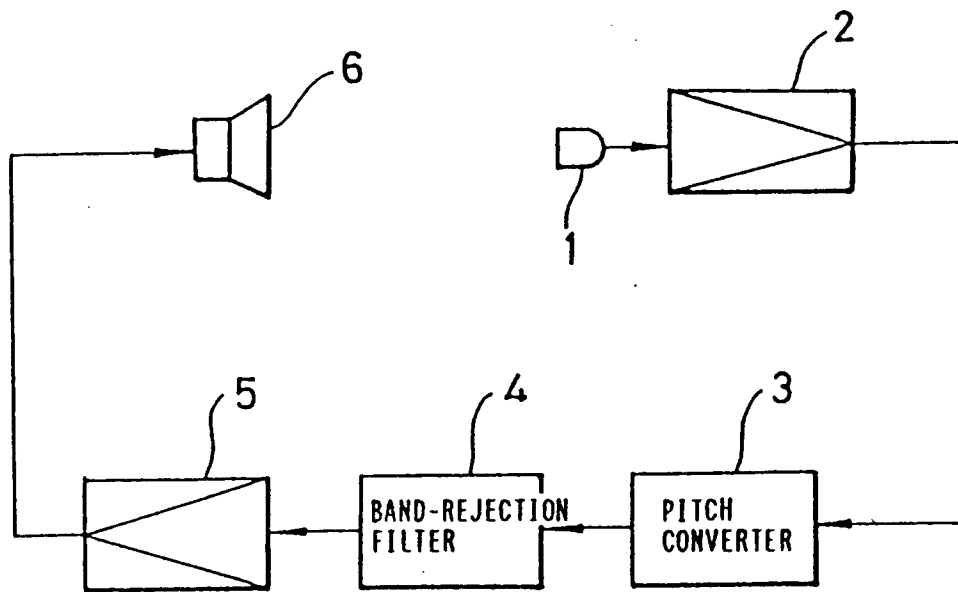
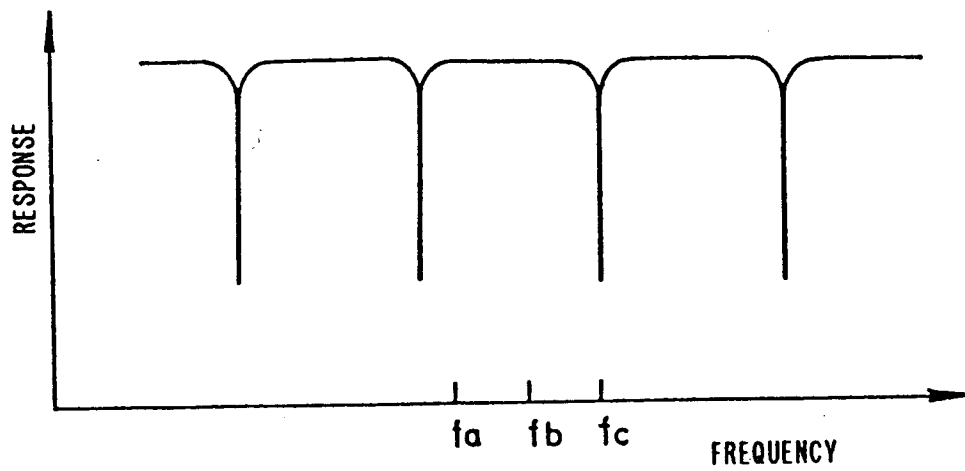


FIG. 2



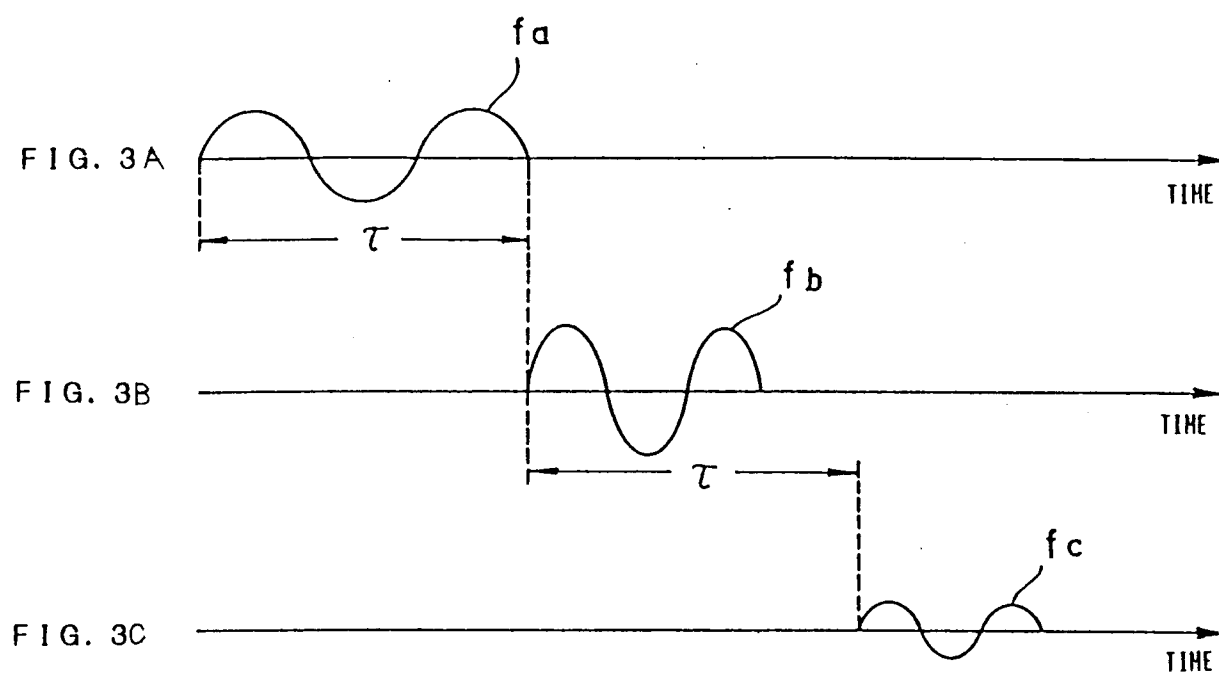


FIG. 4

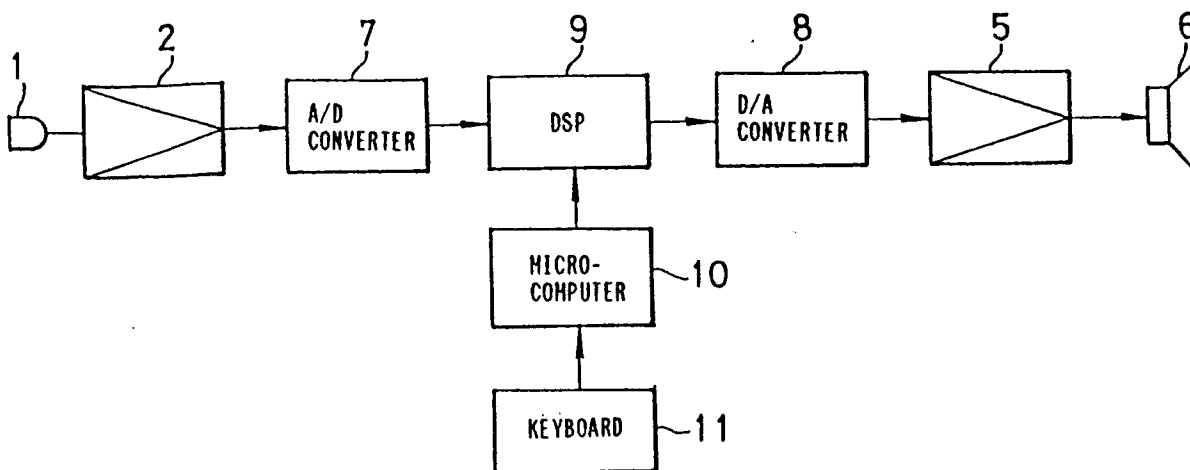


FIG. 6

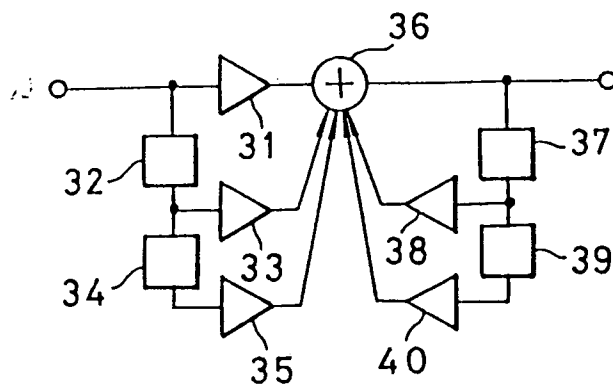


FIG. 5

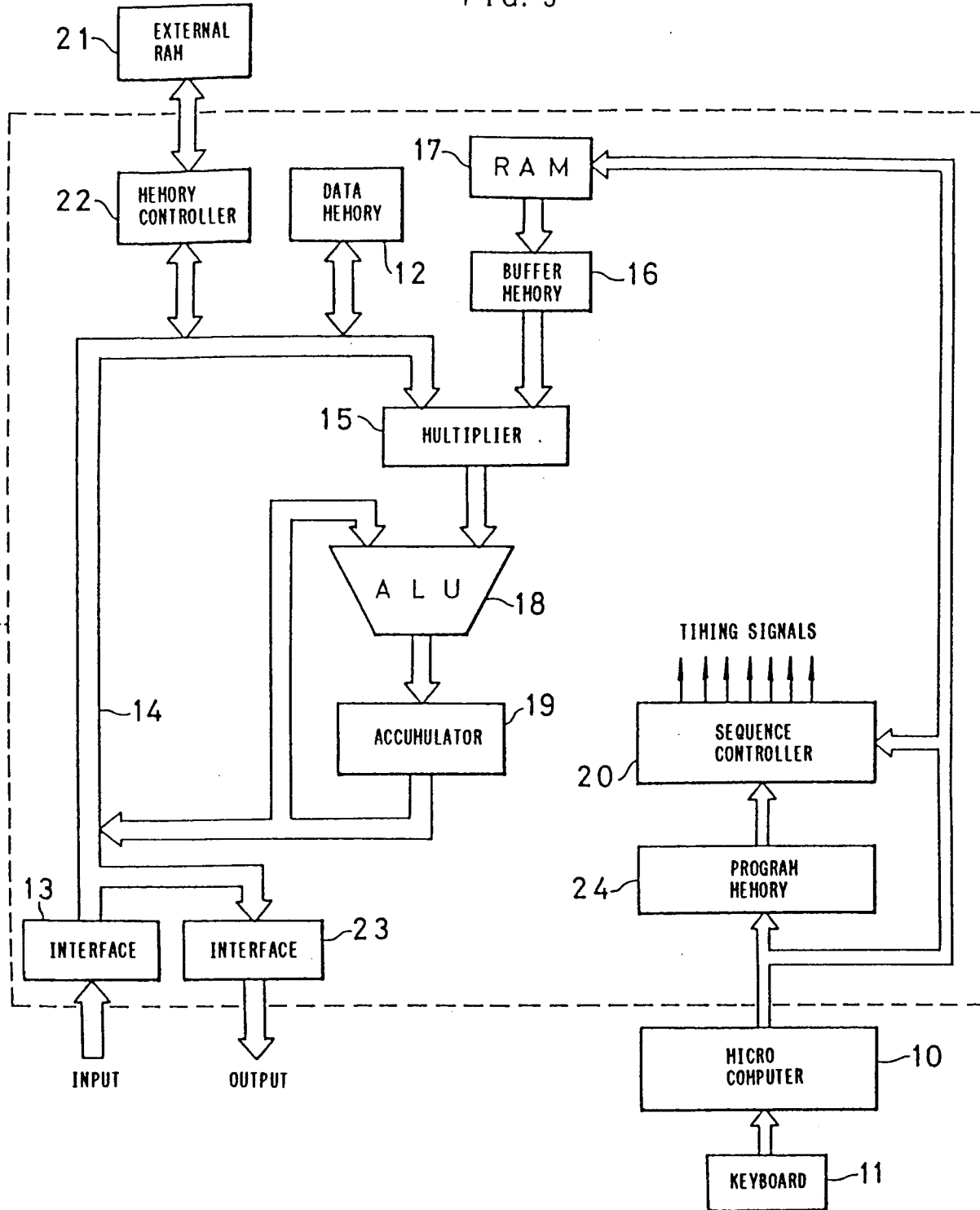


FIG. 7

READ NO.	COEFFICIENT DATA GROUP	READ NO.	COEFFICIENT DATA GROUP	READ NO.	COEFFICIENT DATA GROUP
1	F_1	11	$F_1 + 2 \Delta F_1$	21	$F_1 + 4 \Delta F_1$
2	F_2	12	$F_2 + 2 \Delta F_2$	22	$F_2 + 4 \Delta F_2$
3	F_3	13	$F_3 + 2 \Delta F_3$	23	$F_3 + 4 \Delta F_3$
4	F_4	14	$F_4 + 2 \Delta F_4$	24	$F_4 + 4 \Delta F_4$
5	F_5	15	$F_5 + 2 \Delta F_5$	25	$F_5 + 4 \Delta F_5$
6	$F_1 + \Delta F_1$	16	$F_1 + 3 \Delta F_1$	26	$F_1 + 5 \Delta F_1$
7	$F_2 + \Delta F_2$	17	$F_2 + 3 \Delta F_2$	27	$F_2 + 5 \Delta F_2$
8	$F_3 + \Delta F_3$	18	$F_3 + 3 \Delta F_3$	28	$F_3 + 5 \Delta F_3$
9	$F_4 + \Delta F_4$	19	$F_4 + 3 \Delta F_4$	29	$F_4 + 5 \Delta F_4$
10	$F_5 + \Delta F_5$	20	$F_5 + 3 \Delta F_5$	30	$F_5 + 5 \Delta F_5$

FIG. 8

PROCESS NO.	1ST NOTCH FILTER BAND-REJECTION FREQUENCY	2ND NOTCH FILTER BAND-REJECTION FREQUENCY	3RD NOTCH FILTER BAND-REJECTION FREQUENCY	4TH FILTER BAND-REJECTION FREQUENCY	5TH FILTER BAND-REJECTION FREQUENCY
1	f_1	f_2	f_3	f_4	f_5
2	$f_1 + \Delta f_1$	$f_2 + \Delta f_2$	$f_3 + \Delta f_3$	$f_4 + \Delta f_4$	$f_5 + \Delta f_5$
3	$f_1 + 2\Delta f_1$	$f_2 + 2\Delta f_2$	$f_3 + 2\Delta f_3$	$f_4 + 2\Delta f_4$	$f_5 + 2\Delta f_5$
4	$f_1 + 3\Delta f_1$	$f_2 + 3\Delta f_2$	$f_3 + 3\Delta f_3$	$f_4 + 3\Delta f_4$	$f_5 + 3\Delta f_5$
5	$f_1 + 4\Delta f_1$	$f_2 + 4\Delta f_2$	$f_3 + 4\Delta f_3$	$f_4 + 4\Delta f_4$	$f_5 + 4\Delta f_5$
6	$f_1 + 5\Delta f_1$	$f_2 + 5\Delta f_2$	$f_3 + 5\Delta f_3$	$f_4 + 5\Delta f_4$	$f_5 + 5\Delta f_5$
7	f_1	f_2	f_3	f_4	f_5
8	$f_1 + \Delta f_1$	$f_2 + \Delta f_2$	$f_3 + \Delta f_3$	$f_4 + \Delta f_4$	$f_5 + \Delta f_5$
⋮	⋮	⋮	⋮	⋮	⋮

FIG. 9

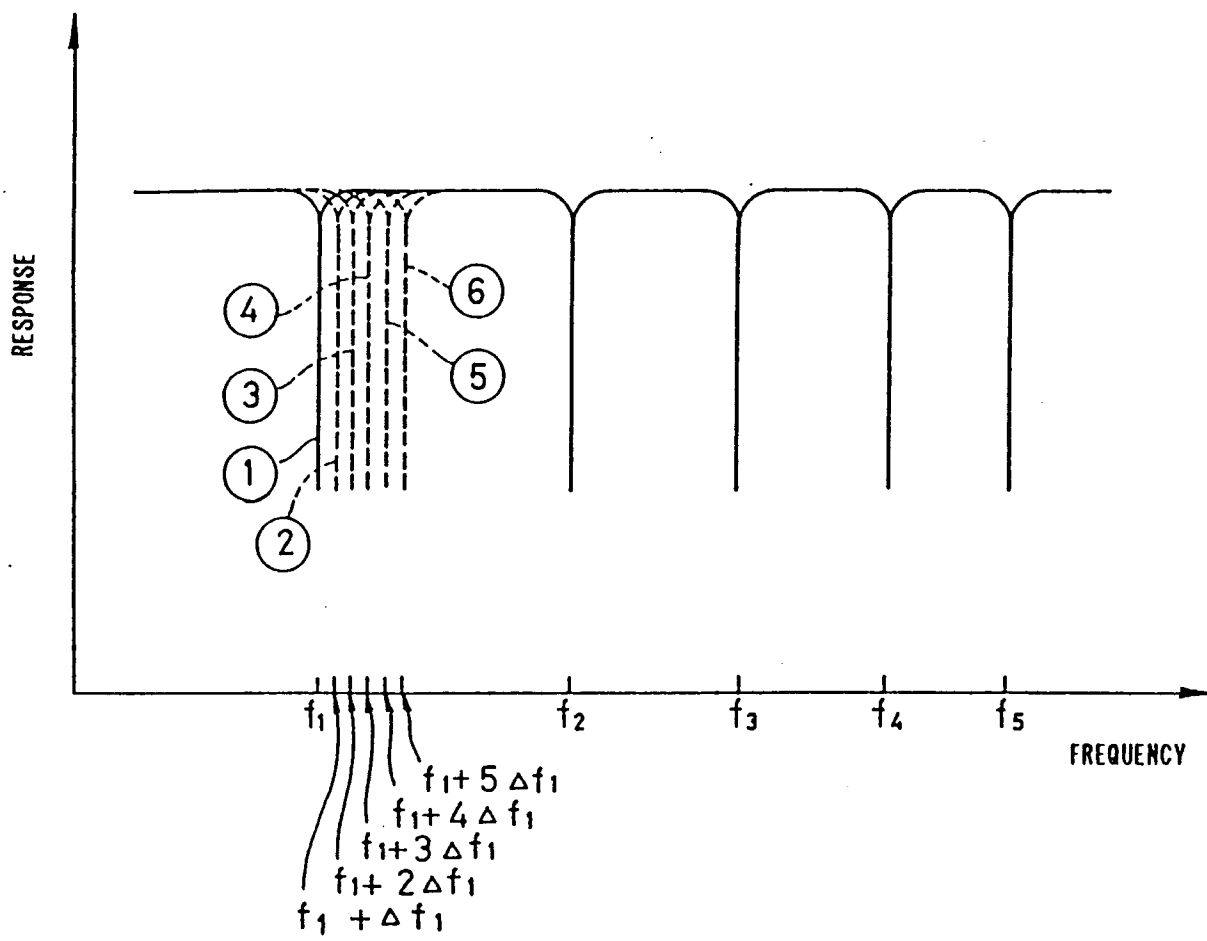


FIG. 10

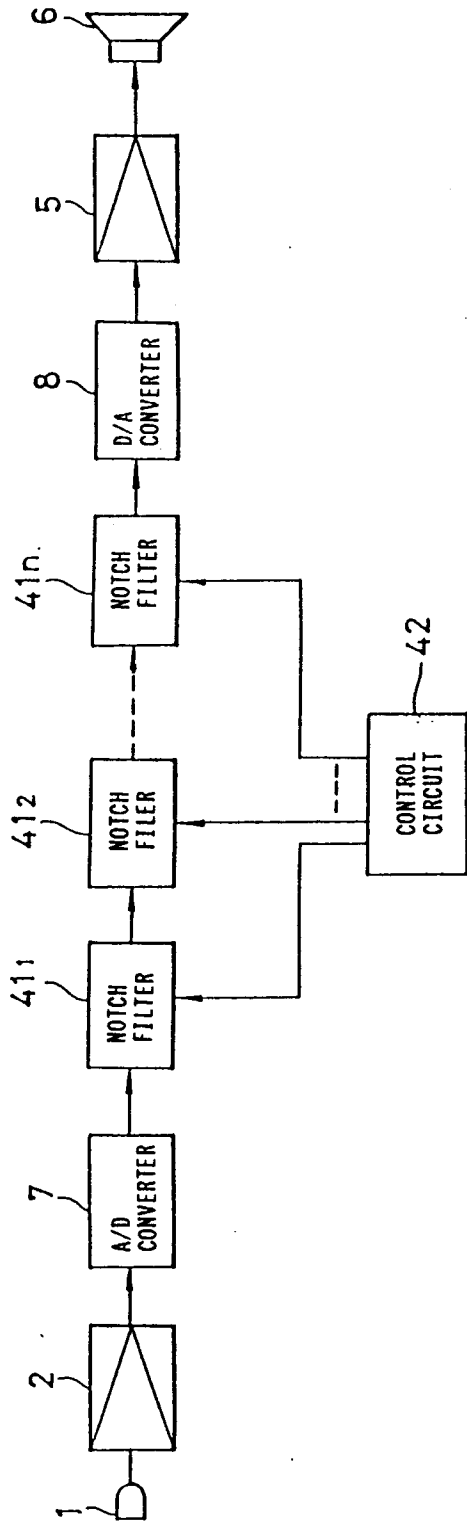


FIG. 11

