(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 477 843 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91116212.1**

(51) Int. Cl.5: **G09G 1/16**

(22) Date of filing: **24.09.91**

(30) Priority: **25.09.90 JP 254895/90**
18.10.90 JP 279919/90

(43) Date of publication of application:
01.04.92 Bulletin 92/14

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **NEC CORPORATION**
7-1, Shiba 5-chome Minato-ku
Tokyo 108-01(JP)

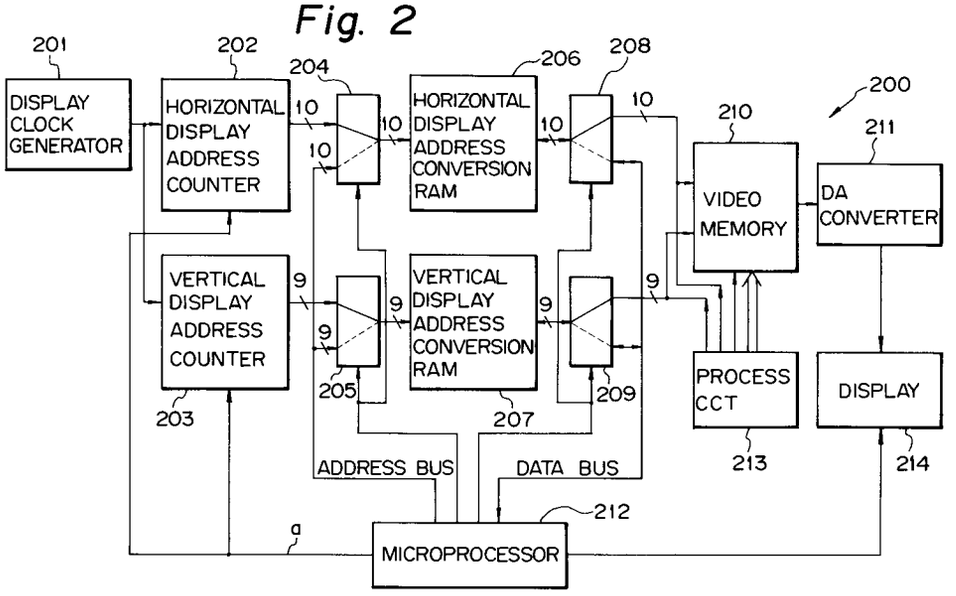
(72) Inventor: **Nakamura, Takaharu, c/o NEC Corporation**
7-1, Shiba 5-chome
Minato-ku, Tokyo(JP)

(74) Representative: **Vossius & Partner**
Siebertstrasse 4 P.O. Box 86 07 67
W-8000 München 86(DE)

(54) Image display system.

(57) An image display system capable of moving, enlarging, reducing or otherwise manipulating an image being displayed on a screen. Display addresses are divided in the horizontal and vertical directions. A horizontal and a vertical display address conversion RAM (206,207) are each connected to respective one of display address buses so as to convert the display addresses in the horizontal or vertical direction. An additional bit representative of an image display timing may be assigned to each of conversion table data stored in horizontal and vertical address conversion RAMs (206,207) which are connected to particular one of a plurality of video memories (210).

Fig. 2



EP 0 477 843 A2

The present invention relates to an image display system and, more particularly, to an image display system capable of moving, enlarging, reducing or otherwise manipulating an image being displayed on a display.

An conventional image display system of the type described has a display clock generator, a display address counter, an address bus switch, a display address conversion RAM (Random Access Memory), a memory address switch, a video memory, a digital-to-analog (DA) converter, and a microprocessor. The display clock generator generates a display clock having a predetermined period. When data is to be read out of the video memory, the display address counter outputs a display address by counting the display clock in response to a command from the microprocessor. The display address is applied to the address input of the conversion RAM via the address bus switch. The conversion RAM converts the input display address on the basis of data stored therein and feeds out the converted display address to a data line. The converted display address is delivered to the address terminal of the video memory with the result that image data designated by the display address is read out. The DA converter converts the image data to a video signal.

To change the position or the size of an image being displayed, the microprocessor is used to switch the display address switch and memory address switch such that the address bus and data bus of the conversion RAM are connected to those of the microprocessor. After the microprocessor has changed the data stored in the RAM, the switches are restored to their original states so as to display the manipulated image. This kind of technology for reading data out of a video memory by address conversion is disclosed in, for example, "A Raster Assembly Processor (RAP) for Integrated HDTV Display of Video data and Image windows," IEEE 1987, pp. 731-739.

The problem with the conventional system is that the conversion RAM has to convert all of the display addresses sequentially generated by the display address counter and, therefore, needs an extremely great capacity. For example, when the display has a resolution of 640 dots (horizontal) $\times$ 400 lines (vertical), a conversion RAM whose capacity is as great as 4, 608, 000 bits is needed.

It is, therefore, an object of the present invention to provide an image display system which noticeably reduces the required capacity an address conversion RAM.

It is another object of the present invention to provide a generally improved image display system.

An image display system of the present invention comprises a horizontal display address counter for outputting a horizontal display address in response to a display clock, a vertical display address counter for outputting a vertical display address in response to the display clock, a horizontal display address conversion memory having an address input to which the horizontal display address is connected, a vertical display address conversion memory having an address input to which the vertical display address is connected, a video memory having address inputs to which a data bus from the horizontal display address conversion memory and a data bus from the vertical display address conversion memory are connected, the video memory outputting video data on the basis of the input addresses, and a rewriting circuit for rewriting data stored in the horizontal and vertical display address conversion memories.

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings in which:

FIG. 1 is a block diagram schematically showing a conventional image display system;

FIG. 2 is a block diagram schematically showing an image display system embodying the present invention;

FIG. 3 is a memory map representative of a video memory included in the embodiment;

FIGS. 4A and 4B are memory maps representative of, respectively, a horizontal and a vertical display address conversion RAM also included in the embodiment;

FIG. 5 is a memory map indicative of a specific condition wherein data stored in the vertical display address conversion RAM is manipulated;

FIG. 6 shows table data to be written to the horizontal and vertical conversion RAMs for doubling the size of an image;

FIG. 7 shows a relation between the video memory and a display in the condition shown in FIG. 6;

FIG. 8 is a block diagram schematically showing an alternative embodiment of the present invention; and

FIGS. 9A and 9B show additional bis and a specific condition of a screen.

To better understand the present invention, a brief reference will be made to a prior art image display system, shown in FIG. 1. As shown, the convenional image display system, generally 100, has a display clock generator 101, a display address counter 102, an address bus switch 103, a display address conversion RAM 104, a memory address switch 105, a video memory 106, a DA converter 107, and a microprocessor 108. The display clock generator 101 generates a display clock having a predetermined period. When data is to be read out of the video memory 106, the microprocessor 108 causes the display

address counter 102 to count the display clock to thereby generate a display address. The display address is applied to the address terminal of the RAM 104 via the address bus switch 103. In response, the RAM 104 converts the display address on the basis of data stored therein and feeds the resulting converted address to the address terminal of the video memory 106 via the memory address switch 105. On receiving the display address, the video memory 106 outputs video data. The DA converter 107 converts the video data fed thereto from the video memory 106 to a video signal. To change the position or the size of an image being displayed, the microprocessor 108 is used to switch the display address switch 103 and memory address switch 105 such that the address bus and data bus of the RAM 104 are connected to those of the microprocessor 108. After the microprocessor 108 has changed the data stored in the RAM 104, the switches 103 and 105 are restored to their original states so as to display an image.

The conventional system 100 has a draback that the address conversion RAM has to convert all of the display addresses sequentially generated by the display address counter 102 and, therefore, needs an extremely great capacity, as discussed earlier.

Referring to FIG. 2, an image display system embodying the present invention is shown and generally designated by the reference numeral 200. As shown, the system 200 has a display clock generator 201 for generating a display clock. A horizontal display address counter 202 counts the display clock while sequentially outputting horizontal display addresses. A vertical display address counter 203 is incremented every time it receives m clock pulses from the horizontal clock generator 201 (m being the number of addresses in the horizontal direction), while outputting the resulting count as a vertical display address. A horizontal address bus switch 204 selects either one of an address bus extending from the horizontal display address counter 202 and an address bus extending from a microprocessor 212 which will be described. A vertical address bus switch 205 selects either one of an address bus extending from the vertical address counter 203 and the address bus extending from the microprocessor 212. A horizontal display address conversion RAM 206 has an address input to which the horizontal display address is connected. A vertical display address conversion RAM 207 has an address input to which the vertical display address is connected. The reference numeral 210 designates a video memory. A horizontal memory address switch 208 is connected to the horizontal display address conversion RAM 206 for selecting either one of a data bus terminating at the video memory 210 and a data bus terminating at the microprocessor 212. A vertical memory address switch 209 selects either one of a data bus terminating at the video memory 210 and the data bus terminating at the microprocessor 212. A DA converter 211 converts video data read out of the video memory 210 to a video signal and feeds it to a conventional display 214. The microprocessor 212 controls the states of the switches 204, 205, 208 and 209 and rewrites the data stored in the RAMs 206 and 207. The reference numeral 213 designates an image processing circuit.

The image processing circuit 213 sequentially writes the first to n-th lines of video data in the video memory 210 pixel by pixel. Specifically, the circuit 213 processes TV (Television) video data in a predetermined manner to generate video data pixel by pixel and generates horizontal and vertical addresses representative of particular horizontal and vertical writing positions of the video memory 210 at the same time, thereby writing the image data in such addresses. The display 214 displays the image data stored in the video memory 10 line by line in synchronism with a horizontal scanning signal. The switches 204, 205, 208 and 209 play the role of rewriting means in combination.

In the embodiment, the resolution is assumed to be 640 dots in the horizontal direction of the display 214 and 400 lines in the vertical direction. Hence, the horizontal and vertical display addresses require 10 bits and 9 bits, respectively.

FIG. 3 is a memory map representative of the video memory 210. In the figure, image data A on the second line is designated by an address "0000000001000000001". FIGS. 4A and 4B are memory maps representative of the RAMs 206 and 207, respectively.

In operation, the display clock generator 201 feeds a display dot clock to the horizontal display address counter 202 and vertical display address counter 203. The horizontal display address counter 202 starts counting the input clock in response to a start signal α from the microprocessor 212. The counter 202 repetitively counts the display addresses 0-639 of dots in the horizontal direction in synchronism with the horizontal scanning period of the display 14, while delivering the count to the 10-bit horizontal display address bus. The horizontal address bus switch 204 has a first input connected to the display address bus from the address counter 202 and a second input connected to the address bus from the microprocessor 212. The switch 204, therefore, selects either one of the address buses connected to the first and second inputs thereof and connects it to the address terminal of the horizontal address conversion RAM 206.

During an image display period, the horizontal address bus switch 204 is connected to the horizontal address counter 202. In this condition, display addresses synchronous to the clock signal from the display clock generator 201 are sequentially inputted to the horizontal address conversion RAM 206, whereby data

are sequentially read out of the RAM 206. The data from the RAM 206 has a 10-bit bus width and is applied to the horizontal memory address switch 208. This switch 208 delivers the input 10-bit data to the lower 10-bit data bus of the video memory 210. The video data in the horizontal direction are sequentially read out as designated by the addresses which are fed to the lower address of the video memory 210.

Regarding the display in the vertical direction, the vertical address counter 203 counts the addresses 0-399 of the display lines while delivering the count to the 9-bit vertical display address bus. During an image display period, the vertical display address from the address counter 203 is applied to the vertical address conversion RAM 207 via the vertical address bus switch 205. As a result, 9-bit data is read out of the RAM 207 as designated by the input address and then routed through the switch 209 to the upper address bus of the video memory.

The above-stated display in the horizontal and vertical directions is effected according to the scanning on the screen of the display 214. Consequently, video data are sequentially read out of the video memory 10, converted to an analog video data by the DA converter 211, and then fed to the display 214.

The display addresses inputted to the video memory 10 are the data having been read out of the horizontal and vertical address conversion RAMs 206 and 207. Therefore, the horizontal and vertical addresses in the video memory 210 can be changed if the data in the RAMs 206 and 207 are rewritten. This allows an image being displayed to be moved in the horizontal and vertical directions, enlarged, reduced, or otherwise modified. It should be noted that the system 200 can move an image only on the column or line basis of the video memory 210.

To rewrite the data stored in the conversion RAMs 206 and 207, the microprocessor 212 causes the horizontal and vertical address bus switches 204 and 205 to connect the address bus of the microprocessor 212 to the address buses of the RAMs 206 and 207. Also, the microprocessor 212 causes the horizontal and vertical memory address switches 208 and 209 to connect the data bus of the microprocessor 212 to the data buses of the RAMs 206 and 207. In this condition, the microprocessor 212 rewrites the data stored in the RAMs 206 and 207. Thereafter, the microprocessor 212 again connects the switches 204 and 205 to the address counters 202 and 203 and the switches 208 and 209 to the address buses of the video memory 210. In the illustrative embodiment, the switches 204, 205, 208 and 209 may each be implemented as a switch or a gate, as desired.

FIG. 5 shows a specific condition wherein the the second and 640-th line of the vertical address conversion RAM 207 are replaced with each other. In this case, all that is required is to substitute the data at the addresses 000000001 and 101111111 of the RAM 207 for each other. The data stored in the other RAM 206 remain in the same condition shown in FIG. 4A.

As shown in FIG. 6, when it is desired to double the size of an image, table data are written to the horizontal conversion RAM 206, as follows:

```
(address : data) = (000H : 000H), (001H : 000H),
                   (002H : 001H), (003H : 001H),
                   ..., (27FH : 13 FH)
```

As a result, the display addresses in the horizontal direction are sequentially incremented by 1 (one) for 2 dots, as shown in FIG. 7. The image is, therefore, doubled in size in the horizontal direction. Likewise, table data are written to the vertical address conversion RAM 207, as follows:

```
(address : data) = (000H : 000H), (001H : 000H),
                   (002H : 001H), (003H : 001H),
                   ..., (18FH : OC7H)
```

Then, as shown in FIG. 7, the display addresses in the vertical direction are sequentially incremented by 1 for 2 lines, doubling the image size in the vertical direction.

To halve the image size, table data are written to the RAMS 207 and 207, as shown below:

```
RAM 206:  (address : data) = (000H : 000H),
                             (001H : 002H),
                             (002H : 004H),
                             (003H : 006H),
                             ..., (27FH:4FEH)
RAM 207:  (address : data) = (000H : 000H),
                             (001H : 002H),
                             (002H : 004H),
                             (003H : 006H),
                             ... (18FH : 31EH)
```

In this case, the horizontal and vertical display addresses are sequentially incremented by 2 for one 1 dot each. As a result, the horizontal and vertical addresses and, therefore, the image size is halved.

By the procedure described above, an image being displayed on the display 214 can be moved in the horizontal and vertical directions, enlarged, reduced, or otherwise manipulated, as desired.

The display 214 has a resolution which is 640 dots in the horizontal direction and 400 lines in the vertical direction (see FIG. 7), as stated earlier. The horizontal and vertical display addresses, therefore, need 10 bits and 9 bits, respectively. It follows that the RAMs 206 and 207 need respectively only the capacity of 640 $\times$ 10 = 6,400 bits and the capacity of 400 $\times$ 9 = 3, 600 bits, i. e., the total capacity is only 10, 000 bits which is far smaller than the conventional capacity which is 4, 608, 000 bits.

As stated above, the image display system 200 divides display addresses in the horizontal and vertical directions, connects a horizontal and a vertical address conversion RAM to display address buses, and converts the display addresses in the horizontal and vertical directions. The system 200, therefore, can shift, enlarge, reduce or otherwise modify an image while noticeably reducing the required capacity of the RAMSs.

The system 200 described above changes the display addresses by use of a single video memory to thereby change a particular condition of a single image such as the position or the size. Hence, the system 200 is not practicable with two or more images.

Referring to FIG. 8, an alternative embodiment of the present invention will be described which is capable of handling two different images at the same time. As shown, the image display system or multi-display system, generally 800, has a display clock generator 801. A horizontal and a vertical address counter 802 and 803 each receives the display clock and outputs a horizontal or vertical display address. A first and a second horizontal display address conversion RAM 806 and 814 each has an address input to which the horizontal display address is connected. A first and a second vertical display conversion RAM 807 and 815 each has an address input to which the vertical display address is connected. A first and a second video memory 810 and 818 are connected at the lower side of the address inputs thereof to the data buses of the horizontal address conversion RAMs 806 and 814, respectively, and at the upper side of the same to the data buses of the vertical address conversion RAMs 807 and 815, respectively. These video memories 810 and 818 deliver video data to the associated data buses. A controller 820 rewrites data stored in the RAMs 806, 807, 814 and 815, as needed. A first and a second address switch 804 and 812 are respectively connected to the RAMs 906 and 814, and each selects either one of the address bus extending from the horizontal display address counter 802 and the address bus extending from the controller 820. A first and a second address bus switch 805 and 813 are respectively connected to the RAMs 807 and 815, and each selects either one of the address bus extending from the controller 820 and the address bus extending from the vertical display address counter 803. A first and a second data bus

switch 808 and 816 are respectively connected to the RAMs 806 and 814, and each selects either one of the data bus to the video memory 810 or 818 and the data bus to the controller 820. A first and a second data bus switch 809 and 817 are respectively connected to the RAMs 807 and 815, and each selects either one of the data bus to the video memory 810 or 818 and the data bus to the controller 820. An AND gate 821 produces AND of additional bits provided in conversion table data of the RAMs 806 and 807, as will be described. A second AND gate 822 ANDs the additional bits provided in the conversion table data of the RAMS 814 and 815. A first and a second analog switch 811 and 819 are turned on and off by the AND gates 821 and 822, respectively. The additional bits are added to the uppermost bits of the horizontal and vertical display addresses. Therefore, the inputs of the AND gates 821 and 822 are connected to the uppermost bits of the address buses.

In operation, the horizontal and vertical address counters 820 and 803 each generates a horizontal or vertical display address in response to the display clock from the clock generator 801. The horizontal and vertical display addresses are respectively routed through the first horizontal and vertical address bus switches 804 and 805 and the second horizontal and vertical address bus switches 812 and 813 to the fist horizontal and vertical address conversion RAMs 806 and 807 and the second horizontal and vertical address conversion RAMs 814 and 815. In response, the RAMs 806 and 807 and the RAMs 814 and 815 convert the input display addresses on the basis of data stored therein. The resulting outputs of the RAMs 806, 807, 814 and 815 are respectively routed through the associated data bus switches 808, 809, 816 and 817 to the lower and upper addresses of the first video memory 810 and the lower and upper addresses of the second video memory 818. As a result, video data are fed from the video memories 810 and 818 to a display, not shown.

Assume that the resolution of the display is 640 dots (horizontal) $\times$ 400 lines (vertical). Then, the horizontal address conversion RAMS 814 and 816 each needs 10 bits since it counts up to 640 dots, while the vertical address conversion RAMs 807 and 815 each needs 9 bits since it counts up to 400 lines. In the illustrative embodiment, each of the horizontal and vertical address conversion RAMs is provided with an additional bit indicative of the display timing of a particular image. When the additional bits of the associated RAMs both are 1, image data is applied to the display; when either one of them is 0, the output of image data is inhibited. For this purpose, the analog switches 811 and 819 are respectively connected to the image data outputs of the video memories 810 and 818 and have their outputs commonly connected to the display.

FIGS. 9A and 9B show respectively the additional bits for implementing the above-stated control and specific images appearing on a screen 900. At the timing for horizontal and vertical display, 1 is written to the additional bits I and II of the first horizontal and vertical address conversion RAMs 806 and 807 and to the additional bits III and IV of the second horizontal and vertical address conversion RAMs 814 and 815; at the other timings, 0 is written to the additional bits I-IV. In the specific condition shown in FIGS. 9A and 9B, "00110000" is written to the additional bit I of the RAM 806, "00001100" is written to the additional bit II of the RAM 807, "00000110" is written to the additional bit III of th RAM 14, and "00110000" is written to the additional bit IV of the RAM 815. When the additional bits I and II of the RAMs 806 and 807 both are 1, the analog switch 811 is turned on to deliver video data from the video memory 810 to the display with the result that a first image 901 appears on the display. When the additional addresses III and IV of the RAMs 814 and 815 both are 1, the analog switch 819 is turned on to deliver video data from the video memory 818 to the display with the result that a second image 902 appears on the display.

In the manner described above, the first and second images 900 and 901 appear on the screen 900 at the same time.

In summary, the multi-display system 900 described above assigns an additional bit representative of an image display timing to each of conversion table data stored in horizontal and vertical address conversion RAMs which are connected to particular one of a plurality of video memories, thereby controlling the output timing of image data. The system 900, therefore, allows video data from a plurality of video memories to be displayed in combination on a single screen, as desired.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

Claims

1. An image display system comprising:

a horizontal display address counter for outputting a horizontal display address in response to a display clock;

a vertical display address counter for outputting a vertical display address in response to said

display clock;

a horizontal display address conversion memory having an address input to which said horizontal display address is connected;

a vertical display address conversion memory having an address input to which said vertical display address is connected;

a video memory having address inputs to which a data bus from said horizontal display address conversion memory and a data bus from said vertical display address conversion memory are connected, said video memory outputting video data on the basis of the input addresses; and

rewriting means for rewriting data stored in said horizontal and vertical display address conversion memories.

2. A system as claimed in claim 1, wherein said rewriting means comprises:

a microprocessor;

a horizontal display address bus switch for selecting either one of an address bus from said horizontal display address counter and an address bus from said microprocessor;

a vertical display address bus switch for selecting either one of an address bus from said vertical display address counter and the address bus from said microprocessor;

a horizontal memory address switch connected to said horizontal display address conversion memory for selecting either one of a data bus to said video memory and a data bus to said microprocessor; and

a vertical memory address switch connected to said vertical display address conversion memory for selecting either one of a data bus to said video memory and said data bus to said microprocessor.

3. A system as claimed in claim 2, wherein said microprocessor controls said horizontal display address bus switch, said vertical display address bus switch, said horizontal memory address switch, and said vertical memory address switch and rewrites data stored in said horizontal display address conversion memory and data stored in said vertical display address conversion memory.

Fig. 1

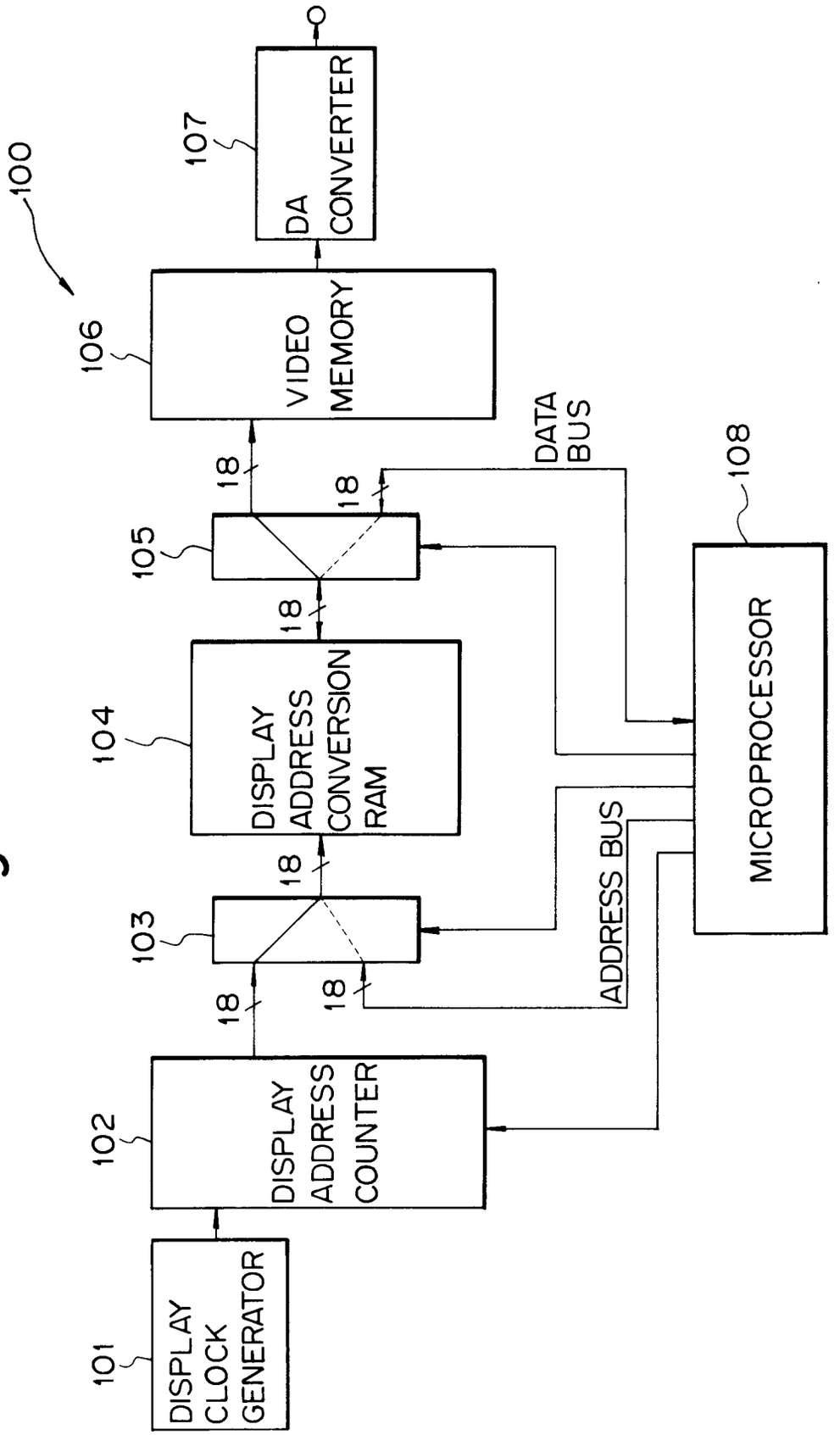

100
101
DISPLAY CLOCK GENERATOR
102
DISPLAY ADDRESS COUNTER
103
104
DISPLAY ADDRESS CONVERSION RAM
105
106
VIDEO MEMORY
107
DA CONVERTER
O
18
ADDRESS BUS
DATA BUS
108
MICROPROCESSOR

Fig. 2

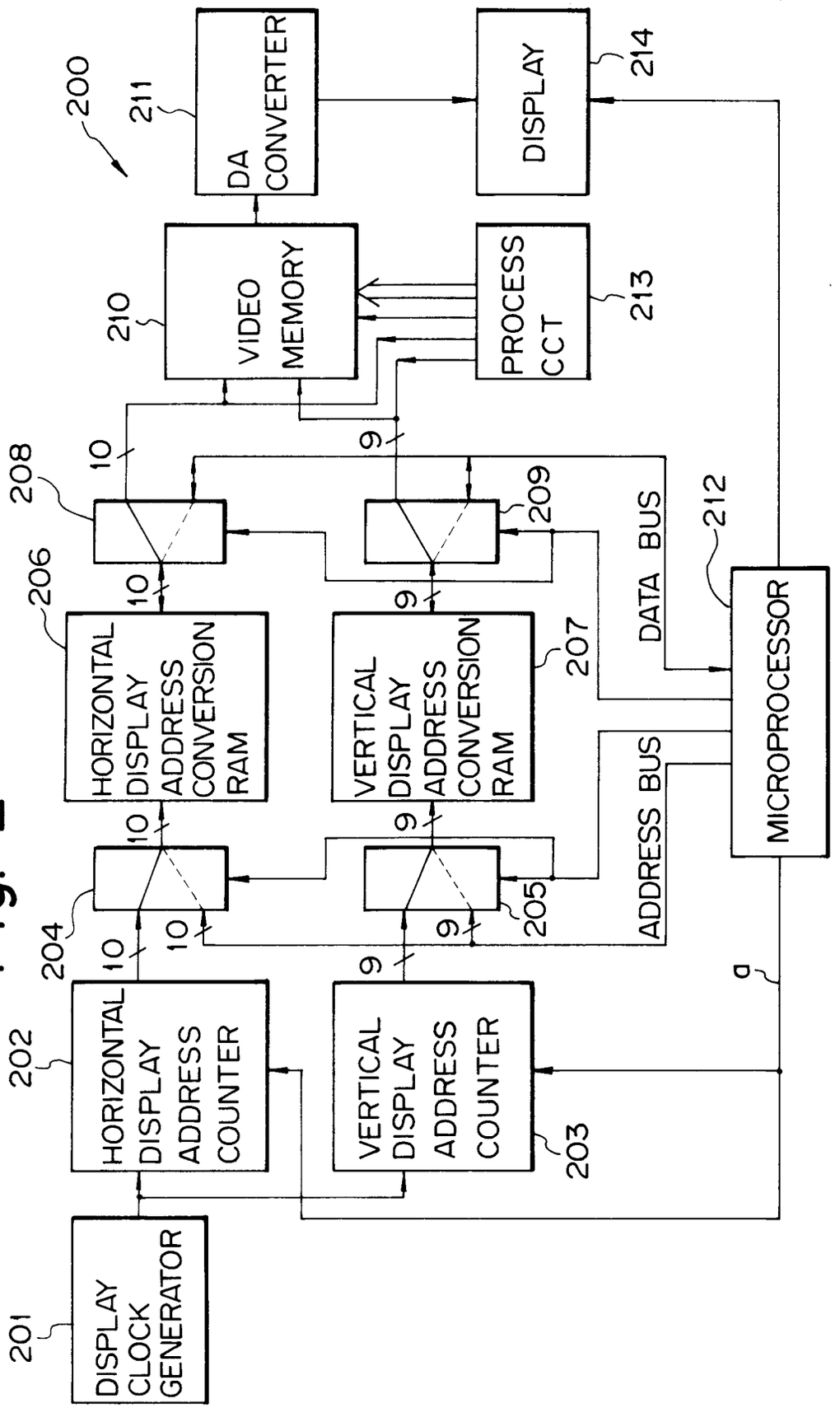

200
211
DA CONVERTER
DISPLAY
214
210
VIDEO MEMORY
PROCESS CCT
213
208
209
206
HORIZONTAL DISPLAY ADDRESS CONVERSION RAM
VERTICAL DISPLAY ADDRESS CONVERSION RAM
207
DATA BUS
212
MICROPROCESSOR
204
205
ADDRESS BUS
202
HORIZONTAL DISPLAY ADDRESS COUNTER
VERTICAL DISPLAY ADDRESS COUNTER
203
201
DISPLAY CLOCK GENERATOR
10
9
q

Fig. 3

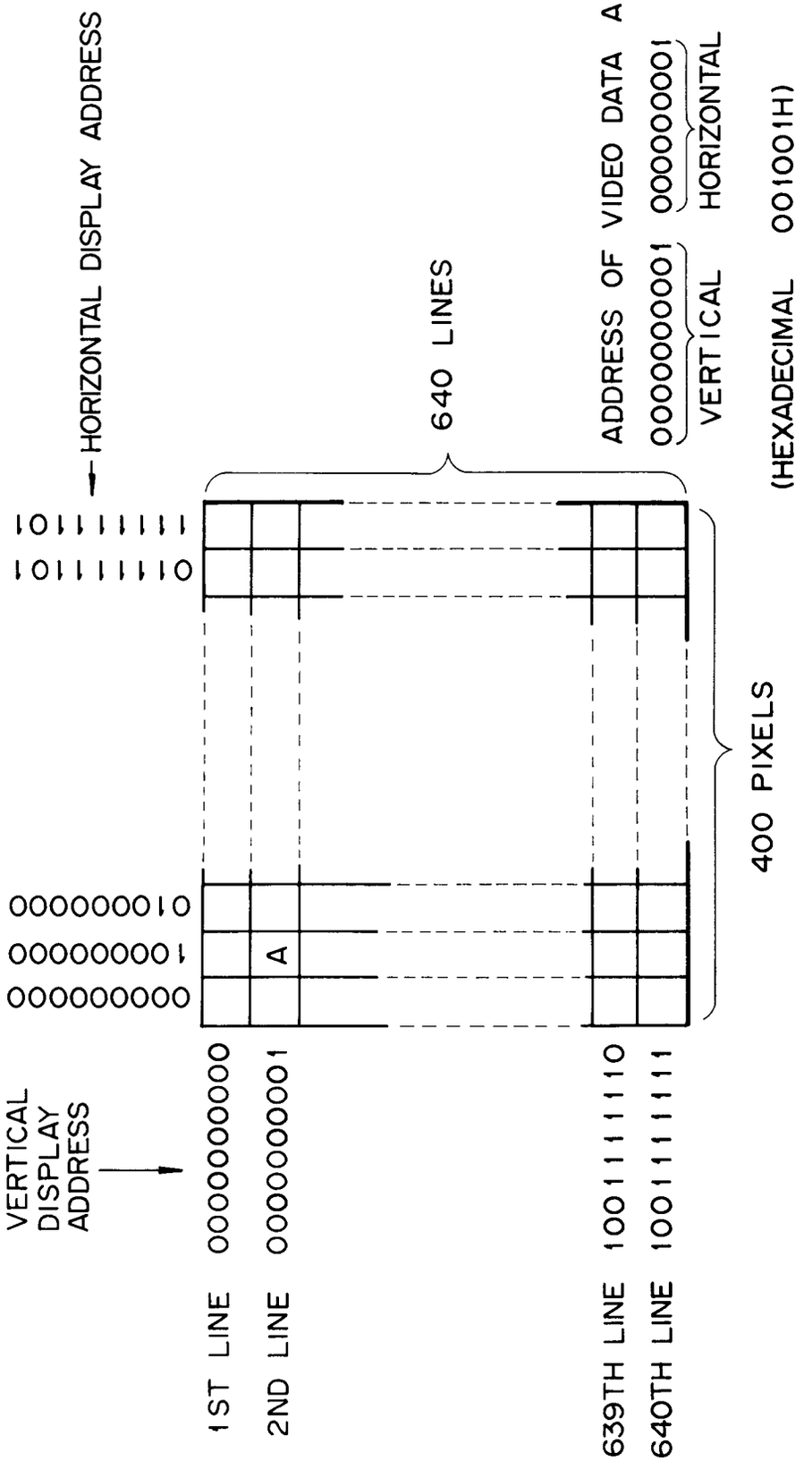

HORIZONTAL DISPLAY ADDRESS
1011111111
1011111110
640 LINES
ADDRESS OF VIDEO DATA A
0000000001 0000000001
VERTICAL HORIZONTAL
(HEXADECIMAL 001001H)
00000010
00000001
000000000
A
400 PIXELS
VERTICAL DISPLAY ADDRESS
1ST LINE 0000000000
2ND LINE 0000000001
639TH LINE 1001111110
640TH LINE 1001111111

Fig. 4A

COUNTER 202 OUTPUT	RAM 206 DATA (HIRIZONTAL DISPLAY ADDRESS)
0000000000	0000000000
0000000001	0000000001
0000000010	0000000010
0000000011	0000000011
⋮	⋮
1001111110	1001111110
1001111111	1001111111

Fig. 4B

COUNTER 203 OUTPUT	RAM 207 DATA (VERTICAL DISPLAY ADDRESS)
0000000000	0000000000
0000000001	0000000001
0000000010	0000000010
0000000011	0000000011
⋮	⋮
1011111110	1011111110
1011111111	1011111111

Fig. 5

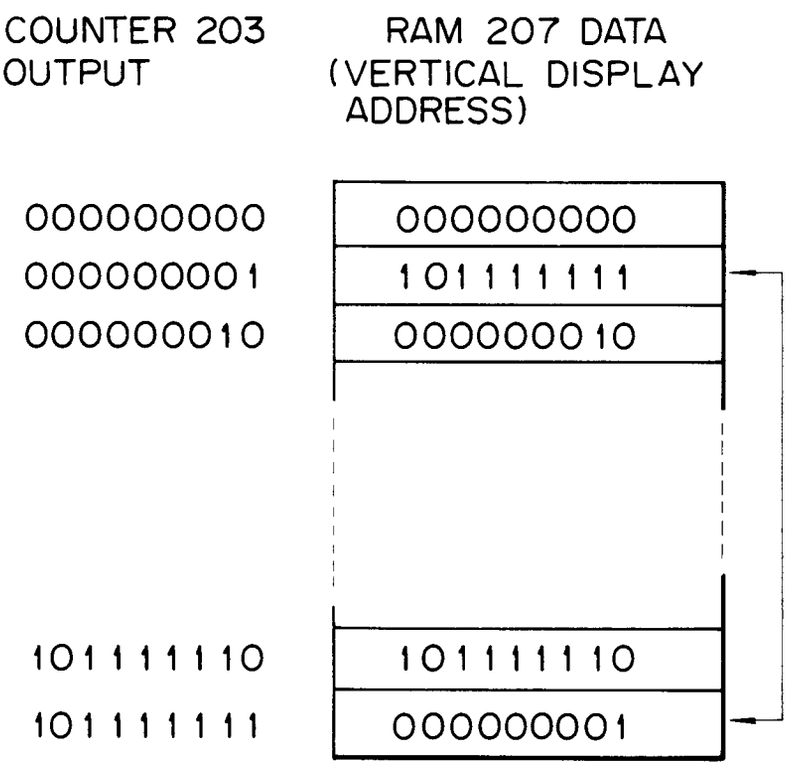

COUNTER 203 OUTPUT
RAM 207 DATA (VERTICAL DISPLAY ADDRESS)
000000000
000000001
000000010
101111110
101111111
000000000
101111111
000000010
101111110
000000001

Fig. 6

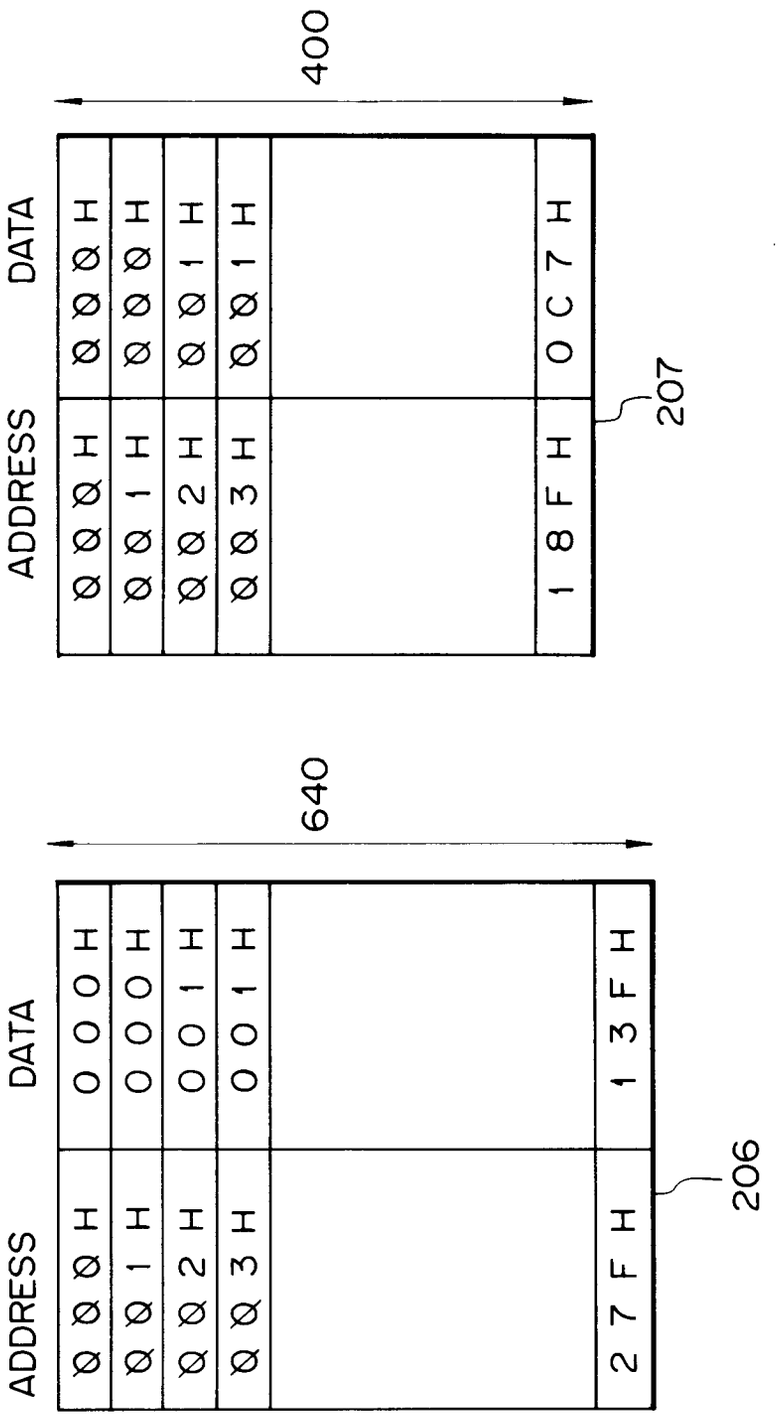

400
ADDRESS
DATA
0000H
0000H
0001H
0002H
0003H
18FH
0C7H
207
640
ADDRESS
DATA
0000H
0001H
0002H
0003H
27FH
13FH
206

Fig. 7

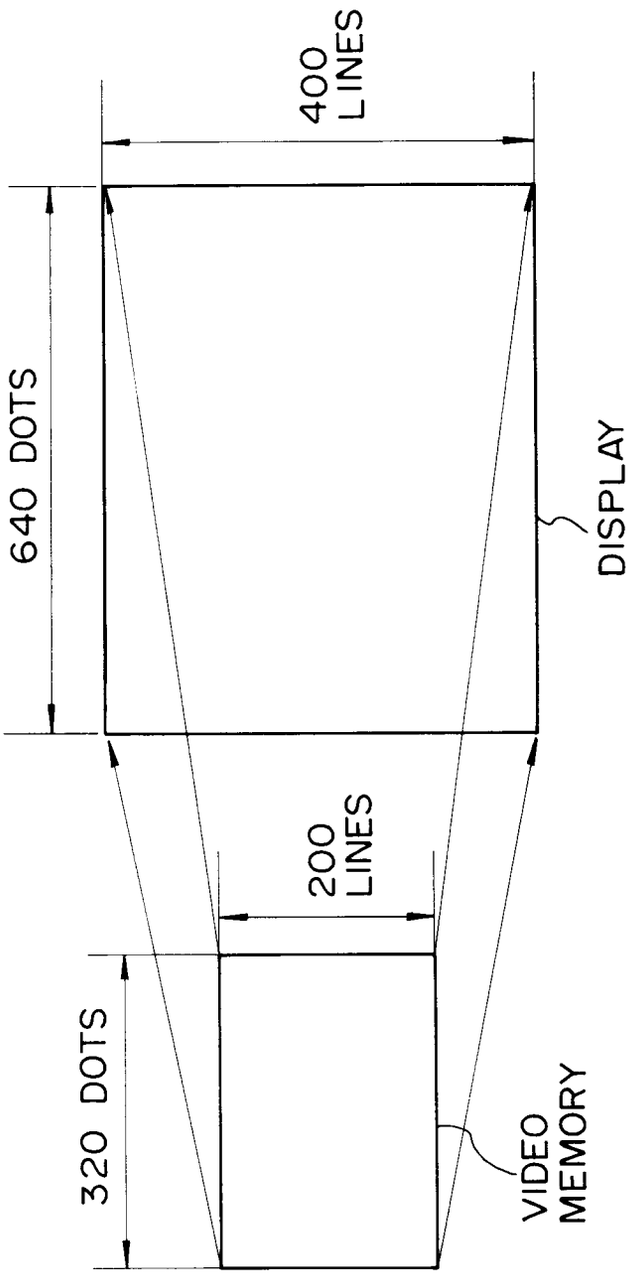


Fig. 8

Fig. 8A	Fig. 8B

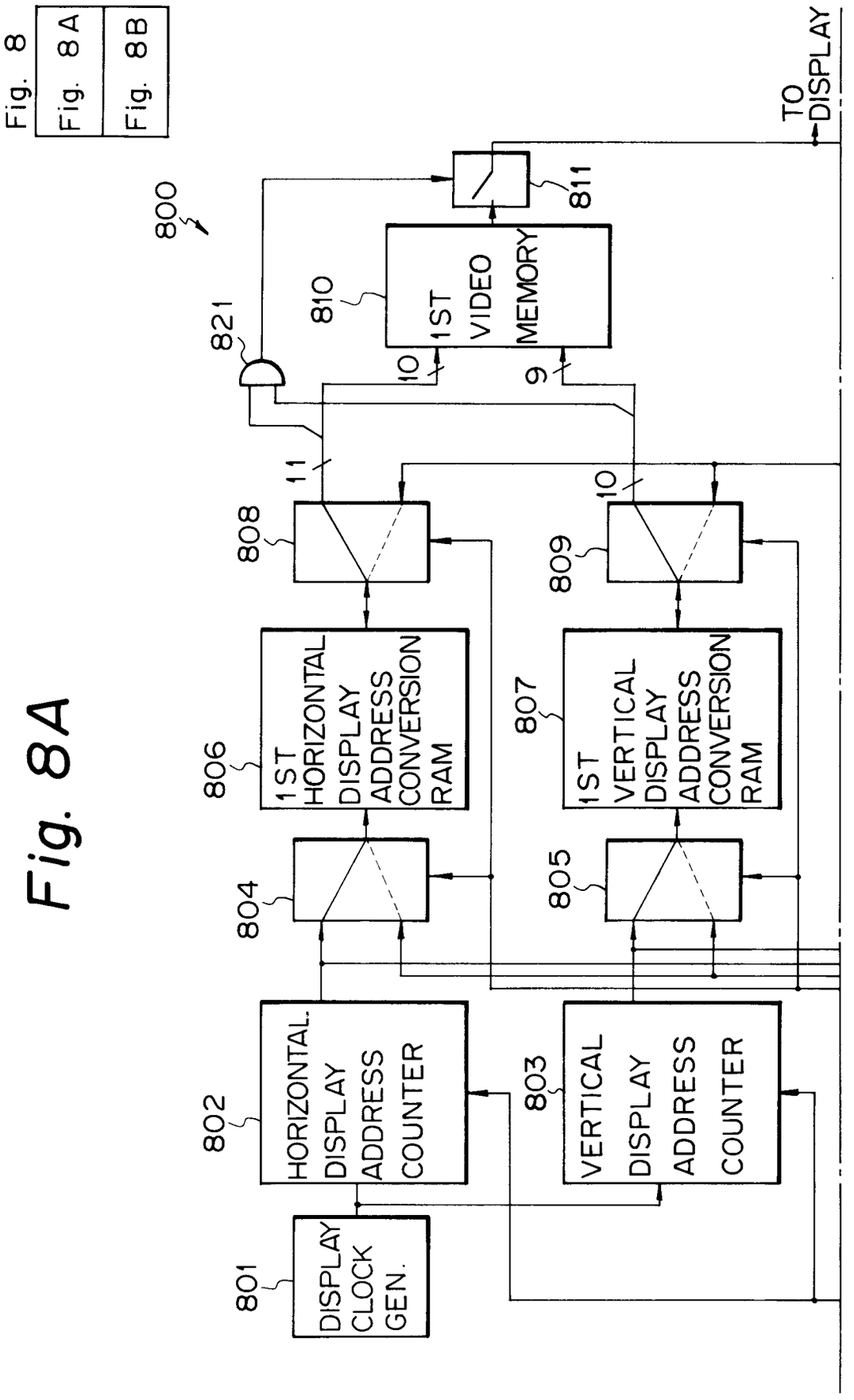


Fig. 8A

Fig. 8B

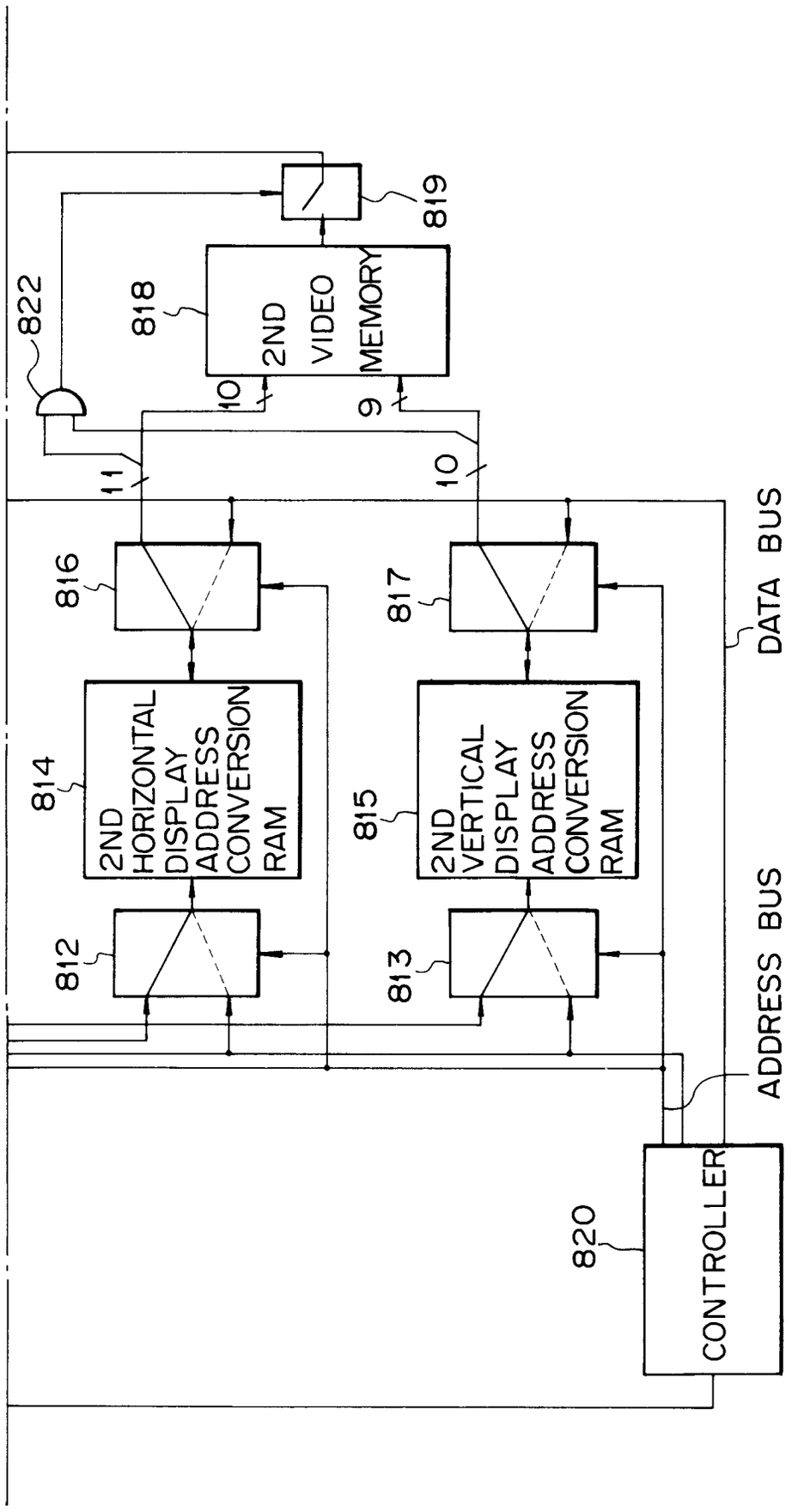

819
822
818
2ND VIDEO MEMORY
10
9
11
10
816
817
814
2ND HORIZONTAL DISPLAY ADDRESS CONVERSION RAM
815
2ND VERTICAL DISPLAY ADDRESS CONVERSION RAM
812
813
DATA BUS
ADDRESS BUS
820
CONTROLLER

Fig. 9A

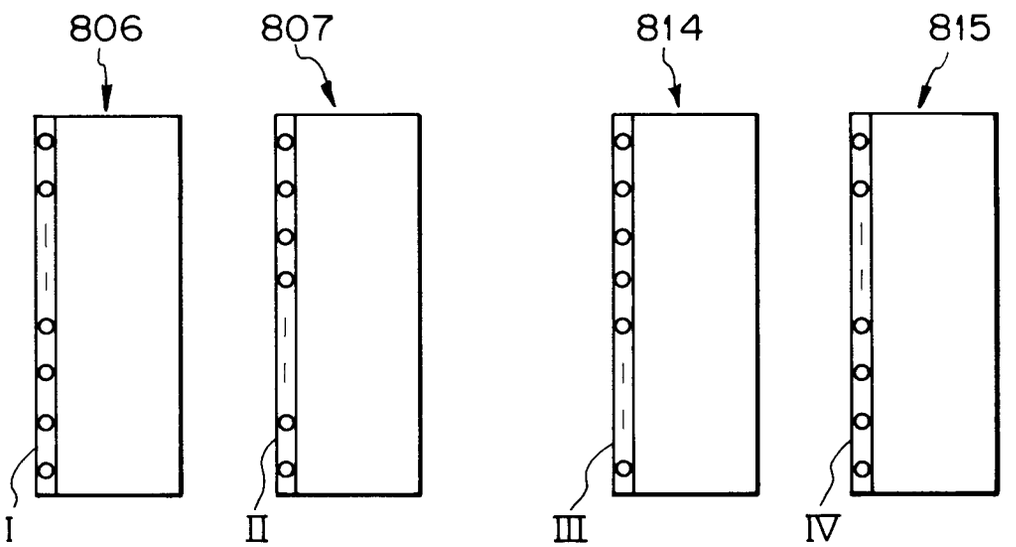


Fig. 9B