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(71) Applicant: **ACER INCORPORATED**
347 Chung Feng Road
Lungtan, Taoyuan 32514(TW)

(72) Inventor: **Yu, Chien-Chih**
347 Chung Feng Road
Lungtan, Taoyuan 32514(TW)

(74) Representative: **Luckhurst, Anthony Henry William et al**
MARKS & CLERK 57-60 Lincoln's Inn Fields
London WC2A 3LS(GB)

(54) **Video memory system with intermediate buffer.**

(57) A video memory system is disclosed including a video memory 38, an intermediate buffer 34, a video display control unit (VDUC) 42, and a video processing means 39. The intermediate buffer 34 is disposed between an external CPU 30 and the video memory 38 to intercept the address 31, data 32, and read/write signals 33 from the CPU. For read operations, signals to the video memory 38, and the data read therefrom travel through the buffer 34 to arrive at the CPU 30. For write operations, the intermediate buffer 34 stores the address and data signals from the CPU 30. The data is later written into the video memory 38 in response to a time slot reference signal 52.

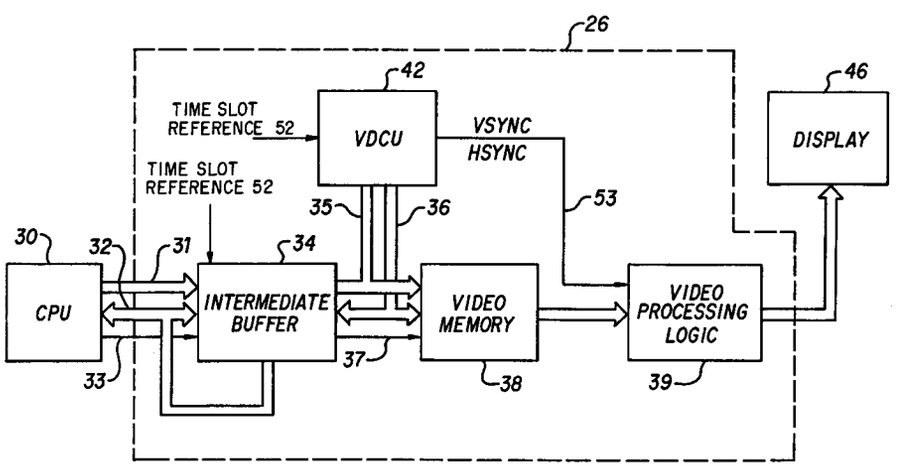

FIG. 3

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The present invention relates to a computer display memory system, and more specifically, to such a system including an intermediate buffer which substantially reduces the memory accessing time of an external processing unit by eliminating the need to insert wait cycles.

Many computer display systems today include a video memory system for storing the data which represents the image to be displayed. In Fig. 1, a typical video memory system 20 is illustrated, comprising a video memory 12, a video display control unit (VDCU) 14, and a video processing means 15. The external processing unit (CPU) 10 sends data and control signals to the video memory 12 to update the information stored therein. The VDCU 14 periodically causes the memory 12 to output data to the video processing means 15. Video processing means 15 then converts the data into signals that the external display means 16 can recognize, and outputs these signals to the display means 16 in response to the control signals on lines 17 from VDCU 14. In this manner, the information on the display screen is periodically refreshed. The video memory system 20 may either be incorporated directly into the motherboard of a host computer (not shown) or may take the form of an add-on card. Its general operation is substantially the same for either configuration.

As shown in Fig. 1, both the CPU 10 and the VDCU 14 of a typical video memory system have direct access to the memory 12. As a result, a method is needed to designate the time slots during which the CPU 10 and the VDCU 14 may respectively access the memory 12. Otherwise, they may try to access the memory simultaneously, an undesirable result. Time allocation is commonly achieved through the use of a time slot reference signal such as that shown in Fig. 2A wherein CPU 10 may only access the memory 12 between times t_1 and t_3 and between times t_5 and t_6. The time slots between t_3, t_5 and between t_6, t_7 are allocated to VDCU 14. This type of procedure inherently introduces delays into the system. To illustrate this point, suppose that the CPU 10 pulls its read/write line low (not shown in Fig. 1) when it is ready to write a set of data to memory 12. As long as the read/write line is pulled low at the beginning of a CPU time slot (times t_1 or t_5 of Fig. 2A), the write operation is performed without delay (Fig. 2B). However, for the general case where the read/write signal is not synchronized with the beginning of a CPU time slot, the CPU must insert wait cycles in order to properly access the memory. For example, if the CPU wishes to write to the memory during a VDCU time slot as shown in Fig. 2C, it must insert wait cycles between times t_4 and t_6 to hold the read/write line low in order to ensure that data is written properly into the memory 12. Also, if the read/write line is pulled low during a CPU time slot but the remaining time is insufficient to complete the write operation (Fig. 2D), the CPU must insert wait cycles to hold the read/write line low until the end of the next CPU time slot t_6. The introduction of these wait cycles causes substantial delays. Thus, there exists a need for a video memory system that allows the CPU to perform its function without the need to insert wait cycles.

The present invention eliminates the need to insert wait cycles for write operations by interposing an intermediate buffer, between the CPU and the video memory, which functions to intercept the address, data, and control signals from the CPU. For read operations, the buffer simply relays the intercepted address signals directly to the video memory. For write operations, however, the buffer stores the address and data sent by the CPU and retains this information within its memory until the beginning of the next CPU time slot, at which time it accesses the video memory via the stored address and writes the data thereto. The invention allows the CPU to perform write operations regardless of whether the time slot is a CPU time slot, thereby, obviating the need to introduce wait cycles. It is true that wait cycles may still need to be inserted for read operations, but since eighty percent of the operations performed by the CPU are write operations and only twenty percent are read operations, the present invention nonetheless saves the CPU a substantial amount of time. The invention is likewise applicable to avoid wait cycles during read operations as well.

A preferred embodiment of the invention comprises a memory means, a VDCU connected to the memory means, a video means connected to both the memory means and the VDCU, and an intermediate buffer interposed between an external CPU and the memory means. The external CPU operates to generate a read/write control signal and address and data signals. The intermediate buffer intercepts these signals, and if a write operation is desired, the address and data signals are stored in the buffer. The buffer then monitors the time slot reference signal until it detects a CPU time slot, at which time, the address and data signals are sent to the memory means. The memory means then stores the data signals at the addresses indicated by the address signals. For read operations, the intermediate buffer simply relays the address signals to the memory means.

Fig. 1 is a block diagram of a prior art video memory system.

Fig. 2A shows a typical time slot reference signal employed to designate time slots during which the CPU and the VDCU may access the video memory used in the system of Fig. 1.

Figs. 2B-2D show the possible time variations between the read/write signal from the CPU and the time slot reference signal in the system of Fig. 1.

Fig. 3 is a functional block diagram of a video memory system to illustrate the invention.

Fig. 4 shows a preferred embodiment of the system of Fig. 3.

A block diagram depicting the basic components of the invention is shown in Fig. 3, comprising intermediate buffer 34, random access video memory 38, VDCU 42, and video processing means 39. Video memory 38, VDCU 42, and video processing means 39 are of regular construction and are found in many typical prior art computer display systems; thus, they will not be discussed in detail herein. The external CPU 30 sends data, representing a portion of the image to be displayed, to the video memory 38 where the information is stored. This continues until the entire image is stored within the video memory 38. Thereafter, the main function of CPU 30 is to update the stored image. To update a portion of the video memory 38, the CPU sends out an address on lines 31 and a read/write control signal on line 33 indicating the nature of the operation. For write operations, CPU 30 also sends out data signals on data lines 32.

Address lines 31, data lines 32, and control line 33 are all connected to intermediate buffer 34. A time slot reference signal 52 such as that shown in Fig. 2A, dictating the times during which the CPU 30 and the VDCU 42 may access video memory 38, is also supplied to intermediate buffer 34. Depending on the status of the read/write line 33, buffer 34 performs different functions.

For read operations, buffer 34 receives a read address on lines 31 and a read signal on line 33. The internal logic of buffer 34 reads the signal on control line 33 and, realizing that a read operation is desired, relays the read address to memory 38 via memory address lines 35. Also, the read/write control signal is relayed to memory 38 via memory control line 37. Data from the addressed location in the video memory 38 is then put onto the memory data lines 36, said data travelling from the memory 38 through buffer 34 to eventually arrive at CPU 30 via CPU data lines 32. Since the intermediate buffer 34 only acts as a relay for read operations, CPU 30 is responsible for ensuring that a read operation only takes place during a time slot which has been allocated to the CPU. Otherwise, bus conflict with the VDCU 42 may result. Thus, wait cycles may need to be inserted for read operations. However, since only about twenty percent of the CPU's operations are read operations, the delaying effect of the wait cycles is not significant.

During write operations, the CPU 30 sends to the intermediate buffer 34 a write address on lines 31, write data on lines 32, and a write control signal on line 33. The internal logic of buffer 34 receives the write control signal and responds by initiating a series of operations. The internal logic first scans the memory portion of the buffer 34 to ascertain which locations may be written into. Once an appropriate location is found, the address and data signals on lines 31 and 32, respectively, are stored. Thereafter, the internal logic checks the status of the time slot reference signal 52 to ascertain whether it indicates a CPU time slot. If so, the stored address and data signals are put onto lines 35 and 36, respectively, and a write control signal is sent on line 37. This results in the data being written into the appropriate address in video memory 38. However, if signal 52 indicates a VDCU time slot or if there is insufficient time to complete a write operation to the memory, the buffer 34 will wait until the beginning of the next CPU time slot to write the data to the memory 38. Since several sets of addresses and data may be stored by the buffer 34 before the next CPU time slot, the intermediate buffer 34 preferably outputs stored data in a first-in-first-out (FIFO) fashion so that no data remains within the buffer 34 for an extended period of time. Once the data in memory 38 is updated during a CPU time slot, the VDCU, during the next VDCU time slot, causes the updated data to be transferred from the memory 38 to the video processing means 39. The video processing means in turn converts the data into video signals and, in response to the control signals from VDCU 42 on lines 53, outputs the video signals to an external display means 46, thereby, refreshing the display screen with updated data.

Note that due to the presence of intermediate buffer 34, the CPU 30 need not generate any wait cycles. It is free to perform write operations at any time without regard to the status of the time slot reference signal 52. The waiting formerly performed by the CPU is now done by the intermediate buffer. This significantly reduces the memory access time of the CPU and allows it to run more efficiently.

A preferred embodiment of intermediate buffer 34 is illustrated in more detail in Fig. 4, comprising buffer register means 60, control means 70, and a read/write multiplexer 80. Buffer register means 60 contains a plurality of storage registers 62 with each register capable of storing a set of address and data signals. Register means 60 receives as input CPU address lines 31, CPU data lines 32, read/write control line 33, and several control lines 65 from control means 70. In response to a write signal on line 33, register means 60 stores within one of its registers 62 the address and data signals

appearing on lines 31 and 32. This occurs irrespective of the status of the time slot reference signal 52. The specific register in which the data is stored is dictated by the control signals on lines 65 sent by control means 70. The data remains stored until a WRITE DATA signal on lines 65 instructs the register means 60 to output data from one of its registers. Again, the control signals on lines 65 specify which register is to be accessed.

The read/write multiplexer 80 is attached to two sets of input lines, one set from register means 60 and the other set from the CPU 30. Multiplexer 80 receives from register means 60 address lines 74 and data lines 75. Multiplexer 80 also receives a write control signal on line 78 from control means 70. From the CPU 30, multiplexer 80 receives address lines 31, data lines 32, and read/write line 33. In response to a MUX control signal from control means 70 on line 68, multiplexer 80 behaves as a switch to selectively connect one of the sets of input lines to the address lines 35, data lines 36, and read/write line 37 of the video memory 38. Thus, by using line 68, control means 70 can control which device (the CPU or the register means) is connected to the video memory 38.

The control means 70 receives as inputs the CPU read/write control signal on line 33, buffer register status signals on lines 81, and the time slot reference signal on line 52. From these inputs signals, the internal logic of the control means 70 generates the appropriate signals to control the register means 60 and the read/write multiplexer 80. To ensure that a register 62 containing fresh data is not overwritten, control means 70 must monitor the status of the registers 62. This may be achieved through the use of a status register 66 which receives, as inputs, buffer register status signals on lines 81 from register means 60. Register 66 preferably contains as many bits 67 as there are registers 62 in the register means 60 so that each bit 67 corresponds to a specific register 62. Consequently, each bit may be used as a flag to indicate whether the register contains fresh data. Whenever a register is written into, an appropriate signal is sent on lines 81 instructing control means 70 to set the flag corresponding to that register to indicate that the register is full. Conversely, if data is read out of a register, its corresponding flag is cleared by control means 70 in response to an appropriate signal on lines 81 from register means 60. Thus, by scanning the status register 66, control means 70 may quickly ascertain which register may be written into.

Control means 70 is also equipped with sequential logic means 72 so that it may perform the FIFO function. Each time data is written into register means 60, sequential logic 72 records the location of the register as well as the sequence in which each register 62 was loaded. This allows the data to be outputted in the same sequence as it was loaded. In other words, sequential logic 72 makes it possible to perform the desired first-in-first-out function. To output data, control means 70 checks the status of the time slot reference signal 52 to determine whether the status indicates a time slot allocated for the CPU. If so, a WRITE DATA signal is issued on one of the control lines 65 instructing the register means 60 to output a set of address and data signals. Sequential logic means 72 also sends out several control signals on lines 65 controlling the sequence in which the registers 62 are selected. Control means 70 then sends a MUX control signal on line 68 instructing multiplexer 80 to connect the output lines of register means 60 with the input lines of memory 38. The data on lines 75 is thus written into memory 38. For read operations, control means 70 instructs multiplexer 80 via line 68 to connect CPU 30 with the memory 38, thereby, allowing the CPU to read data from memory 38 through multiplexer 80.

Although the invention has been described with reference to a specific embodiment, it should not be construed to be so limited. It will be clear to one of ordinary skill in the art with the benefit of this disclosure that many modifications may be made without departing from the spirit of the invention. Thus, the video processing logic 15 and display 16 may, for example, be combined into a single unit if desired. The invention should not be limited by the specific embodiments used to illustrate them but only by the scope of the appended claims.

Claims

1. A video display memory system (26) which functions in response to a time slot reference signal (52), said system receiving address signals (31), data signals (32), and a first control signal (33) from an external processing means (34), said system comprising:

memory means (38) for receiving and storing bits of information;

video display control means (42) connected to said memory means (38) responsive to said reference signal (52) to periodically cause data from said memory means (38) to be outputted, wherein said reference signal (52) designates time slots allocated to said display control means (42) for accessing said memory means (38) and designates time slots allocated to said external processing means (30) for accessing said memory means (38), said video display control means (42) also operative to generate a set of video control signals (53);

a video means (39) for receiving and converting the periodically outputted data from

said memory means (38) into signals which are suitable for display purposes;

characterised by an intermediate memory buffer means (34), interposed between said external processing means (30) and said memory means (38), responsive to said first control signal (33) to store said address and data signals (31,32), said buffer means (34) outputting said stored address and data signals (31,32) to said memory means (38) during a time slot allocated by said reference signal (33) to said external processing means (30) for accessing said memory means (38).

2. A system according to claim 1, characterised in that said buffer (34) sends said address and data signals stored in the buffer to said memory means (38) during the next time slot allocated by said reference signal (52) to said external processing means (30) for accessing said memory means (38) to cause said data signals (32) to be stored within said memory means (38) at the address indicated by said address signals (31).

3. A system according to claim 1 or 2, characterised in that said first control signal (33) from said central processing means (30) indicates a write operation.

4. A system according to claim 1, 2 or 3, characterised in that said external processing means (30) generates a second control signal and said intermediate buffer means (34) responds to said second control signal to relay address signals to said memory means (38).

5. A system according to any one of claims 1 to 4, characterised in that said intermediate memory buffer means comprises (34):

logic means (70) for receiving said first and second control signals (33) and said reference signal (52), operative to generate a series of logic signals in accordance with said control and reference signals;

a buffer memory (60), having a plurality of storage registers, responsive to said logic signals to receive and store said address and data signals from said external processing means, said buffer memory (60) adapted to output said stored address and data signals at a subsequent time in response to said logic signals; and

means (80) connected to a first set of address and data lines (74,75) from said buffer memory (60) and a second set of address and data lines from said external processing means (31,32), for selectively connecting one of said first and second sets of address and data lines to the address and data lines of said memory means (38) in response to said logic signals.

6. A system according to claim 5, characterised in that said selectively connecting means (80) is a multiplexer.

7. A system according to claim 6 or 7, characterised in that said buffer memory (60) is further adapted to output buffer status signals (81) which are indicative of the status of the buffer registers (62) in said buffer memory (60).

8. A system according to claims 6, or 7, characterised in that said logic means (70) is further adapted to receive said buffer status signals (81) and to generate a series of sequential control signals (65, 72), said sequential signals being sent to said buffer memory (60) to cause said buffer memory (60) to output stored data in a first-in-first-out fashion.

9. A method for displaying the contents of a video memory (26) which comprises a memory means (38), said video memory (26) receiving a plurality of signals from an external processing unit (30), said method being characterised by the following steps:

intercepting address signals, data signals, and selected control signals (31,32,33) from said external processing unit (30);

determining from said control signals (33) whether the desired operation is a write operation;

storing said address and data signals (31,32) in a buffer register (34) when the desired operation is a write operation;

writing said stored data signals (32) into said memory means (38) at the address indicated by said stored address signals when the memory means (38) is accessible to receive said address and data signals; and

transferring the data stored within said memory means (38) to a video processing means (39) when said memory means is accessible by a display control means (42); and

transmitting said transferred data from said video processing means (39) to an external display means (46) to be displayed.

10. A method according to claim 9, characterised by additional steps of:

determining from said control signals (33) whether a read operation is desired; and

relaying said address signals (31) to said memory means (38) when the desired operation is a read operation.

11. A method according to claim 9 or 10, characterised in that said writing and transferring steps are performed in response to a time slot reference signal (52), said reference signal (52), designating time slots allocated for writing into said memory means (38) and time slots allocated for transferring data from said memory means (38).

12. A method according to claim 11, characterised in that said writing operation is performed during a time slot allocated for writing into said memory means, and said transferring operation is performed during a time slot allocated for transferring data from said memory means.

13. A method of claim 11 or 12, characterised in that said writing operation is performed during the time slot allocated for writing into said memory means (38) which immediately follows the storing operation.

14. A method for updating the contents of a video memory, said method reducing the accessing time between an external processing unit (30) and the memory means (38) in a video memory system (26), said method comprising the steps of:

intercepting address signals, data signals, and selected control signals (31,32,33) from said external processing unit (30);

determing from said control signals (33) whether the desired operation is a write operation;

storing said address and data signals (31,33) in a buffer register (34) when the desired operation is a write operation; and

writing said stored data signals (32) into said memory means (38) at said stored address when the memory means (38) is accessible to receive said address and data signals.

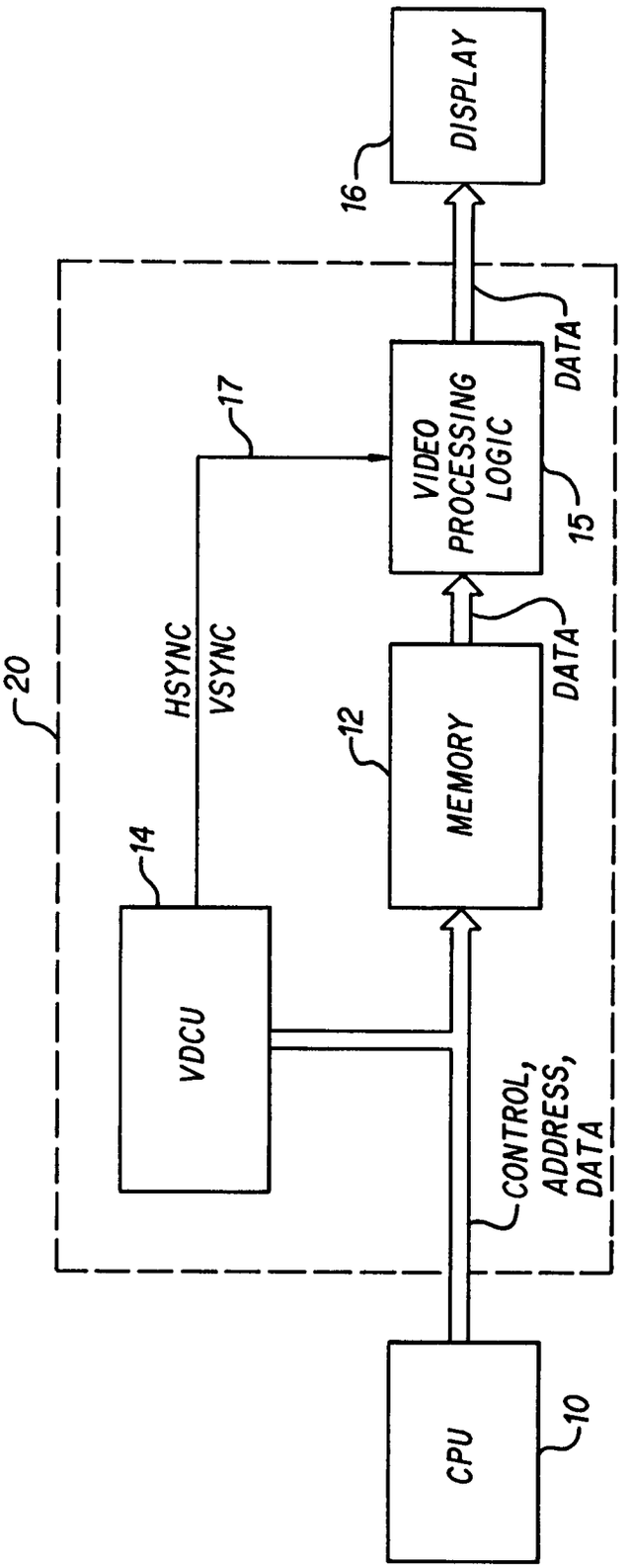

FIG. 1
(PRIOR ART)

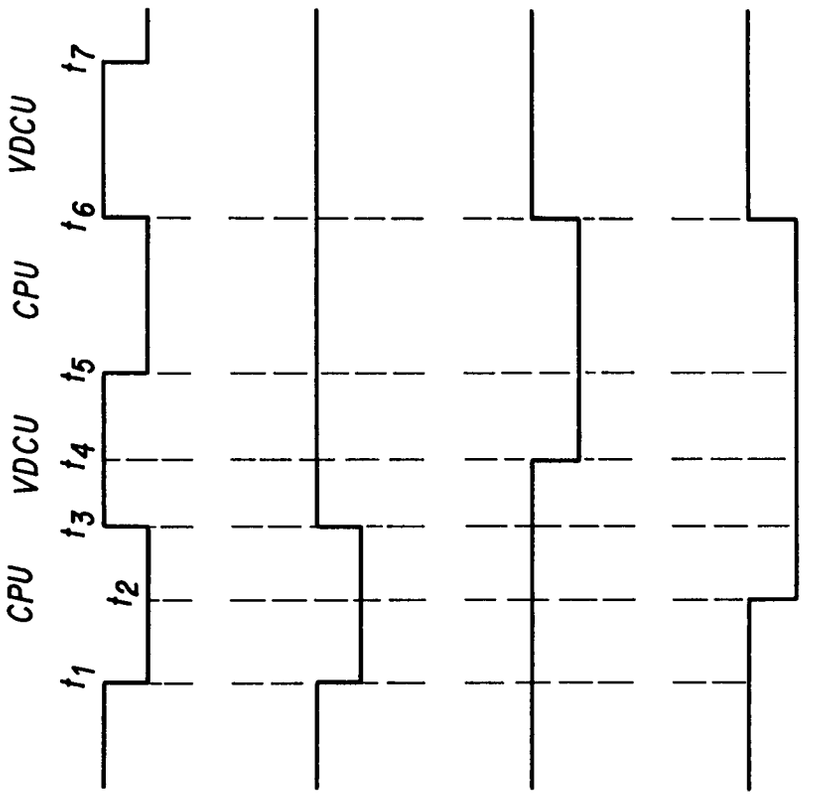

FIG. 2A

FIG. 2B

FIG. 2C

FIG. 2D

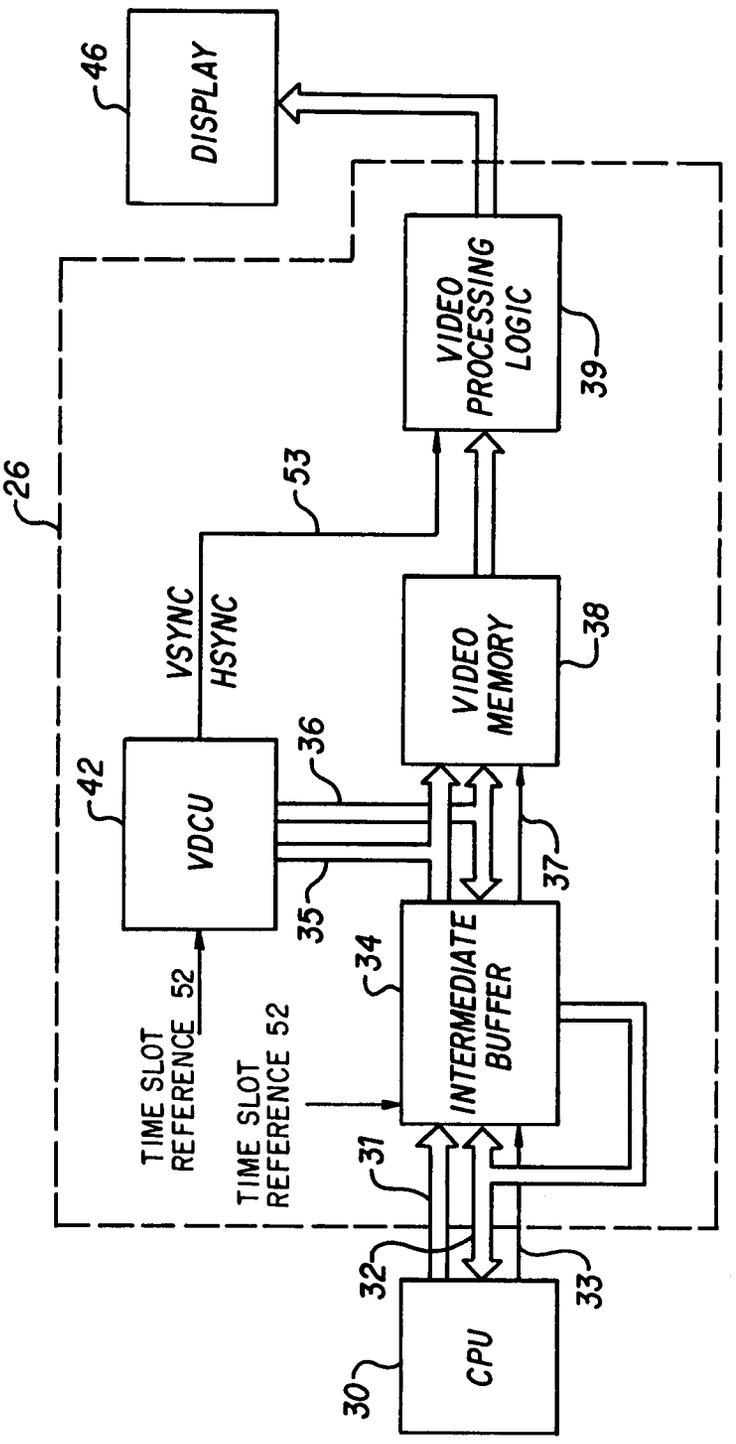
46
DISPLAY
VIDEO PROCESSING LOGIC
39
26
53
VSYNC
HSYNC
VIDEO MEMORY
38
42
VDCU
36
37
35
34
INTERMEDIATE BUFFER
TIME SLOT REFERENCE 52
TIME SLOT REFERENCE 52
31
32
33
30
CPU

FIG. 3

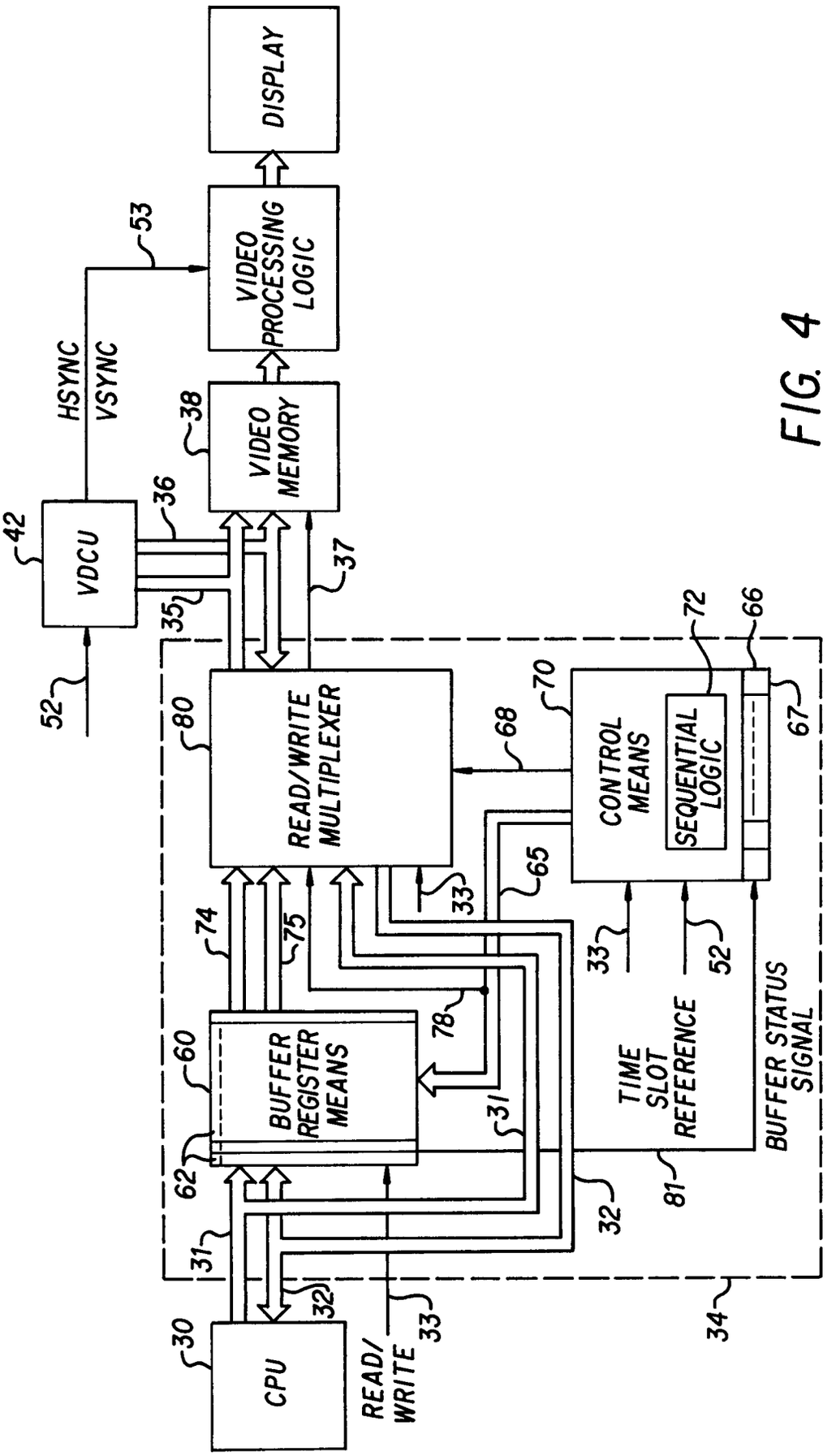
DISPLAY
VIDEO PROCESSING LOGIC
VIDEO MEMORY
VDCU
HSYNC
VSYNC
READ/WRITE MULTIPLEXER
CONTROL MEANS
SEQUENTIAL LOGIC
BUFFER REGISTER MEANS
TIME SLOT REFERENCE
BUFFER STATUS SIGNAL
CPU
READ/WRITE
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FIG. 4