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- ⁵⁴ Video memory system with intermediate buffer.
- © A video memory system is disclosed including a video memory 38, an intermediate buffer 34, a video display control unit (VDUC) 42, and a video processing means 39. The intermediate buffer 34 is disposed between an external CPU 30 and the video memory 38 to intercept the address 31, data 32, and read/write signals 33 from the CPU. For read oper-

ations, signals to the video memory 38, and the data read therefrom travel through the buffer 34 to arrive at the CPU 30. For write operations, the intermediate buffer 34 stores the address and data signals from the CPU 30. The data is later written into the video memory 38 in response to a time slot reference signal 52.

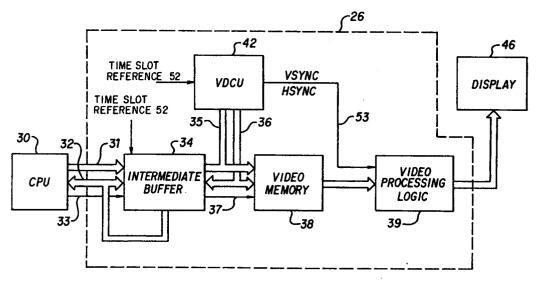


FIG. 3



EUROPEAN SEARCH REPORT

EP 90 31 3405

ategory	Citation of document with ind of relevant pass		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
١.	US-A-4 418 343 (JOSEPH L	. RYAN)	1,3, 9-12,14	G09G1/16 G09G5/36
	* abstract; figures 1-6	*	•	,
	* column 4, line 50 - co			
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`	vol. 009, no. 273 (P-401 & JP-A-60 117 327 (FUJI * abstract *)30 October 1985		
				
				TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			:	G09G
	The present search report has been	<u>-</u>		Residen
	Place of search THE HAGUE	Date of completion of the search 29 JUNE 1992		ROOST L.L.A.
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doc A : tech	cicularly relevant if combined with anot ument of the same category inological background i-written disclosure	L : document ci	ted in the application ted for other reasons the same patent famil	***************************************