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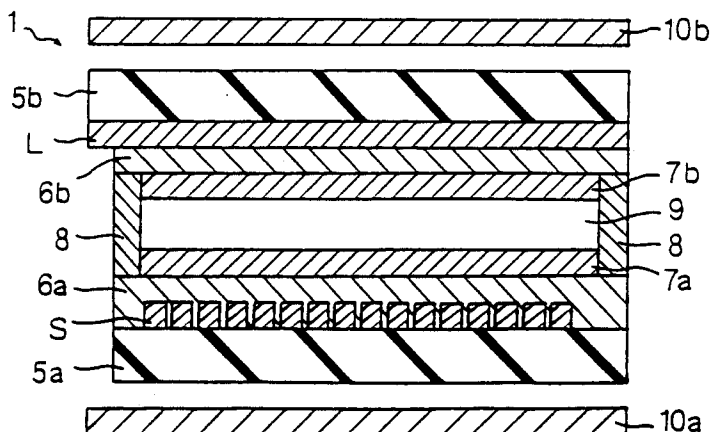
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Nara-shi, Nara-ken(JP)**(84) Designated Contracting States:
DE GB NL(74) Representative: **TER MEER - MÜLLER -
STEINMEISTER & PARTNER
Mauerkircherstrasse 45
W-8000 München 80(DE)**(71) Applicant: **SHARP KABUSHIKI KAISHA
22-22 Nagaike-cho Abeno-ku
Osaka 545(JP)**(54) **Method of display control.**

(57) The invention relates a display control method for a ferroelectric liquid crystal panel (1), according to which a display without noticeable flickers can be obtained with less memory capacity. The driving method, in which a reloading bright voltage or reloading dark voltage is applied to signal electrodes (S) depending upon whether pixels on scanning electrodes (L) to which a selective voltage is applied should be reloaded into a dark state of a display or a bright state of a display, or not utterly reloaded, is characterized in that data which are already displayed

can be retained by applying the reloading dark voltage to the signal electrodes when data to be displayed are dark but applying the reloading bright voltage to the signal electrodes when the data to be displayed are bright if there is no difference between the data to be displayed by the pixels on the scanning electrodes to which the selective voltage is applied and the data already displayed, but by applying a non-reloading voltage to the signal electrodes if there is any difference between the data to be displayed and the data already displayed.

FIG. 2**EP 0 492 542 A2**

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of display control for a ferroelectric liquid crystal (referred to as "FLC" hereinafter) panel. Related Art

Fig. 26 is a sectional view showing a schematic structure of a FLC panel 26. Two glass substrates 5a and 5b are disposed opposed to each other, one glass substrate 5a is provided on its surface a plurality of signal electrodes S of an indium tin oxide (referred to as "ITO" hereinafter) arranged in parallel to one another, and it is covered with a transparent insulating film 6a of SiO₂. The other glass substrate 5b opposed to the signal electrodes S is provided on its surface with a plurality of scanning electrodes L in parallel with one another orthogonal to the signal electrodes S, and it is covered with a transparent insulating film 6b of SiO₂. The insulating films 6a and 6b are formed on their respective surfaces with arrangement films 7a and 7b which may be, for example, subjected to a rubbing process and made of polyvinyl alcohol. The two glass substrates 5a and 5b are stuck together by a sealing material 8, with an inlet alone unstuck. FLC 9 is introduced from the inlet to a space defined by the arrangement films 7a and 7b by vacuum injection, and thereafter, the inlet is closed by the sealing material 8. The two glass substrates 5a and 5b, which are stuck together into a lamination in this way, are sandwiched by deflection plates 10a and 10b which are arranged for their deflection axes to be orthogonal to each other.

Fig. 27 is a plan view showing a structure of a FLC display (referred to as an abbreviation "FLCD" hereinafter) where a driving circuit 28 for a scanning side is connected to the above-mentioned scanning electrodes L of a simple matrix configuration FLC panel 26 while another driving circuit 29 for a signal side is connected to the above-mentioned signal electrodes S. The driving circuit 28 is a circuit for applying voltage to the scanning electrodes L, while the driving circuit 29 is a circuit for applying voltage to the signal electrodes S. To make a discussion simple, herein disclosed is a case in which there are nine scanning electrodes L and eight signal electrodes S, in other words, a case in which a FLCD 4 consisting of 9 x 8 pixels is employed, and each of the scanning electrodes L is identified by a subscript "i" (i = 0 to 8) added to the character "L" while each of the signal electrodes S is identified by a subscript "j" (j = 0 to 7) added to the character "S". In the explanation hereinafter, a pixel at a point where an arbitrary scanning electrode Li and an arbitrary signal electrode Sj intersect is denoted by a symbol "Aij".

Fig. 25 is a block diagram schematically showing an architecture of a display system in which the above mentioned FLCD 27 is employed. In the display system, information required for an image display is drawn from digital signals which a personal computer 2 applies to a CRT display 3, a control circuit 25 transduces the digital signals into signals used for an image display on the FLCD 27, and FLCD 27 displays an image in accordance with the transduced signals.

Fig. 4 is a waveform diagram showing various signals applied by the above-mentioned personal computer 2 to the CRT display 3, in which Fig. 4(1) shows a horizontal synchronizing signal HD which applies a period equivalent to a single horizontal scanning section of an image information output to the CRT display 3, Fig. 4(2) shows a vertical synchronizing signal VD which applies a period equivalent to a single screen of the information, and Fig. 4(3) shows display data "Data" of the information for each single horizontal scanning section, with subscript numerals in correspondence with the scanning electrodes Li of the FLCD 27. Fig. 4(4) is a waveform diagram showing an enlarged single horizontal scanning section of the horizontal synchronizing signal HD, Fig. 4(5) is a waveform diagram showing an enlarged single horizontal scanning section of the above-mentioned display data Data, with subscript numerals in correspondence with the signal electrodes Sj of the FLCD 27, and Fig. 4(6) is a waveform diagram showing a data transferring clock CLK of the display data Data for each pixel.

A method of driving the FLCD 27 is disclosed in Japanese Unexamined Patent Publication No. 59389/1989. Fig. 10 is a waveform diagram showing an example of waveforms of voltages applied to the scanning electrodes L and signal electrodes S employed in the driving method. Among them, a waveform shown in Fig. 10(1) is a waveform of a selective voltage A which is applied to the scanning electrodes L to reload a state of memory of pixels on the very scanning electrodes L, or a state of a brightness on the display, while a waveform shown in Fig. 10(2) is a waveform of a non-selective voltage B which is applied to the other scanning electrodes L so as not to reload a state of display of pixels on the very scanning electrodes L.

A waveform shown in Fig. 10(3) is a waveform of a reloading dark voltage C for reloading the display state of the pixels on the scanning electrodes L to which the selective voltage A is applied to a brightness state "dark", a waveform shown in Fig. 10(4) is a waveform of a reloading bright voltage D for reloading the display state of the pixels on the scanning electrodes L to which the selective voltage A is applied to a brightness state "bright", and a waveform shown in Fig. 10(5) is a

waveform of a non-reloading voltage G which is applied to the signal electrodes S for preventing the display state of the pixels on the scanning electrodes L to which the selective voltage A is applied from being reloaded.

Figs. 10(6) to (11) show waveforms of effective voltage related to the pixel Aij, in which a waveform A-C shown in Fig. 10(6) is a voltage waveform related to the pixel Aij when the selective voltage A is applied to the scanning electrode Li while the reloading dark voltage C is applied to the signal electrode Sj, a waveform A-D shown in Fig. 10(7) is a voltage waveform related to the pixel Aij when the selective voltage A is applied to the scanning electrode Li while the reloading bright voltage D is applied to the signal electrode Sj, a waveform A-G shown in Fig. 10(8) is a voltage waveform related to the pixel Aij when the selective voltage A is applied to the scanning electrode Li while the non-reloading voltage G is applied to the signal electrode Sj, a waveform B-C shown in Fig. 10(9) is a voltage waveform related to the pixel Aij when the non-selective voltage B is applied to the scanning electrode Li while the reloading dark voltage C is applied to the signal electrode Sj, a waveform B-D shown in Fig. 10(10) is a voltage waveform related to the pixel Aij when the non-selective voltage B is applied to the scanning electrode Li while the reloading bright voltage D is applied to the signal electrode Sj, a waveform B-G shown in Fig. 10(11) is a voltage waveform related to the pixel Aij when the non-selective voltage B is applied to the scanning electrode Li while the non-reloading voltage G is applied to the signal electrode Sj.

When a display state of the pixel Aij of the FLC 27 shown in Fig. 27 should be reloaded in accordance with the above-mentioned driving method, the selective voltage A shown in Fig. 10(1) is applied to the scanning electrode Li, the non-selective voltage B shown in Fig. 10(2) is applied to all the other scanning electrodes Lk ($k \neq i$, $k = 0$ to 8), the reloading dark voltage C shown in Fig. 10(3) is applied to the signal electrode Sj when the pixel Aij should be reloaded into a "dark" display state, the reloading bright voltage D shown in Fig. 10(4) is applied to the signal electrode Sj when the pixel Aij should be reloaded into a "bright" display state, and the non-reloading voltage G shown in Fig. 10(5) is applied to the signal electrode Sj when the pixel Aij may be unchanged in the "bright" display state or "dark" display state as in its previous frame.

For example, in the case where the personal computer 2 applies to the control circuit 25 a signal for displaying a letter "E" as shown in Fig. 5 under the condition that a letter "A" is displayed on a screen by pixels Aij in the "dark" display state shown by oblique lines in the FLC 27 in Fig. 27,

when the pixels Aij reloaded from the "bright" display state to the "dark" display state are denoted by a character "C" in correspondence with the reloading dark voltage C, the pixels Aij reloaded from the "dark" display state to the "bright" display state are denoted by a character "D" in correspondence with the reloading bright voltage D, the pixels Aij remaining in the "dark" display state are denoted by a character "H", and the pixels Aij remaining in the "bright" display state are expressed without character, a conversion of the whole screen is shown in Fig. 28.

In the above-mentioned driving method, the selective voltage A is applied to the scanning electrodes L0 to L8 in this order, applied to the signal electrodes S0 to S7 are the reloading dark voltage C in correspondence with the character "C" in positions corresponding to the pixels Ai0 to Ai7 on the scanning electrodes Li shown in Fig. 28 to which the selective voltage A is applied, the reloading bright voltage D in correspondence with the character "D", and the non-reloading voltage G in correspondence with the character "H" and a void without character.

Specifically, the reloading dark voltage C is applied to the signal electrodes S1 and S5 while the non-reloading voltage C is applied to the other signal electrodes when the selective voltage A is applied to the scanning electrode L2, and the reloading bright voltage D is applied to the signal electrode S5 while the non-reloading voltage C is applied to the other signal electrodes when the selective voltage A is applied to the scanning electrode L3.

In this way, merely the voltage shown in Fig. 10(8) and the voltages shown in Figs. 10(9) to (11) are applied to the pixels denoted by the character "H" and the void without character in Fig. 28, and since there is so much difference between optical effects that the former and latter voltages exert on the pixels, a display without flicker can be attained even if a period of time from an application of the selective voltage A to the scanning electrode Li to another application of the selective voltage A to the same scanning electrode, namely, a single frame frequency is less than 60 Hz or over (30 Hz or over according to another report).

It is very difficult to keep a perfect bistable state of memory in a FLC panel, and even within a display region of an ordinary panel, both areas stable in a dark state of memory and areas stable in a bright state of memory are included. In the case where the selective voltage is applied to the scanning electrodes of the FLC panel without controlling such an arrangement of the areas, a continuous application of the non-reloading voltage to the signal electrodes causes the pixels to be in a stable state of memory, and consequently arises

the problem that what is displayed cannot be recognized.

On the other hand, in the Japanese Unexamined Patent Publication No. 298286/1988 titled "Method of Driving a Display Device", all the scanning electrodes are uniformly divided in four adjacent scanning electrodes to make scanning electrode groups, a 4 : 1 skip scanning is performed where the selective voltage is successively applied to first scanning electrodes of the four scanning electrodes of the scanning electrode groups in a first field, the selective voltage is successively applied to second scanning electrodes of the four scanning electrodes of the scanning electrode groups in a second field, the selective voltage is successively applied to third scanning electrodes of the four scanning electrodes of the scanning electrode groups in a third field, and the selective voltage is successively applied to the last scanning electrodes of the four scanning electrodes of the scanning electrode groups in a fourth field, and additionally, keeping the field frequency 30 Hz or over, a display without conspicuous flicker can be obtained.

In such a driving method where a N : 1 skip scanning is employed to reload a display, there is the problem that N fields, or a single frame, are required only to reload a slight display.

Then, it can be easily expected that each time the selective voltage is applied to a certain number of the scanning electrodes by the N : 1 skip scanning, the selective voltage is applied to a certain number of the scanning electrodes including the pixels which have been observed to make a change of display in accordance with the driving method described in the Japanese Unexamined Patent Publication No. 59389/1989 to reload the pixels on the scanning electrodes, so that a FLCD which has no conspicuous flicker and can quickly respond to a change in the contents of a display can be obtained.

Now, an existing refresh driving method will be described with an example of a multi-interlace driving method described in Japanese Unexamined Patent Publication No. 128044/1989 filed by Canon Co., Ltd, which is an improved version of an interlace refresh driving.

Fig. 29 is a combination of waveforms of voltages applied to scanning electrodes L and signal electrodes S employed as an embodiment disclosed in the gazette of the Japanese Unexamined Patent Publication No. 128044/1989. A combination of voltage waveforms shown in Fig. 29(A) is a combination of waveforms of voltages for reloading pixels on the scanning electrodes into a first stable state, wherein 1) is a selective voltage V_{CA} which allows a state of the pixels on the scanning electrodes to which this voltage is applied to be re-

loaded into the first stable state, 2) is a non-selective voltage V_{CB} which never allow the state of the pixels on the scanning electrodes to which this voltage is applied to be reloaded into the first stable state, 3) is a reloading dark voltage V_{SC} for reloading the pixels consisting of the signal electrodes to which this voltage is applied and the scanning electrodes to which the voltage V_{CA} is applied into the first stable state, 4) is a non-reloading dark voltage V_{SG} for preventing the pixels consisting of the signal electrodes to which this voltage is applied and the scanning electrodes to which the voltage V_{CA} is applied from being reloaded into the first stable state, 5) is a voltage A-C which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CA} is applied and the signal electrodes to which the voltage V_{SC} is applied, 6) is a voltage A-G which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CA} is applied and the signal electrodes to which the voltage V_{SG} is applied, 7) is a voltage B-C which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CB} is applied and the signal electrodes to which the voltage V_{SC} is applied, and 8) is a voltage B-G which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CB} is applied and the signal electrodes to which the voltage V_{SG} is applied.

A combination of voltage waveforms shown in Fig. 29(B) is a combination of waveforms of voltages for reloading pixels on the scanning electrodes into a second stable state, wherein 1) is a selective voltage V_{CE} which allows a state of the pixels on the scanning electrodes to which this voltage is applied to be reloaded into the second stable state, 2) is a non-selective voltage V_{CF} which never allow the state of the pixels on the scanning electrodes to which this voltage is applied to be reloaded into the second stable state, 3) is a reloading dark voltage V_{SD} for reloading the pixels consisting of the signal electrodes to which this voltage is applied and the scanning electrodes to which the voltage V_{CE} is applied into the second stable state, 4) is a non-reloading dark voltage V_{SH} for preventing the pixels consisting of the signal electrodes to which this voltage is applied and the scanning electrodes to which the voltage V_{CE} is applied from being reloaded into the second stable state, 5) is a voltage A-D which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CE} is applied and the signal electrodes to which the voltage V_{SD} is applied, 6) is a voltage E-H which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CE} is applied and the signal electrodes to which the voltage V_{CH} is applied, 7) is a voltage F-D which is applied to the pixels consisting of the

scanning electrodes to which the voltage V_{CF} is applied and the signal electrodes to which the voltage V_{SD} is applied, and 8) is a voltage F-H which is applied to the pixels consisting of the scanning electrodes to which the voltage V_{CF} is applied and the signal electrodes to which the voltage V_{SH} is applied.

In this embodiment, all the scanning electrodes are divided into four groups by picking up every four of them to make a group (a group is composed of L0, L4, L8 and L12), and in a first field the pixels on the scanning electrodes belonging to a first group are refreshed by the combination of voltage waveforms shown in Fig. 29(A), while the pixels on the scanning electrodes belonging to a third group are refreshed by the combination of voltage waveforms shown in Fig. 29(B). In a second field, the pixels on the scanning electrodes belonging to a second group are refreshed by the combination of voltage waveforms shown in Fig. 29(A), while the pixels on the scanning electrodes belonging to a fourth group are refreshed by the combination of voltage waveforms shown in Fig. 29(B) in a fourth field.

In a third field, the pixels on the scanning electrodes belonging to a third group are refreshed by the combination of voltage waveforms shown in Fig. 29(A), while the pixels on the scanning electrodes belonging to a first group are refreshed by the combination of voltage waveforms shown in Fig. 29(B). In a fourth field, the pixels on the scanning electrodes belonging to a fourth group are refreshed by the combination of voltage waveforms shown in Fig. 29(A), while the pixels on the scanning electrodes belonging to a second group are refreshed by the combination of voltage waveforms shown in Fig. 29(B).

A state of a display of pixels A11 to A22 consisting of the scanning electrodes L1 to L4 and the signal electrodes S1 and S2 is shown in Fig. 30, voltages applied to the scanning electrodes L1 to L4 and the signal electrodes S1 and S2 when this embodiment is employed are shown in Fig. 31, and voltages applied to the pixels A11 to A22 are shown in Fig. 32. In Fig. 31, 1) is a voltage applied to the scanning electrode L1, 2) is a voltage applied to the scanning electrode L2, 3) is a voltage applied to the scanning electrode L3, 4) is a voltage applied to the scanning electrode L4, 5) is a voltage applied to the signal electrode S1, and 6) is a voltage applied to the signal electrode S2. In Fig. 32, 1) is a voltage applied to the pixel A11, 2) is a voltage applied to the pixel A12, 3) is a voltage applied to the pixel A21, and 4) is a voltage applied to the pixel A22.

In this embodiment, if you see all the pixels A11 to A22 at a time, a brightness of the FLCD 4 has a peak in a cycle of a single field, and if the

field frequency is set to a frequency of 60 Hz or over (30 Hz or over according to another report) in which no flicker is within sight of a person, pixels of the FLCD can be refreshed without flicker.

It is not preferable that pixels in an area where the contents of a display is changed are reloaded by the N : 1 skip scanning (including the multi-interlace driving method described in the gazette of the Japanese Unexamined Patent Publication No. 128044/1989) before the pixels are reloaded in accordance with the driving method described in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989, because the contents of the display are changed at intervals of several scanning electrodes. To avoid such a disadvantage, a screen of states of pixels to be displayed next and a screen of states of pixels already displayed on the FLC panel are recorded, and both of those data may be used if the pixels should be reloaded in accordance with the driving method described in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989, while the latter data may be used if the pixels should be reloaded by the N : 1 skip scanning. However, a structure of a control circuit to perform such operations must be too complicated.

In the interlace refresh driving, assuming that it takes t_1 seconds to reload pixels on a single scanning electrode and that P scanning electrodes are picked up on the average to be driven for a partial reloading after a single scanning electrode is picked up to be driven for a refreshment, when all the scanning electrodes are skip-driven at intervals of every Q scanning electrodes, the number N of the scanning electrodes which can be used for a display must satisfy the following formula:

$$t_1 \times (1 + P) \times N/Q \leq 1/60 \text{ [ms]} \quad (1)$$

This formula can be transformed into

$$Q \geq 60 \times N \times (1 + P) \times t_1 \quad (2)$$

and assuming now that 100 &Ls is required for reloading the pixels on a single scanning electrode, when a single scanning electrode is picked up on the average to be driven for a partial reloading after a single scanning electrode is picked up to be driven for a refreshment, all the scanning electrodes must be skip-driven every Q scanning electrodes to display the FLCD having 4096 scanning electrodes, where Q is expressed as follows:

$$Q \geq 60 \text{ Hz} \times 4096 \times (1 + 1) \times 100 \mu\text{s} = 49.152$$

However, even if the scanning electrodes are skip-driven every so large a number of the scanning electrodes, sometimes so many pixels cannot

be within sight of a person at a time, and naturally, the number of the scanning electrodes which can be skip-driven at a time is restricted. The number is approximately 16 to 32, and hence, naturally, the number of the scanning electrodes which can be used for a display with an FLC is restricted.

SUMMARY OF THE INVENTION

It is intended that this invention should overcome the above-mentioned disadvantages, and it is an object of the present invention to provide the optimum driving method to the above-mentioned display control method.

It is another object of the present invention to provide a refresh driving method according to which the number of scanning electrodes which can be used for a display can be increased by employing an existing refresh driving method.

The purpose of performing the N : 1 skip scanning in this invention is to retain the states of pixels on an FLC panel without conspicuous flicker. According to the driving method of this invention, in order to prevent the contents of a display from changing every several scanning electrodes, a non-reloading voltage is applied to signal electrodes so as not to change the states of a display of the pixels if there is any difference between a state of a display of the pixels on the scanning electrodes to which a selective voltage is applied and data to be displayed through the pixels,

a reloading dark voltage is applied to the signal electrodes when data displayed through the pixels are dark while a reloading bright voltage is applied to the signal electrodes when the data displayed through the pixels are bright so as to retain a state of a display of the pixels, if there is no difference between the state of a display of the pixels on the scanning electrodes on the FLC panel to which the selective voltage is applied and data to be displayed through the pixels.

The purpose of the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989 is to reload the states of the pixels on the FLC panel without conspicuous flicker. According to this driving method, in order to avoid a conspicuous flicker, if there is any difference between a state of the pixels on the scanning electrodes to which the selective voltage is applied and data to be displayed through the pixels, a reloading dark voltage is applied to the signal electrodes when the data displayed through the pixels are dark, a reloading bright voltage is applied to the signal electrodes when the data displayed through the pixels are bright, while a non-reloading voltage is applied to the signal electrodes to avoid a conspicuous flicker when there is no difference between the state of a display of the

pixels on the scanning electrodes on the FLC panel to which the selective voltage is applied and data to be displayed through the pixels, so as to keep the state of a display of the pixels in an intended state of a display.

To make such a driving method effective, a control circuit is made including means for recording states of the pixels to be displayed on the FLC panel, and means for recording if there is any difference between a state of the pixels to be displayed on the FLC panel and the state of the pixels already displayed for every several pixels (recording there is a difference if only a single pixel in a group of several pixels has the difference), and the data recorded by the former means are defined as display data while the data recorded by the latter means are defined as identifying data,

when the selective voltage is applied to the scanning electrodes to perform the N : 1 skip scanning in accordance with the above driving method, the non-reloading voltage is applied to the signal electrodes indifferent of the display data if the identifying data show some difference, and if the identifying data show no difference, the reloading dark voltage is applied to the signal electrodes when the display data are dark, while the reloading bright voltage is applied to the signal electrodes when the display data are bright,

when the selective voltage is applied to the scanning electrodes to perform the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989, if the identifying data show some difference, the reloading dark voltage is applied to the signal electrodes when the display data are dark, while the reloading bright voltage is applied to the signal electrodes when the display data are bright, and if the identifying data show no difference, the non-reloading voltage is applied to the signal electrodes indifferent of the display data,

if the selective voltage is applied to a certain number of the scanning electrodes containing the pixels of which display makes some change in accordance with the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989 each time the selective voltage is applied to a certain number of the scanning electrodes by the N : 1 skip scanning in accordance with this invention, a display in which the contents of the display do not change every several scanning electrodes can be obtained. Also, a control circuit which requires a storing capacity less than 2 screens can be made.

In the invention of the refresh driving method, a combination of voltage waveforms satisfying the following four requirements:

- I) A combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages

to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the the scanning electrodes to which the non-selective voltage is applied and the signal electrodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 1 is followed by the voltage of a polarity 2 which is substantially the same value as the voltage of the polarity 1,

II) a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the the scanning electrodes to which the non-selective voltage is applied and the signal electrodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 1 is followed by the voltage of a polarity 2 which is substantially the same value as the voltage of the polarity 1,

III) a combination of a selective voltage applied to scanning electrodes to drive them for a refreshment, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage applied to the scanning electrodes, and

IV) a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes,

with regard to these four combinations of the voltage waveforms, after a single scanning electrode is driven for a refreshment using the combination of voltage waveforms III) or IV), another scanning electrode is driven for a refreshment using the combination of voltage waveforms IV) or III), and then, P scanning electrodes are driven for a partial reloading using the combination of voltage waveforms II), so as

to overcome the disadvantages in the conventional art.

Preferably, as to the driving for a refreshment, a skip driving is performed every Q scanning electrodes.

Such a driving method can be implemented for the following reasons: When the selective voltage is applied to the scanning electrodes for the purpose of performing the N : 1 skip scanning in accordance with the driving method of this invention, the selective voltage is immediately applied to the scanning electrodes to perform the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989 even without a retention of the state of a display of the pixels about which the identifying data show some difference, and as to the pixels about which the identifying data show some difference, the reloading dark voltage is applied to the signal electrodes when the display data of the pixels are dark, while the reloading bright voltage is applied to the signal electrodes to reload the pixels when the display data are bright; and hence, there is no necessity of retaining the contents of a display of the pixels which make some change in the N : 1 skip scanning.

The driving method disclosed in the Japanese Unexamined Patent Publication No. 59389/1989 can be implemented for the following reasons: Even if the pixels which make some change in a state of a display are reloaded, a variation in brightness due to the reloading cannot be distinguished from a variation in brightness due to a variation in a state of a display, and the variation in brightness due to the reloading cannot be found whether a frame frequency is 60 Hz or 1 Hz.

The driving method disclosed in the Japanese Unexamined Patent Publication No. 59389/1989 also makes it possible that the required storing capacity is reduced less than two frames. Reloading one of the pixels which have some difference between a state to be displayed on the FLC panel and a state already displayed, it is certain that the variation in brightness in the very part on the FLC panel can be found without reloading a plurality of adjacent pixels having no difference between the state to be displayed on the FLC panel and the state already displayed, and hence there is no need of recording the identifying data pixel by pixel, but it is possible to record a plurality of pixels at a time.

Fig. 34 shows a state of FLC molecules 101 in a smectic C-phase. The FLC molecules 101 move on an inherent circular cone. Fig. 11(A) is a view showing this state seen from above, where angles (tilt angles) of the maximum axis 107 and 106 along which the FLC molecules 101 can move are $-\theta$ and θ related to a center axis 103, while angles

(memory angles) of the first stable state 105 and the second stable state 104 are $-\omega$ and ω related to the center axis 103. The FLC molecules must be moved to the angle 0 in many cases to convert them from the first stable state to the second stable state, while the FLC molecules must be moved to the angle $-\theta$ in many cases to convert them from the second stable state to the first stable state.

Assume that the FLC molecules 101 stay in the first stable state 105. When the voltage of the polarity 2 is applied to the FLC molecules 101 to move them from the angle $-\omega$ to the angle ω and thereafter the voltage is reduced to zero, the FLC molecules 101 return naturally from the angle ω to $-\omega$. Also, when the voltage of the polarity 1 is applied to the FLC molecules 101 to move them from the angle $-\omega$ to the angle $-\theta$ and thereafter the voltage is reduced to zero, the FLC molecules 101 return naturally from the angle $-\theta$ to $-\omega$. This means that once the FLC molecules 101 stay in the first stable state 105, a restoring force is exerted for the FLC molecules 101 to return to the angle $-\omega$.

Similarly, when the FLC molecules 101 stay in the second stable state 104, a restoring force is exerted for them to return to the angle ω .

Then, repeating an operation that the voltage of the polarity 2 is applied to the FLC molecules 101 in the first stable state 105 and thereafter the voltage of the polarity 1 identical in value to the voltage of the polarity 2 is applied thereto, the center of swinging of the FLC molecules 101 is first close to the angle 0, and soon the center comes almost to the angle $-\omega$ because a restoring force is exerted so that the FLC molecules 101 may return to the angle $-\omega$. Similarly, repeating an operation that the voltage of the polarity 1 is applied to the FLC molecules 101 in the second stable state 104 and thereafter the voltage of the polarity 2 identical in value to the voltage of the polarity 1 is applied thereto, the center of swinging of the FLC molecules 101 is first close to the angle 0, and soon the center comes almost to the angle ω .

With the driving method according to the present invention, assuming that the FLC molecules composing pixels on scanning electrodes which are not picked up in the driving for a partial reloading stay in the first stable state, an operation that the voltage of the polarity 1, the voltage of the polarity 2, and further, the voltage of the polarity 1 are applied in this order to the FLC molecules is repeated P times.

When the voltage of polarity 2 is applied after the application of the voltage of the polarity 1 at the P-th time, it can be expected that the center of the swinging of the FLC molecules comes close to the angle $-\omega$. The center close to the angle $-\omega$ means

that the center comes close to the angle 0 immediately after the application of the voltage of the polarity 2 to the FLC molecules, and if the voltage of the polarity 2 is applied to the FLC molecules lying in this angle, the FLC molecules can be moved closer to the angle θ rather than the voltage of the polarity 2 is applied to the FLC molecules lying in the angle ω .

After that, repeating P times an operation that the voltage of the polarity 2 is applied and thereafter the voltage of the polarity 1 is applied, the center of the swinging of the FLC molecules come close to the angle $-\omega$, and the center lies closer to the angle $-\theta$ immediately after the application of the voltage of the polarity 1 to the FLC molecules. If the voltage of the polarity 1 is applied to the FLC molecules lying in this angle, the FLC molecules can be moved closer to the angle θ rather than the voltage of the polarity 1 is applied to the FLC molecules lying in the angle $-\omega$.

Then, positioning a deflection axis of an deflection plate at an angle of $-\omega$ or an angle slightly deviated from the angle $-\omega$, pixels which stays a dark state of a display and are composed of the FLC molecules in the first stable state has an increasingly larger amount of light transmission each time the operations are switched, and an effect that an amount of the light transmission caused when the pixels are reloaded in the refresh driving becomes inconspicuous is observed.

A similar effect is observed as to the FLC molecules in the second stable state and composing the pixels which lie in a bright state of a display.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a schematic architecture of a display system to which a display control method of this invention is applied;

Fig. 2 is a sectional view showing a structure of an FLC panel employed in an FLCD of the display system;

Fig. 3 is a diagram showing a state where characters "ABCD" are displayed on the FLCD employed in the display system;

Fig. 4 is a waveform diagram showing an output signal from a personal computer in the display system;

Figs. 5 and 6 are diagrams showing a matrix of data which are carried by the output signal in Fig. 4;

Fig. 7 is a diagram showing a matrix of data of a display memory circuit included in the display system;

Fig. 8 is a diagram showing a matrix of variation in the data in the display memory circuit;

Fig. 9 is a diagram showing a matrix of data in an identifying memory circuit included in the display system;

Fig. 10 is a waveform diagram showing applied voltage used for driving the FLC panel in Embodiment 1 in this invention and a conventional embodiment;

Fig. 11 is a diagram showing a matrix of the data of the identifying memory circuit included in the display system;

Fig. 12 is a diagram showing an exemplary configuration of an electrode on the FLC panel;

Fig. 13 is a diagram showing a concept of a state of FLC molecules of which pixels consist when the electrode in Fig. 12 is employed;

Fig. 14(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state, while Fig. 14(B) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a second stable state;

Fig. 15 is a block diagram showing a schematic structure of a control circuit employed in Embodiment 2 in this invention;

Fig. 16 is a circuit diagram showing an exemplary structure of an input control circuit in the control circuit;

Fig. 17 is a circuit diagram showing an exemplary structure of an output control circuit in the control circuit;

Fig. 18 is a circuit diagram showing an exemplary structure of an address circuit in the control circuit;

Fig. 19 is a circuit diagram showing an exemplary structure of a display memory circuit in the control circuit;

Fig. 20 is a circuit diagram showing an exemplary structure of a group memory circuit in the control circuit;

Fig. 21 is a circuit diagram showing an exemplary structure of an identifying memory circuit in the control circuit;

Figs. 22 and 23 are diagrams for explaining the operation of the output control circuit in the control circuit;

Fig. 24 is a waveform diagram showing voltages related to several scanning and signal electrodes and pixels on the FLC panel in Embodiment 2;

Fig. 25 is a block diagram showing a schematic architecture of a conventional display system;

Fig. 26 is a sectional view showing a structure of an FLC panel employed in an FLCD of the conventional display system;

Fig. 27 is a diagram showing a state in which a character "A" is displayed on the FLCD em-

ployed in the conventional display system;

Fig. 28 is a diagram showing a concept of a state of a display of pixels on the conventional FLC panel, with a variation in the state indicated by symbols;

Fig. 29(A) is a waveform diagram showing applied voltages employed in the conventional embodiment for reloading pixels on scanning electrodes into a first stable state, while Fig. 29(B) is a waveform diagram showing applied voltages employed in the conventional embodiment for reloading the pixels on the scanning electrodes into a second stable state;

Fig. 30 is a diagram showing a state of a display of pixels exemplified in the conventional embodiment;

Fig. 31 is a waveform diagram showing voltages applied to the scanning electrodes and signal electrodes in the conventional embodiment;

Fig. 32 is a waveform diagram showing voltages applied to the pixels in the conventional embodiment;

Fig. 33 is a diagram showing FLC molecules seen from above;

Fig. 34 is a diagram showing a state of the FLC molecules in smectic C phase;

Figs. 35 and 36 are diagram showing a structure of a control circuit for implementing this invention;

Fig. 37 is a diagram showing data of an identifying memory circuit included in the control circuit;

Fig. 38 is a waveform diagram showing voltages applied to the scanning electrodes and signal electrodes in an embodiment according to the present invention;

Fig. 39 is a waveform diagram showing voltages applied to pixels in the embodiment according to the present invention;

Fig. 40 is a waveform diagram for explaining the operation of the FLC molecules of which pixels in the first stable state consist in the embodiment according to the present invention;

Fig. 41(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state;

while Fig. 41(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state;

Fig. 42 is a waveform diagram for explaining the operation of the FLC molecules of which pixels in the first stable state consist in the embodiment according to the present invention;

Fig. 43(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a

first stable state, while Fig. 43(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 44(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state, while Fig. 44(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 45(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state, while Fig. 45(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 46(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state, while Fig. 46(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 47(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state;

while Fig. 47(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 48(A) is a waveform diagram showing applied voltages employed in this invention for reloading pixels on scanning electrodes into a first stable state; while Fig. 48(B) is a waveform diagram showing applied voltages employed in this invention for reloading the pixels on the scanning electrodes into a second stable state; Fig. 49 is a waveform diagram showing another operation in the control circuit according to the present invention; Fig. 50 is a circuit diagram showing an exemplary structure of a group memory circuit in the control circuit; and Fig. 51 is a circuit diagram showing an exemplary embodiment of an identifying memory circuit in the control circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[Embodiment 1]

Fig. 2 is a sectional view showing a schematic structure of an FLC panel 1 employed in this

embodiment, and the description of the FLC panel 1 is omitted because it is almost the same as the FLC panel 26 shown in Fig. 26 except that the FLC panel 1 is provided with sixteen scanning electrodes L and sixteen signal electrodes S. Polyimide subjected to a rubbing process is employed as an arrangement film in the FLC panel 1 while ferroelectric liquid crystal employed in this embodiment is ZL1-4237/000 manufactured by Merck Co., Ltd.

Fig. 3 is a plan view showing a structure of an FLC panel 1 in which a scanning side driving circuit 11 is connected to the scanning electrodes L of the FLC panel 1 having the above-mentioned 16 x 16 simple matrix configuration while a signal side driving circuit 12 is connected to the signal electrodes S. Each of the scanning electrodes L is identified by a subscript "i" (i = 0 to F) added to the character "L" while each of the signal electrodes S is identified by a subscript "j" (j = 0 to F).

Fig. 1 is a block diagram schematically showing an architecture of the display system in which the above-mentioned FLC panel 1 is employed. The architecture of the display system is similar to a conventional display system, for example, information required for an image display is drawn from digital signals identical to the conventional art in Fig. 4, which a personal computer 2 applies to a CRT display 3. A control circuit 13 converts the digital signals into signals used for an image display on the FLC panel 1, and the FLC panel 1 displays an image in accordance with the converted signals.

Figs. 5 and 6 are data diagrams showing a matrix of display data "Data" of the digital signals shown in Figs. 4(3) and 4(5).

The whole 16 x 16 pixels on the FLC panel 1 can be used for a data display although each of the digital signals is equivalent only to 9 x 8 pixels. This is because the 16 x 16 pixels can be virtually divided into four parts which are comprised of a display section "0" consisting of the scanning electrodes L0 to L7 and signal electrodes S0 to S7, a display section "1" consisting of the scanning electrodes L0 to L7 and signal electrodes S8 to SF, a display section "2" consisting of the scanning electrodes L8 to LF and signal electrodes S0 to S7, and a display section "3" consisting of the scanning electrodes L8 to LF and signal electrodes S8 to SF, and as shown in Figs. 5 and 6, commands are issued which display sections "0" to "3" data in the 0-th horizontal scanning section and data in the following first to eighth horizontal scanning sections correspond to.

Referring to Figs. 5 and 6, if the third data in the 0-th horizontal scanning section are "bright" (data without oblique lines) and the seventh data are "bright" (Fig. 5 is relevant to this), data in the following first to eighth horizontal scanning sections

corresponds to the display section "0". If the third data in the 0-th horizontal scanning section are "bright" and the seventh data are "dark" (data with oblique lines), the data in the following first to eighth horizontal scanning sections corresponds to the display section "1". If the third data in the 0-th horizontal scanning section are "dark" and the seventh data are "bright" (Fig. 6 is relevant to this), the data in the following first to eighth horizontal scanning sections corresponds to the display section "2". If the third data in the 0-th horizontal scanning section are "dark" and the seventh data are "dark", the data in the following first to eighth horizontal scanning sections corresponds to the display section "3".

Fig. 7 is a data diagram showing the contents of a display memory for recording display data DA which are made from the above-mentioned 9 x 8 digital signal in accordance with the above-mentioned rule and are to be displayed next on the FLC panel 1, in a 16 x 16 matrix corresponding to each pixel on the FLC panel 1.

Although it is desirable that data "ABCD" already displayed on the FLC panel 1 and shown in Fig. 3 are stored in the display memory in the 16 x 16 matrix, input of display data "E" shown in Fig. 5 to the control circuit 13 causes data "EBCD" shown in Fig. 7 to be stored instead. A variation in the data in the display memory at this time in the 16 x 16 matrix corresponding to every pixel on the FLC panel 1 (data indicated by oblique lines are the data which are varied) is shown in Fig. 8.

In this embodiment, the variation in the data in the display memory is stored in an identifying memory four pixels on the FLC panel 1 together at a time (if one of those pixels is varied). Specifically, a variation in the data in the display memory in Fig. 8 is stored as identifying data DF in the identifying memory four pixels together at a time corresponding with pixels on the FLC panel 1, Ai0 to Ai3, Ai4 to Ai7, Ai8 to AiB, AiC to AiF, as shown in Fig. 9 (data identified by oblique lines are the data which are varied). A skip scanning is performed at a rate of 4 : 1 in order of the scanning electrodes, L0, L4, L8, LC, L1, L5, L9, LD, L2, L6, LA, LE, L3, L7, LB and LF, and after the selective voltage is applied to one of the scanning electrodes in accordance with the driving method of the N : 1 skip scanning of this invention, the selective voltage is applied to two of the scanning electrodes in accordance with the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989.

Then, "ABCD" in Fig. 3 is displayed on the FLC panel 1, "EBCD" in Fig. 7 is stored in the display memory in the control circuit 13, the data in Fig. 9 is stored in the identifying memory, and in this conditions an application of the selective voltage to the scanning electrode LE in accordance with the

driving method of the N : 1 skip scanning of this invention is completed. The operation of this invention will be specifically explained, and the explanation begins with an application of the selective voltage to the scanning electrode L0 in accordance with the driving method in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989 in order of time, following the order of steps 1) to 4).

1) The driving method described in the Japanese Unexamined Patent Publication No. 59389/1989, in which it is found that all the display data DA of the pixels A00 to A0F are "bright" according to the record of the display memory in Fig. 7 while the identifying data DF is "not varied" according to the record of the identifying memory in Fig. 9, the selective voltage is applied from the scanning side driving circuit 11 to the scanning electrode L0, the non-selective voltage is applied to the scanning electrodes L1 to LF, and the non-reloading voltage is applied from the signal side driving circuit 12 to the signal electrode S0 to SF. At this time, four identifying data in the identifying memory corresponding to the scanning electrode L0 are reloaded to "not varied".

2) The driving method described in the Japanese Unexamined Patent Publication No. 59389/1989, in which it is found that the pixels A10, A16 to A18, and A1D to A1F are "bright" and A11 to A15, and A19 to A1C are "dark" according to the record of the display memory in Fig. 7 while the pixels A10 to A17 are "varied" and the pixels A18 to A1F are "not varied" according to the record of the identifying memory in Fig. 9, the selective voltage is applied from the scanning side driving circuit 11 to the scanning electrode L1, the non-selective voltage is applied to the scanning electrodes L0, and L2 to LF, the non-reloading voltage is applied from the signal side driving circuit 12 to the signal electrode S8 to SF, the reloading dark voltage is applied to the signal electrodes S1 to S5, and the reloading bright voltage is applied to the signal electrodes S0, S6 and S7. At this time, four identifying data corresponding to the scanning electrode L1 are reloaded to "not varied".

3) The driving method for the skip scanning, in which it is found that the pixels A30, A32 to A38, A3A to A3C, A3E and A3F are "bright" and the pixels A31, A39 and A3D are "dark" according to the record of the display memory in Fig. 7 while the pixels A34 to A37 are "varied" and the pixels A30 to A33, and A38 to A3F are "not varied" according to the record of the identifying memory in Fig. 9, the selective voltage is applied from the scanning side driving circuit 11 to

the scanning electrode L3, the non-selective voltage is applied to the scanning electrodes L0 to L2, and L4 to LF, the reloading dark voltage is applied to the signal electrodes S1, S9 and SD, the reloading bright voltage is applied to the signal electrodes S0, S2, S3, S8, SA to SC, SE and SF, and the non-reloading voltage is applied to the signal electrode S4 to S7. At this time, four identifying data corresponding to the scanning electrode L3 are not reloaded.

4) After that, the scanning electrodes are driven in the following order: L2 and L3 in accordance with the driving method in the Japanese Unexamined Patent Publication No. 59389/1989, L7 in accordance with the driving method for the skip scanning, L4 and L5 in accordance with the driving method in the Japanese Unexamined Patent Publication No. 59389/1989, LB in accordance with the driving method for the skip scanning, and so forth.

In the above-mentioned embodiment, the voltage waveforms in Figs. 10(1) to 10(5) are used as the selective voltage, non-selective voltage, reloading dark voltage, reloading bright voltage, and non-reloading voltage.

With the display control of the FLC panel 4 in the above-mentioned manner, a display in which the contents of a display never vary every several scanning electrodes can be obtained, and only a screen of the display memory and 1/4 screen of the identifying memory may be enough as the required memory capacity.

While the identifying memory in Fig. 9 has a storage of the data of every scanning electrode, it may have a storage of a variation in the display data of a plurality of the scanning electrodes together of each scanning electrode group as shown in Fig. 11.

Also, with the scanning electrodes L or signal electrodes S which have a configuration where a pixel electrode 24 corresponding to each pixel as shown in Fig. 12 is insulated by a film 23 of high dielectric constant from a conductive electrode 22 so as to conduct voltage from the scanning side driving circuit 11 or signal side driving circuit 12, the FLC panel 1 can be structured.

With the above-mentioned structure, effective voltage in Fig. 10(6) A-C or Fig. 10(7) A-D causes most of nine molecules of ferroelectric liquid crystal of which a single pixel is comprised to be reversed in polarity. However, in a pixel in which a part of the molecules is not reversed in polarity as shown in Fig. 13, such molecules are attracted by the polarity of the majority of molecules, and electric charge of opposite polarity is induced in the pixel electrode 24. Then, the polarity of the majority of the molecules repels the polarity of the part of the molecules of which polarity has not been

reversed, and the part of the molecules are reversed in polarity, so that the display of the pixels can be uniform.

In the above experiment, tantalum oxide (Ta_2O_5) is employed for the high dielectric constant insulating film 23 while ITO is employed for the pixel electrode 24 and conductive electrode 22.

[Embodiment 2]

Although the embodiment by which the present invention can be most easily understood has been described in the above Embodiment 1, there is another embodiment of the present invention, which provides a driving method in which the scanning electrodes on the FLC panel 1 are divided into groups each of which includes several scanning electrodes, and the control circuit 13 includes means for foreknowing a group of the scanning electrodes having its identifying memory varied,

the selective voltage is successively applied to all the scanning electrodes of a certain group to perform the driving method in the Japanese Unexamined Patent Publication No. 59389/1989, then an operation that the selective voltage is applied to a specific scanning electrode to perform the driving method for the N:1 skip scanning of this invention is repeated twice to the same scanning electrode group and the same scanning electrode,

first either of two kinds of voltages which reloads or not reload the pixel Aij on the scanning electrode Li, to which the selective voltage is applied, into a dark state is applied to the signal electrode Sj, and second either of two kinds of voltages which reloads or not reload the pixel Aij on the scanning electrode Li, to which the selective voltage is applied, into a bright state is applied to the signal electrode Sj.

In this embodiment, the FLC panel 4 is driven in accordance with the above-mentioned methods. Also in this embodiment, configurations of the FLC panel 1 and FLC panel 4 are the same as in Figs. 2 and 3, and a configuration of the display system is similar to Fig. 1.

In this embodiment, the 0-th scanning electrode group is comprised of the scanning electrodes L0 and L1, the first scanning electrode group is comprised of the scanning electrodes L2 and L3, the second scanning electrode group is comprised of the scanning electrodes L4 and L5, the third scanning electrode group is comprised of the scanning electrodes L6 and L7, the fourth scanning electrode group is comprised of the scanning electrodes L8 and L9, the fifth scanning electrode group is comprised of the scanning electrodes LA and LB, the sixth scanning electrode group is comprised of the scanning electrodes LC and LD, and the seventh scanning electrode group is comprised

of the scanning electrodes LE and LF. The driving method of a 4 : 1 skip scanning is performed in order of the scanning electrodes, L0, L4, L8, LC, L1, L5, L9, LD, L2, L6, LA, LE, L3, L7, LB and LF, and after the selective voltage is applied to two of the scanning electrodes in accordance with the driving method in the Japanese Unexamined Patent Publication No. 59389/1989, the selective voltage is applied to specified one of the scanning electrodes in accordance with the driving method of the 4 : 1 skip scanning. This operation is repeated twice as mentioned above.

Figs. 14(A) and 14(B) show combinations of waveforms of voltages to be applied to the scanning electrodes L and signal electrodes S on the FLC panel 1.

The waveform shown in Fig. 14(A)(1) shows a waveform of a selective voltage A which is applied to the scanning electrodes L so that a state of a display on the pixels on the scanning electrodes L may be reloaded into a "dark" luminance state, while Fig. 14(A)(2) shows a waveform of a selective voltage B which is applied to the other scanning electrodes L so that a state of a display on the pixels on the scanning electrodes L may not be reloaded.

Fig. 14(A)(3) shows a waveform of a reloading dark voltage C which is applied to the signal electrodes S so that a state of a display of the pixels on the scanning electrodes L to which the selective voltage A is applied may be reloaded into a "dark" luminance state, while Fig. 14(A)(4) shows a waveform of a non-reloading voltage G which is applied to the signal electrodes S so that a state of a display of the pixels on the scanning electrodes L to which the selective voltage A is applied may not be reloaded. Figs. 14(A)(5) to 15(A)(8) show waveforms of effective voltages related to the pixel Aij, of which a waveform A-C in Fig. 14(A)(5) is a waveform of voltage related to the pixel Aij when the reloading dark voltage C is applied to the signal electrode Sj, a waveform A-G in Fig. 14(A)(6) is a waveform of voltage related to the pixel Aij when the non-reloading voltage G is applied to the signal electrode Sj, a waveform B-C in Fig. 14(A)(7) is a waveform of voltage related to the pixel Aij when the reloading dark voltage C is applied to the signal electrode Sj, and a waveform B-G in Fig. 14(A)(8) is a waveform of voltage related to the pixel Aij when the non-reloading voltage G is applied to the signal electrode Sj.

A waveform shown in Fig. 14(B)(1) is a waveform of a selective voltage E which is applied to the scanning electrodes L may be reloaded into a "bright" luminance state, while a waveform shown in Fig. 14(B)(2) is a waveform of a non-selective voltage F which is applied to the other scanning electrodes L so that a state of a display

of the pixels on the scanning electrodes L may not be reloaded.

A waveform shown in Fig. 14(B)(3) is a waveform of a reloading dark voltage D which is applied to the signal electrodes S so that a state of a display of the pixels on the scanning electrodes L to which the selective voltage E is applied may be reloaded into a "bright" luminance state, while a waveform shown in Fig. 14(B)(4) is a waveform of a non-reloading voltage H which is applied to the signal electrodes S so that a state of a display of the pixels on the scanning electrodes L to which the selective voltage E is applied may not be reloaded.

Figs. 14(B)(5) to 14(B)(8) show waveforms of effective voltages related to the pixel Aij, of which a waveform E-D in Fig. 14(B)(5) is a waveform of a voltage related to the pixel Aij when the selective voltage E is applied to the scanning electrode Li while the reloading dark voltage D is applied to the signal electrode Sj, a waveform E-H in Fig. 14(B)(6) is a waveform of a voltage related to the pixel Aij when the selective voltage E is applied to the scanning electrode Li while the non-reloading voltage H is applied to the signal electrode Sj, a waveform F-D in Fig. 14(B)(7) is a waveform of a voltage related to the pixel Aij when the non-selective voltage F is applied to the scanning electrode Li while the reloading dark voltage D is applied to the signal electrode Sj, a waveform F-H in Fig. 14(B)(8) is a waveform of a voltage related to the pixel Aij when the non-selective voltage F is applied to the scanning electrode Li while the non-reloading voltage H is applied to the signal electrode Sj.

A configuration of a control circuit 13 is shown in a block diagram in Fig. 15. The control circuit 13 is comprised of an interface circuit 14 receiving a digital signal from a personal computer 2 for distributing to circuits which need it, a display memory circuit 15 recording the display data DA which is to be displayed next on the FLC panel, an identifying memory circuit 17 storing a variation in data of the display memory circuit 15 every four pixels together, a group memory circuit 16 storing a variation in data of the display memory circuit 15 every two scanning electrodes together, an input control circuit 18 for controlling a timing for writing required data in the three memory circuits 15, 16 and 17, an output control circuit 19 and address circuit 20 for controlling a timing for reading data to be output from the three memory circuits 15, 16 and 17 to the FLC 4, and a drive control circuit 21 receiving data from the display memory circuit 15, identifying memory circuit 17, output control circuit 19 and address circuit 20 for controlling the operation of a scanning side driving circuit 11 and signal side driving circuit 12 of which the FLC 4 is

comprised.

Fig. 16 is a diagram showing a structure of the above-mentioned input control circuit 18. The input control circuit 18 is comprised of ten NAND gates 40a to 40j, two AND gates 41a and 41b, ten D-type flip flops 42a to 42j, two shift registers 43a and 43b, a single register 44a with load function, three counters 45a to 45c, two read only memories (ROMs), and three rotary switches 47a to 47c.

Fig. 17 is a diagram showing a structure of the above-mentioned output control circuit 19. The output control circuit 19 is comprised of eleven NAND gates 48a to 48k, two AND gates 49a and 49b, eight counters 50a to 50h, two D-type flip flops 51a and 51b, a single shift register 52a, and eight rotary switches 53a to 53h.

Fig. 18 is a diagram showing a structure of the above-mentioned address circuit 20. The address circuit 20 is comprised of a single D-type flip flop 54a, and two selectors 55a and 55b.

Fig. 19 is a diagram showing a structure of the above-mentioned display memory circuit 15. The display memory circuit 15 is comprised of a single selector 56a, a single shift register 57a, a single register 58a with load function, a single three-valued buffers 59a, two D-type flip flops 60a and 60b, a single parallel/serial converter 61a, a single random access memory (RAM) 62a, four NAND gates 63a to 63d, four AND gates 64a to 64d, four EOR gates 65a to 65d, and a single OR gate 66a.

Fig. 20 is a diagram showing a structure of the above-mentioned group memory circuit 16. The group memory circuit 16 is comprised of a single selector 67a, two three-valued buffers 68a and 68b, four D-type flip flops 69a to 69d, two registers with load function 70a and 70b, a single RAM 71a, three NAND gates 72a to 72c, two OR gates 73a and 73b, and six AND gates 74a to 74f.

Fig. 21 is a diagram showing a structure of the above-mentioned identifying memory circuit 17. The identifying memory circuit 17 is comprised of two selectors 75a and 75b, a single three-valued buffers 76a, two D-type flip flops 77a and 77b, a single register with load function 78a, a single RAM 79a, two OR gates 80a and 80b, three NAND gates 82a to 82c, six AND gates 81a to 81f, and a single decoder 83a.

The interface circuit 14 and the drive control circuit 21 has a simple configuration, and therefore, configuration diagrams of them are omitted.

Figs. 22 and 23 show a process in which a display of "ABCD" shown in Fig. 3 on the FLCD 4 is turned to a display of "EBCD" in Fig. 7.

Figs. 22(1) and 23(1) show a synchronizing signal HP of 4t0 period, while Figs. 22(2) and 23(2) show an address for distinguishing two scanning electrodes which becomes effective when a drive mode H/R = "1" and included in a scanning

electrode group from each other. Figs. 22(3) and 23(3) show a drive mode H/R which corresponds to the driving method in the Japanese Unexamined Patent Publication No. 59389/1989 when it turns to "1" ("HIGH" in the drawings) but corresponds to the driving method of the N : 1 skip scanning of this invention when it turns to "0" ("LOW" in the drawings), while Figs. 22(4) and 23(4) show a voltage mode E/W which are combined with the drive mode H/R to shift a voltage combination between those in Fig. 14(B). Figs. 22(5) and 23(5) show an address identifying the scanning electrodes in the driving method of the N : 1 skip scanning of this invention, while Figs. 22(6) and 23(6) show an address identifying the scanning electrode groups in the driving method of the Japanese Unexamined Patent Publication No. 59389-1989. Figs. 22(7) and 23(7) show an address OGA outputting to the group memory 16 for searching a state of the scanning electrode groups, while Figs. 22(8) and 23(8) show an address OAC outputting to the display memory 15 and identifying memory 17 for allowing them to output the display data DA and identifying data DF. Fig. 23 is a signal diagram follows Fig. 22, partially overlaps with it in respect of time. According to a time chart shown in Figs. 22 and 23, an outline is provided below in order of time from 1) to 9).

1) For a period t ($t = 0$ to $4t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L4, the address circuit 20 to output the address OAC = "4", and the output control circuit 19 to output the drive mode H/R = "0" and voltage mode E/W = "1" to the drive control circuit 21. At the same time, the output control circuit 19 and address circuit 20 confirm a state of the fourth to sixth scanning electrode groups of the group memory circuit 16, but the data are "not varied."

In this period, the input control circuit 18 allows the data stored in the display memory circuit 15 to change from the state "ABCD" in Fig. 3 to the state "EBCD" in Fig. 7, all the data stored in the identifying memory circuit 17 to change the state "not varied" to the state "varied" of the data indicated by oblique line in Fig. 9, and all the data stored in the group memory circuit 16 to change from the state "not varied" to the state "varied" of the 0-th to third scanning electrode groups.

After that, the data stored in the display memory circuit 15 stay in the state "EBCD" shown in Fig. 7.

2) For a period t ($t = 4t_0$ to $8t_0$), the output control circuit 19 and address circuit 20 allow

the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode LA, and the address circuit 20 to output the address OAC = "A", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "1" to the drive control circuit 21. At the same time, the output control circuit 19 and address circuit 20 confirm a state of the seventh and following scanning electrode groups of the group memory circuit 16, but since the data in the 0-th scanning electrode group are "varied," the confirmation of the state of the scanning electrode groups is completed. In this way, it can be foreseen that there is some variation in a record corresponding to the 0-th scanning electrode group of the identifying memory circuit 17.

3) For a period t ($t = 8t_0$ to $12t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode LB, and address circuit 20 to output the address OAC = "B", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "1" to the drive control circuit 21.

4) For a period t ($t = 12t_0$ to $16t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L8, the address circuit 20 to output the address OAC = "8", and the output control circuit 19 to output the drive mode H/R = "0" and voltage mode E/W = "0" to the drive control circuit 21. At the same time, the output control circuit 19 and address circuit 20 allows the group memory circuit 16 to output a state of the fourth scanning electrode group and a state of the 0-th electrode group as group identification data RGDF and DGDF to the drive control circuit 21, and the state of the 0-th scanning electrode group stored in the group memory circuit 16 is returned to "not varied."

After that, when the input control circuit 18 allows the display memory circuit 15 and identifying memory circuit 17 to store the data corresponding to the 0-th scanning electrode group, the data in the identifying memory circuit 17 are once reloaded to "not varied", and thereafter, a variation of the display memory circuit 15 is stored again.

5) For a period t ($t = 16t_0$ to $20t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA

and identifying data DF corresponding to the scanning electrode L0, the address switching circuit 20 to output the address OAC = "0", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "0" to the drive control circuit 21. At the same time, the output control circuit 19 and address circuit 20 allow the states of the first and following scanning electrode groups stored in the group memory circuit 16 to be confirmed, but since the data in the first scanning electrode group are "varied", the confirmation of the states of the scanning electrode groups is completed at this point of time.

In this way, it is foreknown that there was a variation in the data corresponding to the first scanning electrode group stored in the identifying memory circuit 17.

6) For a period t ($t = 20t_0$ to $24t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L1, the address circuit 20 to output the address OAC = "1", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "0" to the drive control circuit 21.

7) For a period t ($t = 24t_0$ to $28t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L8, the address circuit 20 to output the address OAC = "8", and the output control circuit 19 to output the drive mode H/R = "0" and voltage mode E/W = "1" to the drive control circuit 21.

8) For a period t ($t = 28t_0$ to $32t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L0, the address circuit 20 to output the address OAC = "0", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "1" to the drive control circuit 21.

9) For a period t ($t = 32t_0$ to $36t_0$), the output control circuit 19 and address circuit 20 allow the display memory circuit 15 and identifying memory circuit 17 to output the display data DA and identifying data DF corresponding to the scanning electrode L1, the address circuit 20 to output the address OAC = "1", and the output control circuit 19 to output the drive mode H/R = "1" and voltage mode E/W = "1" to the drive control circuit 21.

The drive control circuit 21 receives the drive mode H/R, voltage mode E/W, display data DA, identifying data DF, group identifying data RGDF and DGDF, etc. to operate as follows:

A) When the drive mode H/R is "1" and the voltage mode E/W is "0", the voltage combination in Fig. 14(A) is applied to the scanning side driving circuit 11 and signal side driving circuit 12, and if the display data DA are "dark", the identifying data DF are "varied", and the group identifying data DGDF are "not varied", the data "DATA" corresponding to VSC in the Fig. 14(A)-(3) is applied to the signal side driving circuit 12, but otherwise the data "DATA" corresponding to VSG in Fig. 14(A)(4) is applied thereto.

B) When the drive mode H/R is "0" and the voltage mode E/W is "1", the voltage combination in Fig. 14(A) is applied to the scanning side driving circuit 11 and signal side driving circuit 12, and if the display data DA are "dark" and the identifying data DF are "not varied", or the display data DA are "dark" and the group identifying data RGDF are "not varied", the data "DATA" corresponding to VSC in the Fig. 14(A)-(3) is applied to the signal side driving circuit 12, but otherwise the data "DATA" corresponding to VSG in Fig. 14(A)(4) is applied thereto.

C) When the drive mode H/R is "1" and the voltage mode E/W is "1", the voltage combination in Fig. 14(B) is applied to the scanning side driving circuit 11 and signal side driving circuit 12, and if the display data DA are "bright", the identifying data DF are "varied", and the group identifying data DGDF are "varied", the data "DATA" corresponding to VSD in the Fig. 14(B)-(3) is applied to the signal side driving circuit 12, but otherwise the data "DATA" corresponding to VSH in Fig. 14(B)(4) is applied thereto.

D) When the drive mode H/R is "0" and the voltage mode E/W is "0", the voltage combination in Fig. 14(B) is applied to the scanning side driving circuit 11 and signal side driving circuit 12, and if the display data DA are "bright" and the identifying data DF are "not varied", or the display data DA are "bright" and the group identifying data RGDF are "not varied", the data "DATA" corresponding to VSD in the Fig. 14(B)-(3) is applied to the signal side driving circuit 12, but otherwise the data "DATA" corresponding to VSH in Fig. 14(B)(4) is applied thereto.

The data "DATA" corresponding to the pixel Aij is retained by the signal side driving circuit 12, "i" is output from the drive control circuit 21 to the scanning side driving circuit 11 as an address AX in accord with an application of the corresponding voltage from the signal side driving circuit 12 to the signal electrode Sj, and voltage V_{C0} is applied from the scanning side driving circuit 11 to the scanning

electrode Li while voltage V_{C1} is applied to other scanning electrodes Lk ($k \neq i$, $k = 0$ to F).

When the voltage combination in Fig. 14(A) is output to the scanning side driving circuit 11 and signal side driving circuit 12, V_{CA} in Fig. 14(A)(1) is applied as voltage V_{C0} from the drive control circuit 21, V_{CB} in Fig. 14(A)(2) is as voltage V_{C1} , V_{SC} in Fig. 14(A)(3) is as voltage V_{S0} , and V_{SG} in Fig. 14(A)(4) is as voltage V_{S1} . When the voltage combination in Fig. 14(B) is output to the scanning side driving circuit 11 and signal side driving circuit 12, V_{CE} in Fig. 14(B)(1) is applied as voltage V_{C0} from the drive control circuit 21, V_{CF} in Fig. 14(B)(2) is as voltage V_{C1} , V_{SD} in Fig. 14(B)(3) is as voltage V_{S0} , and V_{SH} in Fig. 14(B)(4) is as voltage V_{S1} .

Thus, voltages related to the scanning electrodes L0, L1 and L2, signal electrodes S1, S2 and S5, and pixels A11, A21, A22 and A25 are shown in Fig. 24. Fig. 24(1) is a waveform of a voltage applied to the scanning electrode L0, Fig. 24(2) is a waveform of a voltage applied to the scanning electrode L1, Fig. 24(3) is a waveform of a voltage applied to the scanning electrode L2, Fig. 24(4) is a waveform of a voltage applied to the signal electrode S1, Fig. 24(5) is a waveform of a voltage applied to the signal electrode S2, Fig. 24(6) is a waveform of a voltage applied to the signal electrode S5, Fig. 24(7) is a waveform of an effective voltage applied to the signal electrode A11, Fig. 24(8) is a waveform of an effective voltage applied to the signal electrode A21, Fig. 24(9) is a waveform of an effective voltage applied to the signal electrode A22, and Fig. 24(10) is a waveform of an effective voltage applied to the signal electrode A25.

Although each of the scanning electrode groups is comprised of two scanning electrodes in this embodiment, as more scanning electrodes are employed, accordingly a scanning electrode group may include two to 64 scanning electrodes. Also, while one scanning electrode is driven in accordance with the N : 1 skip scanning method of this invention each time all the scanning electrodes in one scanning electrode group are driven in accordance with the method disclosed in the gazette of the Japanese Unexamined Patent Publication No. 59389/1989, more than one scanning electrodes may be driven in accordance with the N : 1 skip scanning method of the present invention. While watching a state of display on the FLC panel, the operator may decide whether one scanning electrode group should be driven by the voltage combination in Fig. 14(A) or the voltage combination in Fig. 14(B) in accordance with the driving method of the Japanese Unexamined Patent Publication No. 59389/1989 after a specified scanning electrode is driven by the voltage combination in Fig. 14(A) in accordance with the driving method of the N : 1

skip scanning of this invention.

Actually, with an FLC panel 1 having 1024 x 1024 pixels where an identifying memory is made so that 1 bit is comprised of eight pixels in one scanning electrode while one scanning electrode group is comprised of sixteen scanning electrodes, each time the sixteen scanning electrodes in a single scanning electrode group are driven, a single scanning electrode is driven in accordance with the N : 1 skip scanning method of the present invention, and when the single scanning electrode group is driven by the voltage combination in Fig. 14(A) in accordance with the driving method in the Japanese Unexamined Patent Publication No. 5938/1989 after the single scanning electrode is driven by the voltage combination in Fig. 14(B) in accordance with a driving method of the N : 1 skip scanning of this invention, a good display where no flicker is conspicuous and an image is not changed every several scanning electrodes can be obtained. A required memory capacity can be reduced from 2 Mbit to about 1.2 Mbit.

Instead of the circuits of Figs. 20 and 21, the circuits 50 and 51 can be used.

Fig. 50 is a diagram showing a structure of the group memory circuit 16. The group memory circuit 16 is comprised of a single selector 67a, two three-valued buffers 68a and 68b, four D-type flip flops 69a to 69d, two registers with load function 70a and 70b, a single RAM 71a, three NAND gates 72a to 72c, two OR gates 73a and 73b, and six AND gates 74a to 74f.

Fig. 51 is a diagram showing a structure of the identifying memory circuit 17. The identifying memory circuit 17 is comprised of two selectors 75a and 75b, a single three-valued buffer 76a, two D-type flip flops 77a and 77b, a single register with load function 78a, a single RAM 79a, two OR gates 80a and 80b, three NAND gates 82a to 82c, six AND gates 81a to 81f, and a single decoder 83a.

[Embodiment 3]

A sectional view of the FLC panel 1 employed in this embodiment is all the same as that of the conventional embodiment shown in Fig. 2, and a plan view of the FLC panel 1 is also the same as in the conventional example in Fig. 3, and hence the description of them is omitted. The FLC panel 1 in this embodiment includes an arrangement film of polyimide subjected to a rubbing process, and ferroelectric liquid crystal CS-1014 manufactured by Chisso Co., Ltd.

This embodiment employs the display system of the same structure as the conventional example in Fig. 1, but employs a control circuit 13 different in structure from the conventional embodiment. The control circuit 33 is, as shown in Figs. 35 and

36, comprised of an interface circuit 34 receiving a digital signal "Data", synchronizing signals HD and VD from the personal computer 2 to distribute them as input data "Din", synchronizing signals IVD and IHD to circuits which need them, a display memory circuit 35 storing display data "DA" to be displayed next on the FLC panel 1, an identifying memory circuit 27 grouping a variation IDF in data of the display memory circuit 25 every four pixels to store them as identifying data DF, an identifying memory circuit 26 grouping a variation IDF in data of the display memory circuit 15 every two scanning electrodes to store them as identifying data IGDF and OGDF, and input control circuit 28 for controlling addresses IACx and IASx for writing input data in the three memory circuits 25 to 27, output control circuits 29 and address circuit 30 for controlling addresses OACx, OASx and OAGx of data to be output from the three memory circuit 23 to 27 to a drive control circuit 31, and the drive control circuit 31 receiving the display data "DA", identifying data DF, drive mode H/R-, voltage mode E-/W, state data DGDF and RGDF, and address OACx to control the operation of the scanning side drive circuit 11 and signal side driving circuit 12 in the FLC panel 1.

Hereinafter, this embodiment of the present invention will treat a variation in a display of the FLC panel 1 from "ABCD" in Fig. 3 to "EBCD" in Fig. 7.

The display data "EBCD" in Fig. 7 is stored in the display memory circuit 25. At this time, a difference between the display "ABCD" in Fig. 3 and the display "EBCD" in Fig. 7 is searched every single pixel, and it is detected that there is a variation in a display in a pixel identified by oblique lines in Fig. 8. Then, the variations of pixels are grouped every four pixels as shown in Fig. 9 and they are stored as identifying data (recognized as "varied" if only a single pixel is changed) in the identifying memory circuit 27.

The scanning electrodes divided into groups each of which is comprised of two scanning electrodes, and as shown in Fig. 37, and if even a single identifying data is varied as shown in Fig. 37, it is stored as two state data ("varied" if even a single identifying data contained in the scanning electrode group is varied) in the identifying memory circuit 26.

Assume that the above mentioned operation is completed at a time $t = 0$ in Fig. 22(A). In Figs. 22(A) and 22(B), 1) is a synchronizing signal HP of 40 t0, 2) is an address which is valid when the drive mode H/R = "1" and is for identifying two scanning electrodes in the scanning electrode group, 3) is the drive mode H/R for drive the electrodes for a partial reloading when it is "1" (in a state of "High" in the drawings) and for a refresh-

ment when it is "0" (in a state of "Low" in the drawings), 4) is a voltage mode E/W for switching a combination of voltage waveforms in each drive mode, 5) is an address identifying the scanning electrode which is an object of the refresh driving, 6) is an address for seeking the scanning electrode group which is an object of a partial reloading drive, 7) is an address for reading state data from the identifying memory circuit 26, and 8) is an address for reading data from the display memory circuit 25 and identifying memory circuit 27.

At a time $t = 0$ in Fig. 22(A), the scanning electrode LD is being driven for a refreshment while the scanning electrodes LA and LB are being driven for a partial reloading, and then, until a time $t = 12t_0$ the scanning electrode group 0, or the scanning electrodes L0 and L1, is to be partially reloaded. For a period $t = 12t_0$ to $36t_0$ in Fig. 22(B), the scanning electrode L2 is driven for a refreshment, and the scanning electrodes L0 and L1 are driven for a partial reloading.

I) Fig. 14(A) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and the signal electrodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 2 is followed by the voltage which is substantially the same value as the voltage of the polarity 1,

II) Fig. 14(B) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and the signal elec-

trodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 1 is followed by the voltage of a polarity 2, which is substantially the same value as the voltage of the polarity 1,

III) Fig. 14(A) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a refreshment, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage applied to the scanning electrodes, and

IV) Using Fig. 14(B) as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes.

Fig. 39 shows voltages applied to the scanning electrodes LD, L2 and L6, and signal electrodes S1, S2 and S5 for a period $t = 0t_0$ to $48t_0$, while Fig. 40 shows voltages applied to the pixels A21, A22, A61 and A62.

Fig. 14(A) shows a combination of voltage waveforms for reloading pixels on scanning electrodes into a first stable state, similar to the conventional embodiment in Fig. 29(A), and its description is omitted. A difference between Fig. 14(A) and Fig. 29(A) is that Fig. 14(A) satisfies the requirement of I) because the voltage B-C of 7) and the voltage B-G of 8) are combinations of voltage waveforms where the voltage of positive polarity is followed by the voltage of negative polarity, but Fig. 29(A) does not satisfy the requirement of I) because the voltage B-G of 8) is a combination of voltage waveforms where the voltage of negative polarity is followed by the voltage of positive polarity.

Fig. 14(B) is also a combination of voltage waveforms for reloading pixels of scanning electrodes into a second stable state, similar to the conventional embodiment Fig. 29(B), and its explanation is omitted. A difference between Fig. 14(B) and Fig. 29(B) is that Fig. 14(B) satisfied the requirement of II) because the voltage F-D of 7) and the voltage F-H of 8) are combinations of voltage waveforms where voltage of negative polarity is followed by voltage of positive polarity, while Fig. 29(B) does not satisfy the requirement II) because the voltage F-H of 8) is a combination of voltage waveforms where voltage of positive polarity is followed by voltage of negative polarity.

Fig. 40 (1) shows a waveform of voltage applied to an pixel A21, Fig. 40 (2) shows at which

angle FLC molecules are positioned when the pixel A is the first stable state, and Fig. 40(3) shows an amount of light transmission when a deflection axis of a deflection plate is positioned at an angle $-\omega$. At time $4t_0$, the FLC molecules are positioned closer to an angle $-\theta$ rather than the angle $-\omega$ since before the time voltage of negative polarity is applied after voltage of positive polarity is applied three times. After that, although voltage of positive polarity is applied three times after voltage of negative polarity is applied, as already mentioned, first the FLC molecules swing up to -18° , but at the third time they can swing barely to -16° . At time $16t_0$, the FLC molecules are a little closer to an angle ω rather than an angle $-\omega$, and therefore, after that when voltage of negative polarity is applied after voltage of positive polarity is applied, the FLC molecules can first swing up to an angle 8° . This attains a larger swing than the angle 6° after a time 0 when voltage of negative polarity is applied after voltage of positive polarity is applied at third time.

In this way, since the FLC molecules swing farther away from the angle $-\omega$ each time a polarity of the bias voltage, positioning the deflection axis of the deflection plate close to the angle $-\omega$, a larger amount of light transmission can be observed each time the polarity of the bias voltage is altered. The amount of light transmission which is brought with reloading the pixel A21 by means of the refresh driving after a time $24t_0$ is partly absorbed as a high frequency component, and this leads to a decrease in flickers caused by the refresh driving. As a result, it becomes possible to skip-scan more scanning electrodes in the refresh driving, and there is no need of satisfying the formula (1) previously presented.

Actually, the FLC having 1024 scanning electrodes were driven every sixteen ones, and when four scanning electrodes were driven for a partial reloading after a single scanning electrode was driven for a refreshment, it took $360 \mu s$ to reload pixels on the single scanning electrode, and a display in which perceptible flickers are hardly caught can be obtained.

[Embodiment 4]

If swing of the FLC molecules after a time $24t_0$ in Fig. 40 can be smaller, an FLC with less noticeable flicker can be obtained. For the purpose, it is effective to make a memory angle 2ω larger so as to be closer to a tilt angle 2θ and to make a voltage V_0 applied to the pixel A21 just after the time $24t_0$ smaller in a range to $V_0/2$ at the lowest. Base upon the idea, Fig. 41 shows a combination of voltage waveforms where the smallest voltage V_0 in Fig. 14(A)(5) is made smaller in a range to $V_0/2$

at the lowest, and contrarily the third largest voltage $V_0/2$ is made larger in a range to V_0 at the highest. Fig. 41 shows a combination of voltage waveforms for reloading pixels on the scanning electrodes into a first stable state, similar to the conventional embodiment in Fig. 29(A), and the description about it is omitted.

In this case, with regard to combinations of four voltage waveforms,

I) Fig. 14(A) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the the scanning electrodes to which the non-selective voltage is applied and the signal electrodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 2 is followed by the voltage which is substantially the same value as the voltage of the polarity 1,

II) Fig. 14(B) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial reloading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes, whereby obtained is a combination of waveforms of voltage applied to the pixels composed of the scanning electrodes to which the non-selective voltage is applied and signal electrodes to which the reloading voltage is applied, and voltage applied to the pixels composed of the the scanning electrodes to which the non-selective voltage is applied and the signal electrodes to which the non-reloading voltage is applied, which appear in such a manner that the voltage of a polarity 1 is followed by the voltage which is substantially the same value as the voltage of the polarity 2,

III) Fig. 42(A) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a refreshment, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a first stable state, and a non-selective voltage

applied to the scanning electrodes, and

IV) Fig. 37(B) is used as a diagram showing a combination of voltage waveforms where a combination of a selective voltage applied to scanning electrodes to drive them for a partial re-loading, reloading and non-reloading voltages to and not to reload pixels on the scanning electrodes into a second stable state, and a non-selective voltage applied to the scanning electrodes.

Fig. 42 shows a waveform of voltage applied to the pixel A21, Fig. 42(2) shows at which angle the FLC molecules in Fig. 33 lie when the pixel A21 is in the first stable state, and Fig. 42(3) shows an amount of light transmission when a deflection axis of a deflection plate is adjusted to the angle $-\omega$. It is found in Fig. 42 that swing of the FLC molecules just after the time $24t_0$ is considerably smaller than the angle 14° in Fig. 40.

However, the swing of the FLC molecules when voltage $-3V_0/2$ is applied and voltage of positive polarity is applied just after the reloading of the pixels is greater, the operator must adjust the first voltage in Fig. 41(A)(5) while actually looking at a state of a display on the FLC. The combination of voltage waveforms in Fig. 41(A) brings about a less capability of reloading pixels, compared with the combination of voltage waveform in Fig. 14(A).

Instead of Fig. 14(B) showing a combination of the selective voltage applied to a scanning electrodes for a refresh driving, reloading and non-reloading voltages for reloading pixels on the scanning electrodes into a second stable state and not, and a non-selective voltage applied to the scanning electrode, a combination of voltage waveforms in Fig. 41(B) can be used, where the first voltage $-V_0$ in Fig. 14(B)(5) is made smaller in a range to $-V_0/2$ at the lowest, and instead the third voltage $-V_0/2$ is made larger in a range to $-V_0$ at the highest. Fig. 41(B) shows, similar to the conventional embodiment in Fig. 29(B), a combination of voltage waveforms for reloading the pixels on the scanning electrodes into a second stable state, and the description about it is omitted.

Combinations of voltage waveforms in Figs. 43 to 48(A) are combinations of voltage waveforms for reloading pixels on the scanning electrodes into a first stable state, similar to the conventional embodiment in Fig. 29(A), while combinations of voltage waveforms in Figs. 43 to 48(B) are combinations of voltage waveforms for reloading pixels on the scanning electrodes into a second stable state, similar to the conventional embodiment in Fig. 29(B), and the description about them is omitted.

Furthermore, instead of Fig. 41, Figs. 43 to 45 can be used.

Fig. 43(A) shows a combination of voltage waveforms when the first voltage V_0 in Figs. 14(B)-

(5) is made smaller in a range to $V_0/2$ at the lowest similar to Fig. 41(A) without a later compensation for it, while Fig. 43(B) shows a combination of voltage waveforms when the lowest voltage $-V_0$ in Fig. 14(B)(5) is made smaller in a range to $-V_0/2$ at the lowest similar to Fig. 41(B) without later compensation for it.

Fig. 44 shows a combination of voltage waveforms reversed in polarity to the bias voltage in Fig. 14 for advancing a time when polarity of the bias voltage in Fig. 40 is altered and swing becomes larger by $4t_0$. In this way, it is also useful to stagger a time of the maximum light transmission when the bias voltage is applied, to make flicker less noticeable.

Fig. 44 is an improvement of the concept of Fig. 43, which shows a combination of voltage waveforms where it is intended that a larger amount of light transmission brought with the reloading of the pixels by the refresh driving after the time $24t_0$ should be absorbed as a high frequency component by slightly raising the bias voltage when the refresh driving is performed.

Also, instead of the combination of voltage waveforms in Fig. 14, a combination of voltage waveforms in Fig. 46 may be used in the partial reloading drive. The combination of voltage waveforms in Fig. 46 seem to be effective when a dielectric anisotropy of the FLC is negative. Figs. 14 and Figs. 43 to 46 commonly denote that a time $4t_0$ is required, but actually, a time $3t_0$ is required and the voltage is zero for the last t_0 .

Since the combination of voltage waveforms in Fig. 41 brings about a less capability of reloading pixels, another combination of voltage waveforms may be employed so that a larger voltage may be applied in biasing only in the refresh drive as in Fig. 48. In this case, voltage V_1 in Figs. 47(A)(7) and 47(A)(8) are commonly of positive polarity while voltage in Figs. 47(B)(7) and 47(B)(8) are commonly of negative polarity, and hence, there is nothing to worry about the reloading of pixels by an accumulated response. It is sure voltage $2V_1 = 3V_0/2$.

Sometimes there is a case where you certainly need to heighten an apparent contrast, though it is not suitable for the partial reloading drive. If so, Fig. 14 is not exclusive but Fig. 43 may be an alternative.

It is not necessary to continuously apply a combination of voltage waveforms which satisfies the requirement in I) to pixels for a partial reloading drive and then apply combinations of voltage waveforms which satisfies the requirements in III) and IV) to the pixels for a refresh drive, but an alternative may be something like that a combination of voltage waveforms which satisfies the requirement in II) to pixels for a partial reloading

drive and then a refresh drive is performed. In this case, the control circuit 13 may operate as in Fig. 49 instead of Fig. 8, and the operation can be implemented with a slight variation of a logic formula for obtaining the drive mode H/R and voltage mode E/W.

As has been described, combining the driving method of the N : 1 skip scanning of this invention with the driving method in the Japanese Unexamined Patent Publication No. 59389/1989, a good display where flickers are less conspicuous and an image is not varied every several scanning electrodes can be obtained. If required, a less memory capacity of a single screen plus &A (approximately 1/8 of a screen) may be enough.

Further, as mentioned in the above Embodiment 3, of the 1024 scanning electrodes in the FLCDD, every sixteenth was driven for a refreshment, a single scanning electrode was driven for a refreshment, and then four scanning electrodes were driven for a partial reloading, and consequently, a display with no noticeable flicker could be obtained though it took 360 μ s. In this case, a single field refresh cycle T_R is expressed as follows:

$$T_R = 360 \mu s \times (1 + 4) \times 1024/16 = 115.2 \text{ ms}$$

which does not satisfy the formula (1), but a display where flickers were hardly noticeable could be obtained. Allowing for these facts, it is found that the effect of the present invention should be apparent.

Claims

1. A display control method in which a ferroelectric liquid crystal is interposed between a plurality of scanning electrodes and a plurality of signal electrodes both of which are disposed orthogonal to each other, pixels are formed by defining regions where the scanning electrodes and the signal electrodes intersect, selective voltage is applied to a single scanning electrode of the scanning electrodes to reload pixels on the single scanning electrode, non-selective voltage is applied to all the other scanning electrodes to prevent the pixels on the single scanning electrode from being reloaded,

reloading bright voltage, reloading dark voltage or non-reloading voltage is applied to the signal electrodes depending upon whether the pixels on the scanning electrode to which the selective voltage is applied should be reloaded into a dark state of a display or a bright state of a display, or not utterly reloaded, characterized in that

if there is no difference between data to be displayed through the pixels on the scanning electrode to which the selective voltage is applied and data already displayed, the reloading dark voltage is applied to the signal electrodes when the data to be displayed are dark while the reloading bright voltage is applied to the signal electrodes when the data to be displayed are bright, but if there is any difference between the data to be displayed and the data already displayed, the data already displayed are retained by applying the non-reloading voltage to the signal electrodes.

2. A display control method, characterized in that in accordance with a display control method as in claim 1, all the scanning electrodes are uniformly divided into groups of a plurality of the adjacent scanning electrodes, the selective voltage is successively applied to one of the scanning electrodes of each of the scanning electrode groups, thereafter an operation that the selective voltage is successively applied to another scanning electrode of each scanning electrode group is successively repeated, and the selective voltage is successively applied to the last one of the scanning electrodes of each scanning electrode group.

3. A display control method characterized in that a switch of process is performed between a display control method as in claim 2 and another method in which the selective voltage is applied to the scanning electrodes having a difference between data to be displayed through them and data already displayed to reload pixels on the scanning electrodes while the non-selective voltage is applied to the other scanning electrodes so as not to prevent pixels on the scanning electrodes from being reloaded, the reloading dark voltage is applied to the signal electrodes when the data to be displayed are dark while the reloading bright voltage is applied to the signal electrodes when the data to be displayed are bright if the pixels on the scanning electrodes to which the selective voltage is applied are different from the data to be displayed,

after the selective voltage is applied to a certain number of the scanning electrodes in accordance with the latter method, the selective voltage is applied to the certain number of the scanning electrodes in accordance with the former method.

4. A display control method in which a ferroelectric liquid crystal is interposed between a plurality of scanning electrodes and a plurality of

signal electrodes both of which are disposed orthogonal to each other, pixels are formed by defining regions where the scanning electrodes and the signal electrodes intersect, and a switch of process is performed between a partially reloading drive for reloading a state of a display of the pixels and a refresh drive for retaining the state of a display of the pixels, characterized in that

a periodical switch of process is performed in each of the drives between

a process in which selective voltage is applied to a single scanning electrode of the scanning electrodes to reload pixels on the single scanning electrode, non-selective voltage is applied to all the other scanning electrodes to prevent the pixels on the single scanning electrode from being reloaded, voltage is applied to the signal electrodes depending upon whether the pixels on the scanning electrode to which the selective voltage is applied should be reloaded into a dark state of a display or a bright state of a display, or not utterly reloaded, and

a process in which voltage is applied to the signal electrodes depending upon whether the pixels on the scanning electrode to which the selective voltage is applied should be reloaded into a bright state of a display or not utterly reloaded.

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FIG. 1

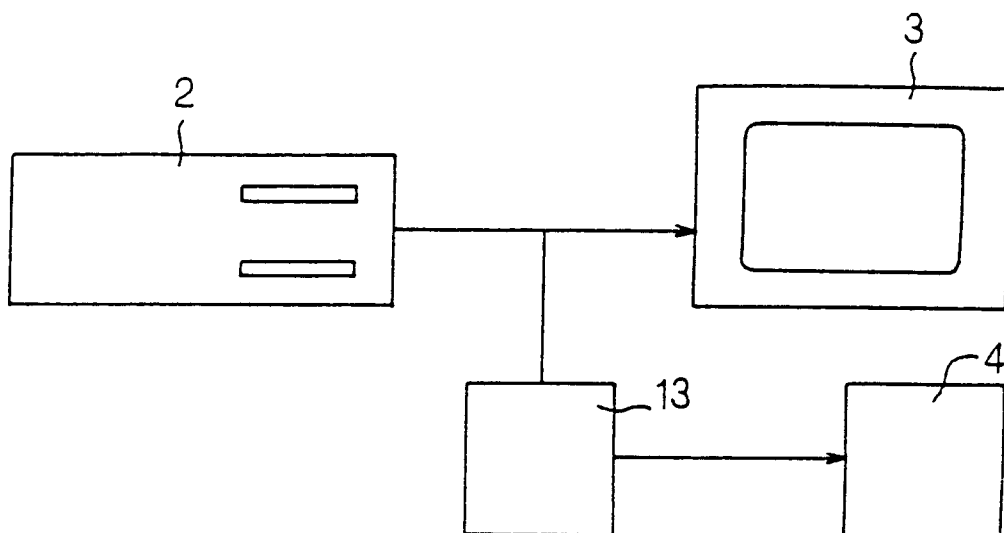


FIG. 2

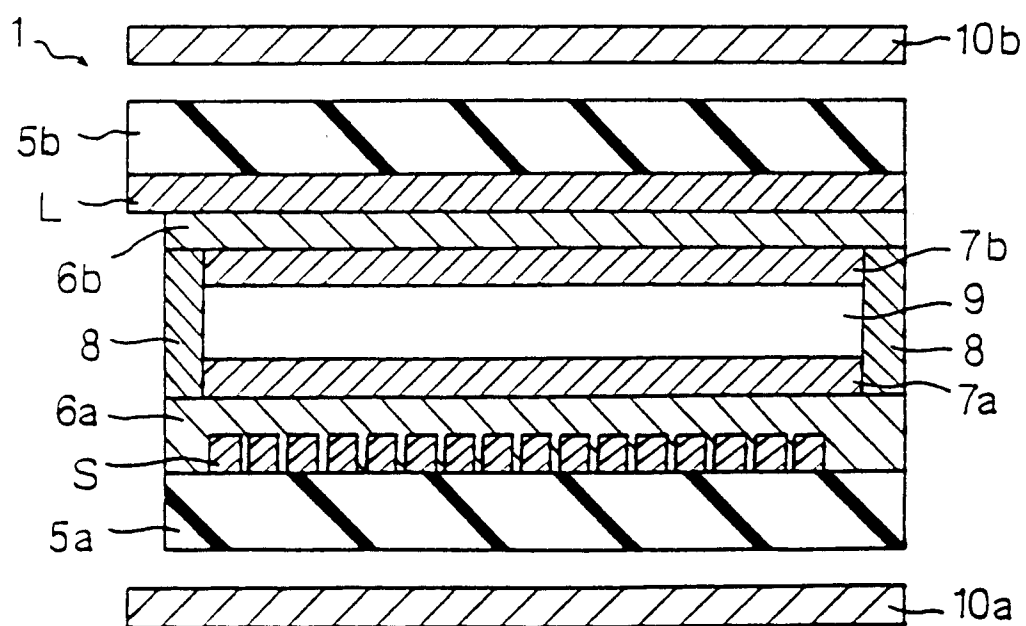


FIG. 3

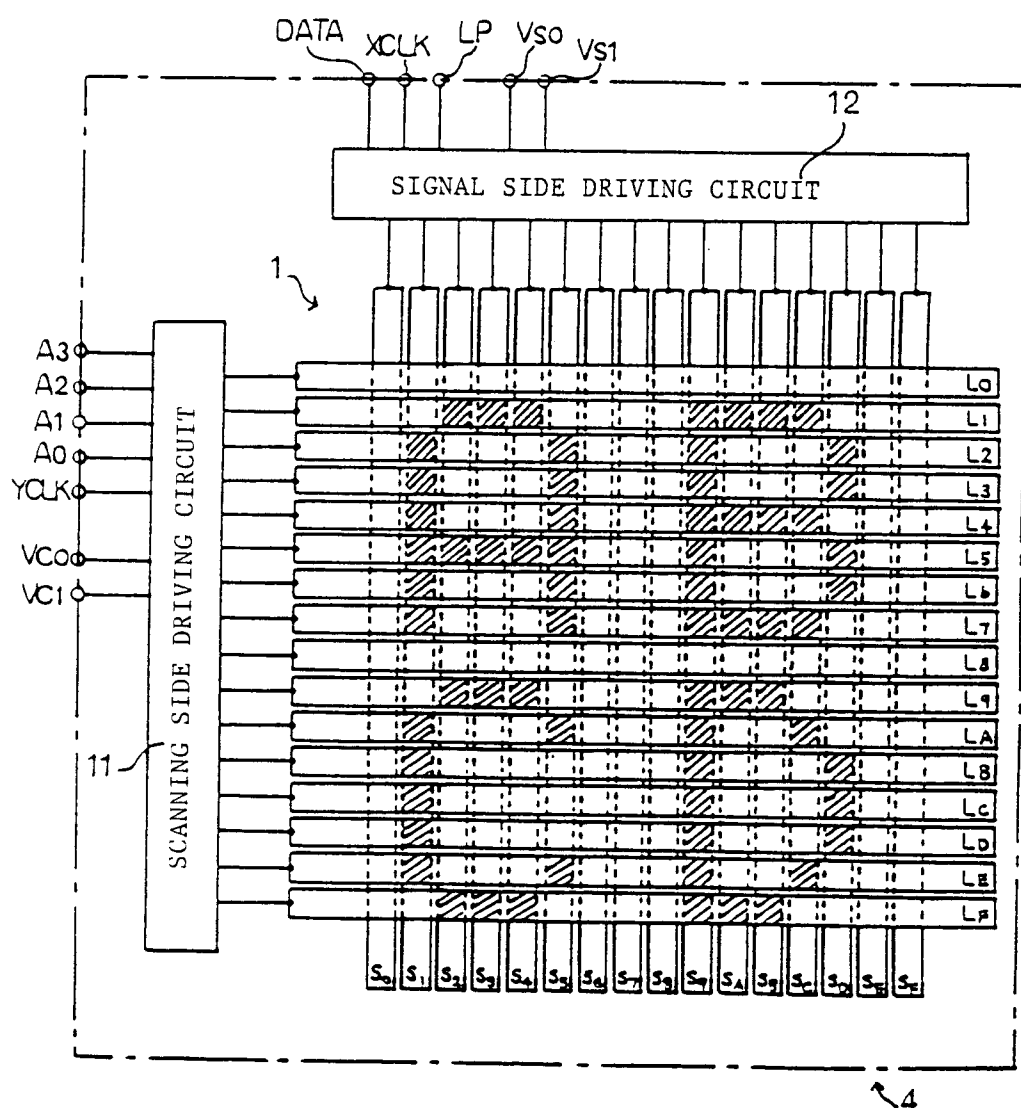


FIG. 4

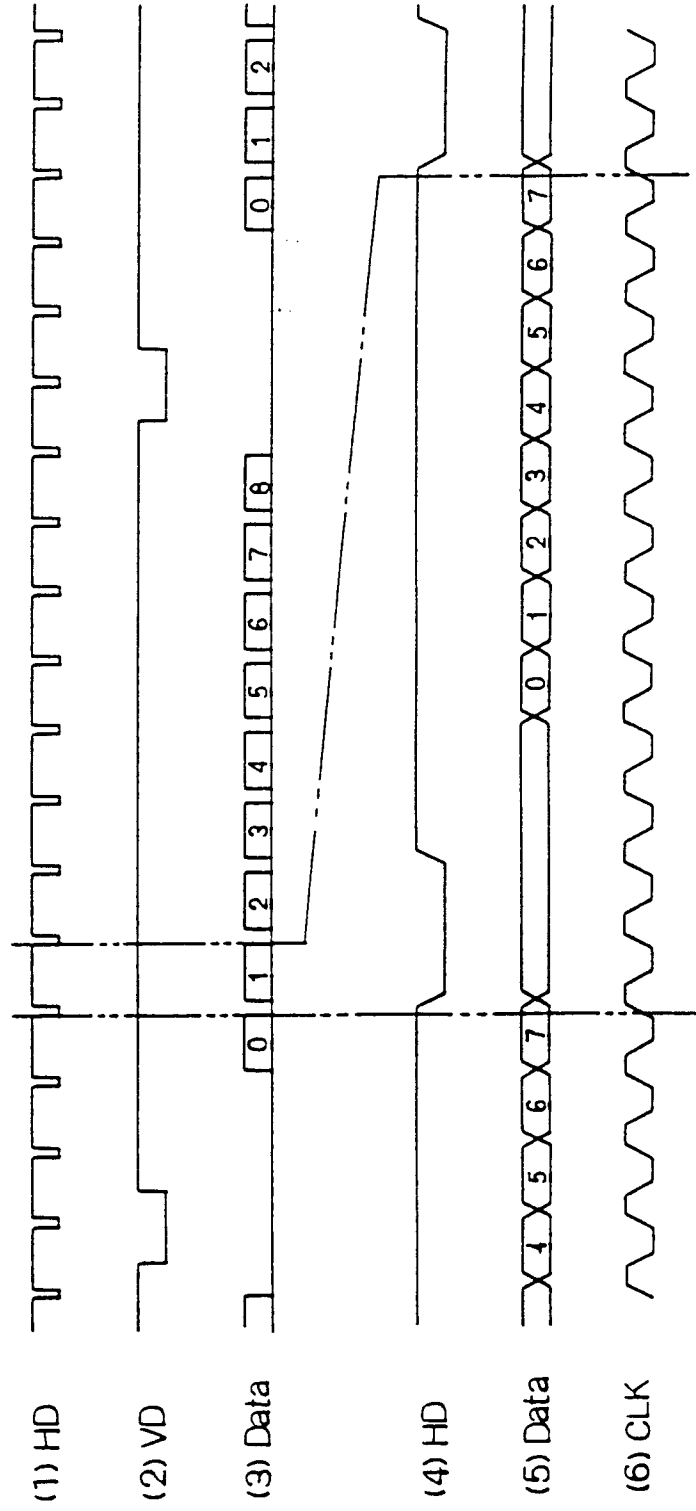


FIG. 5

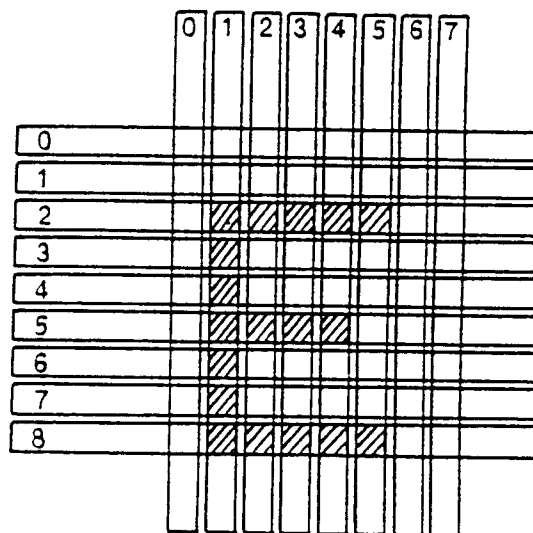


FIG. 6

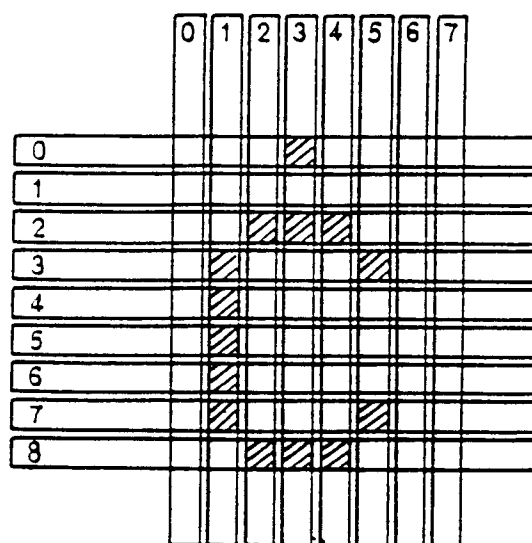


FIG. 7

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

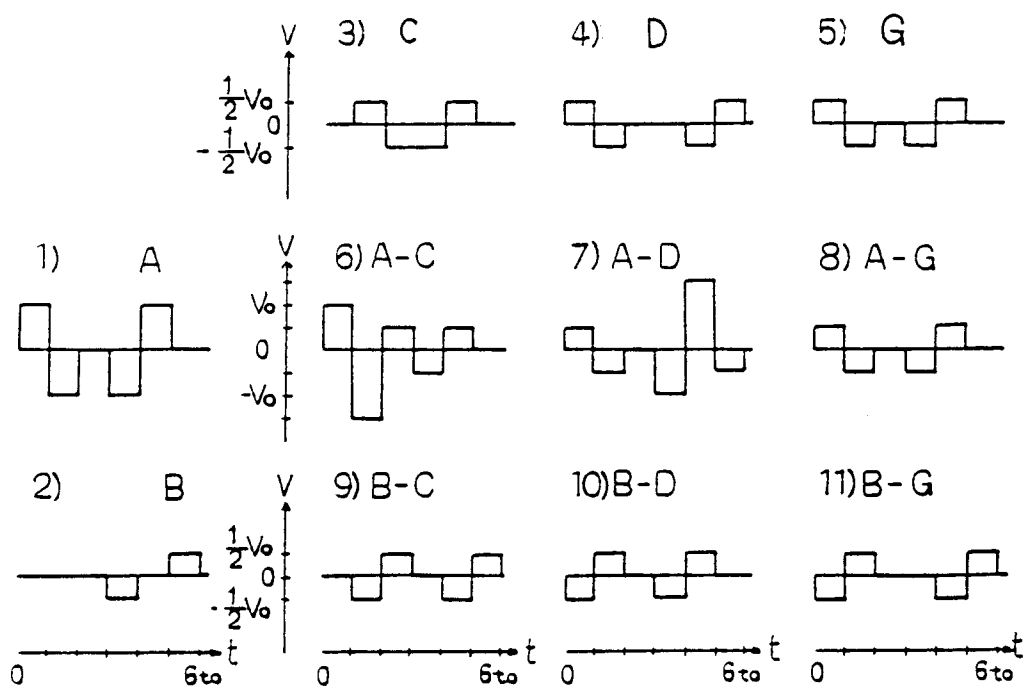
FIG. 8

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

FIG.9

	0	1	2	3
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
A				
B				
C				
D				
E				
F				

FIG. 10



- 1) SELECTIVE VOLTAGE A
- 2) NON-SELECTIVE VOLTAGE B
- 3) RELOADING DARK VOLTAGE C
- 4) RELOADING BRIGHT VOLTAGE D
- 5) NON-RELOADING VOLTAGE G

FIG.11

	0	1	2	3	4	5	6	7
0								
1								
2								
3								
4								
5								
6								
7								

FIG.12

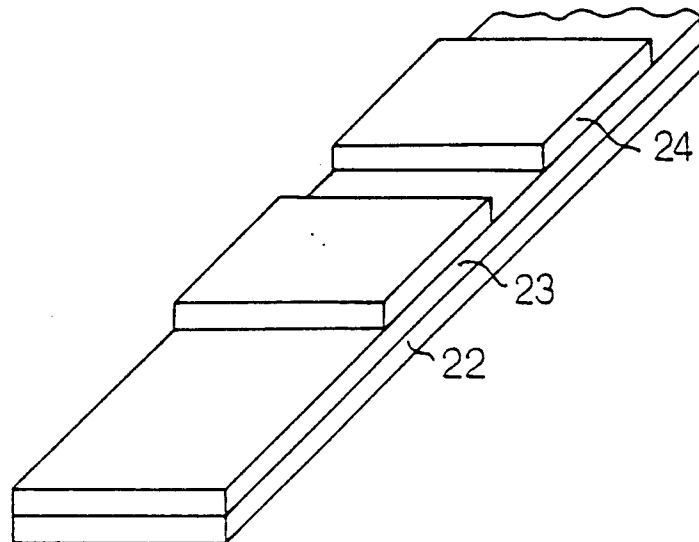


FIG.13

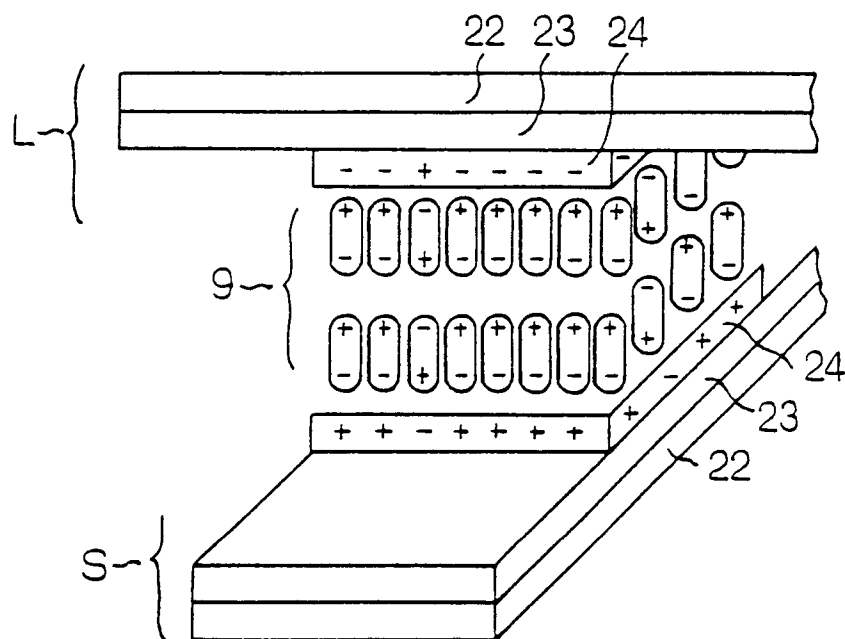
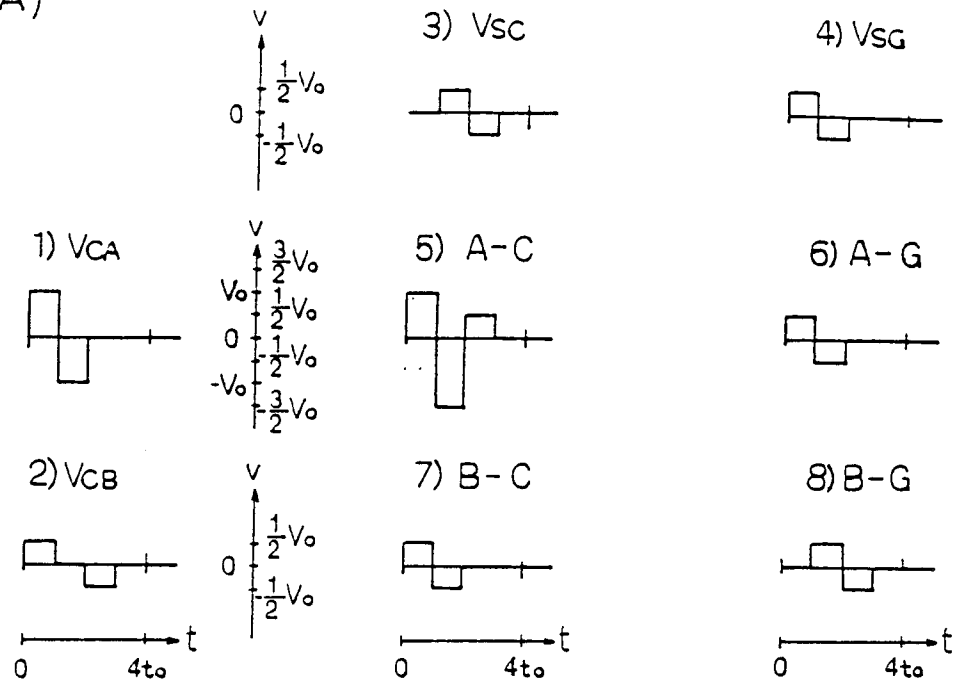


FIG.14

(A)



(B)

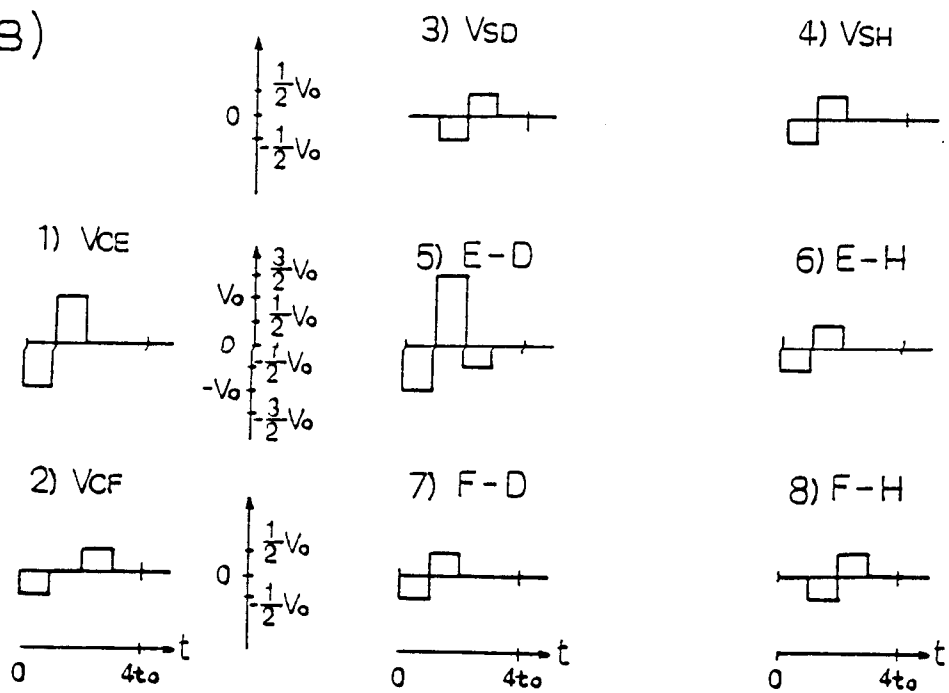


FIG. 15

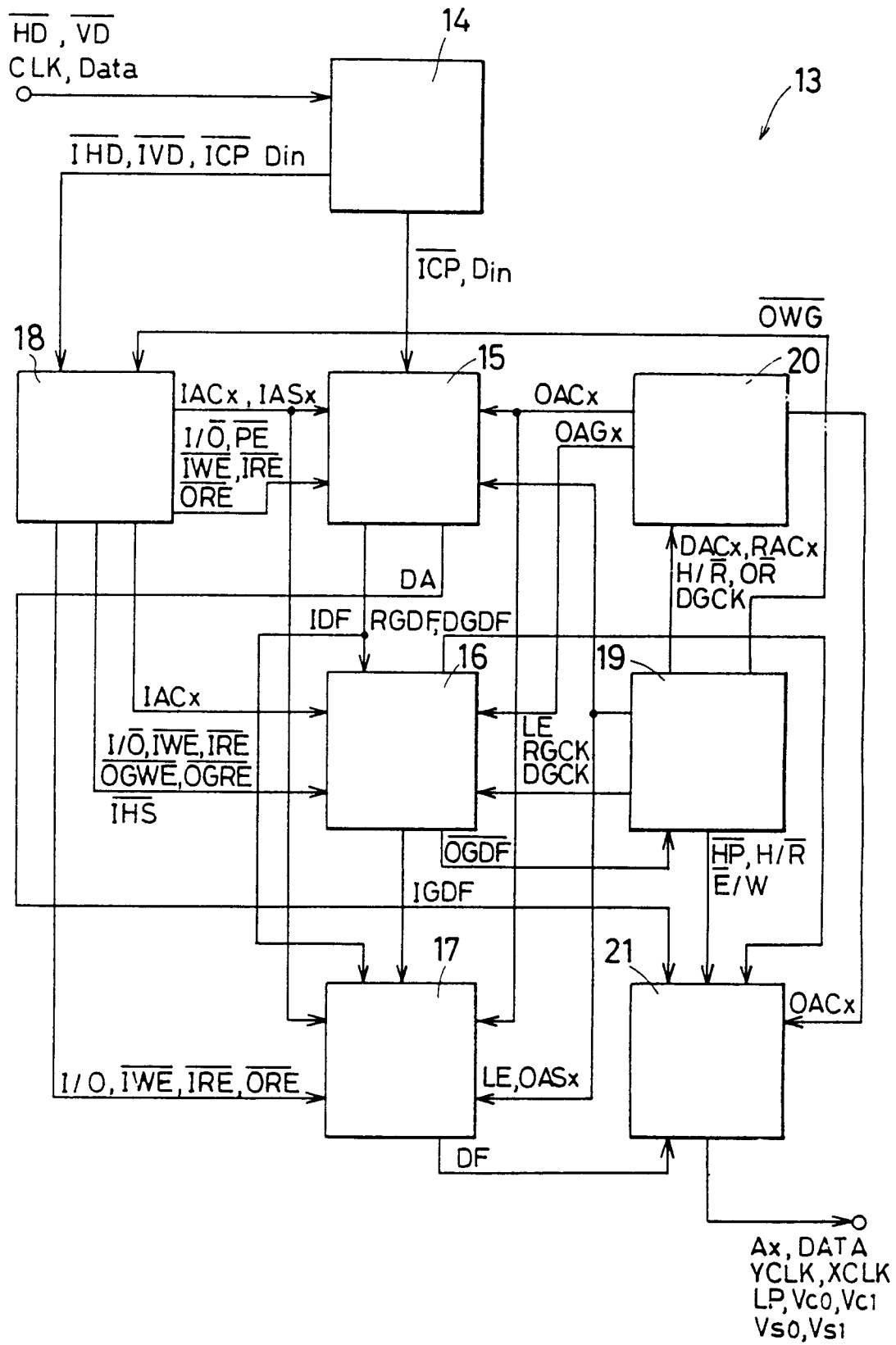


FIG.16

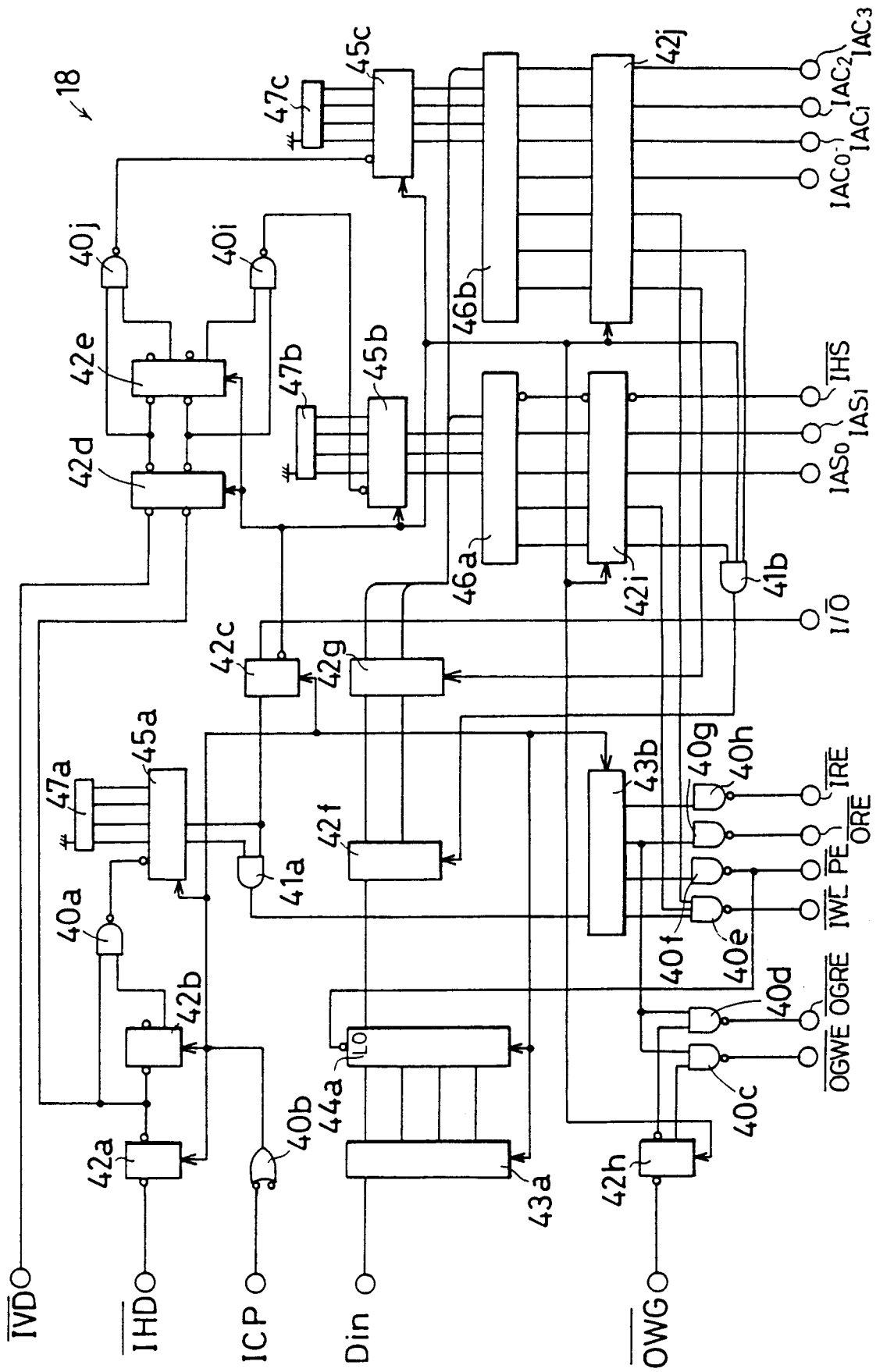


FIG. 17

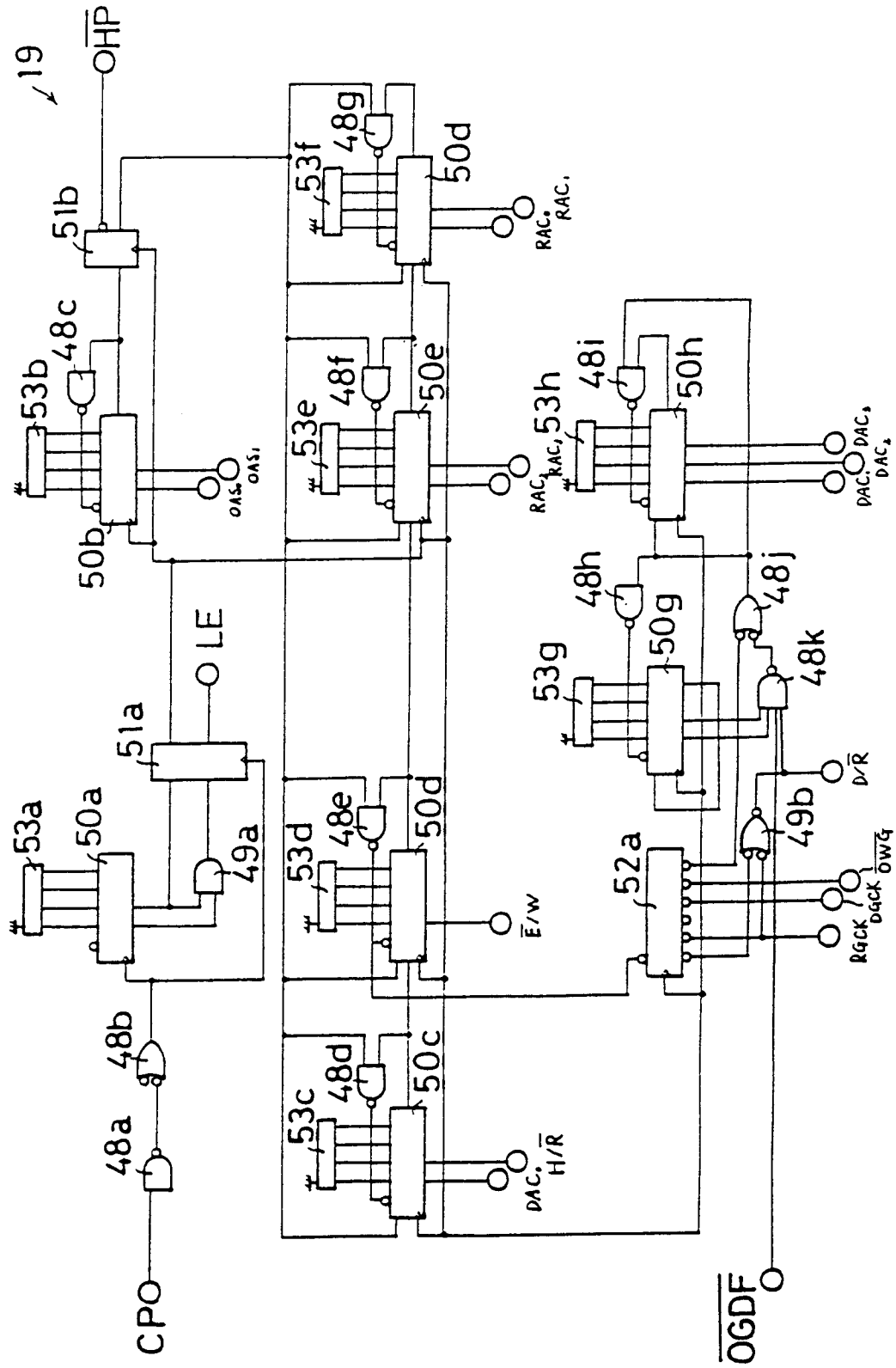


FIG. 18

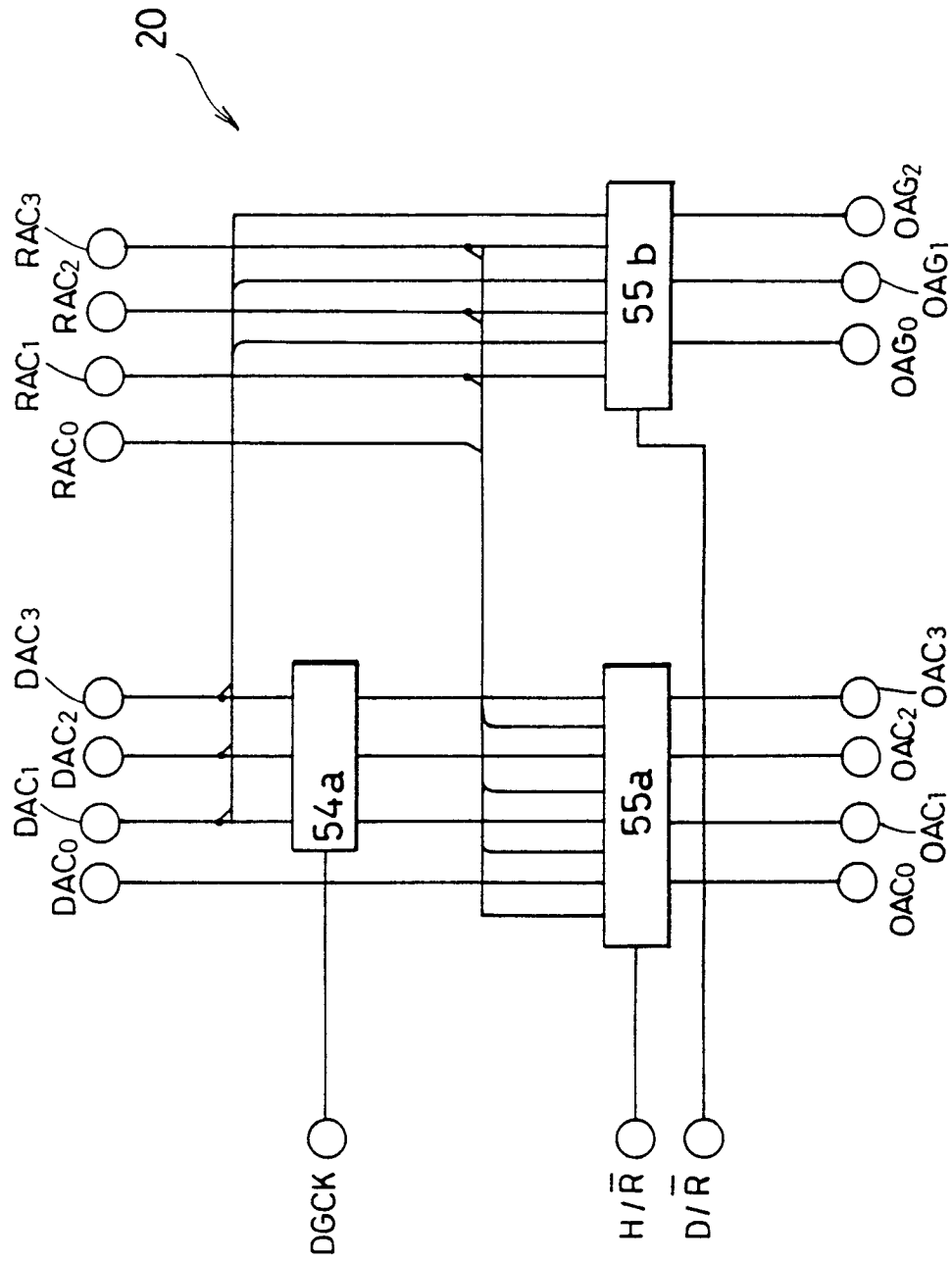


FIG. 19

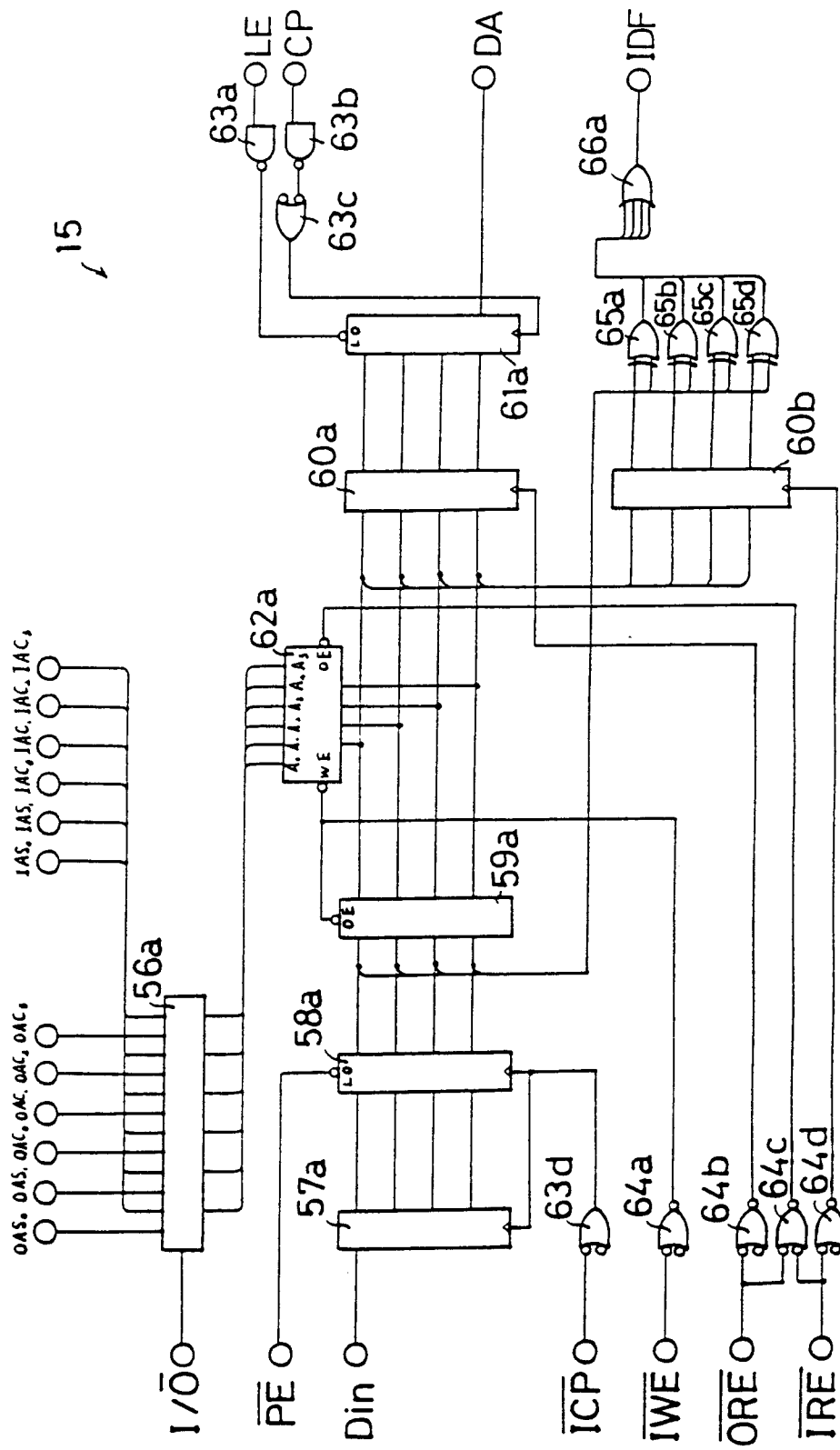


FIG. 20

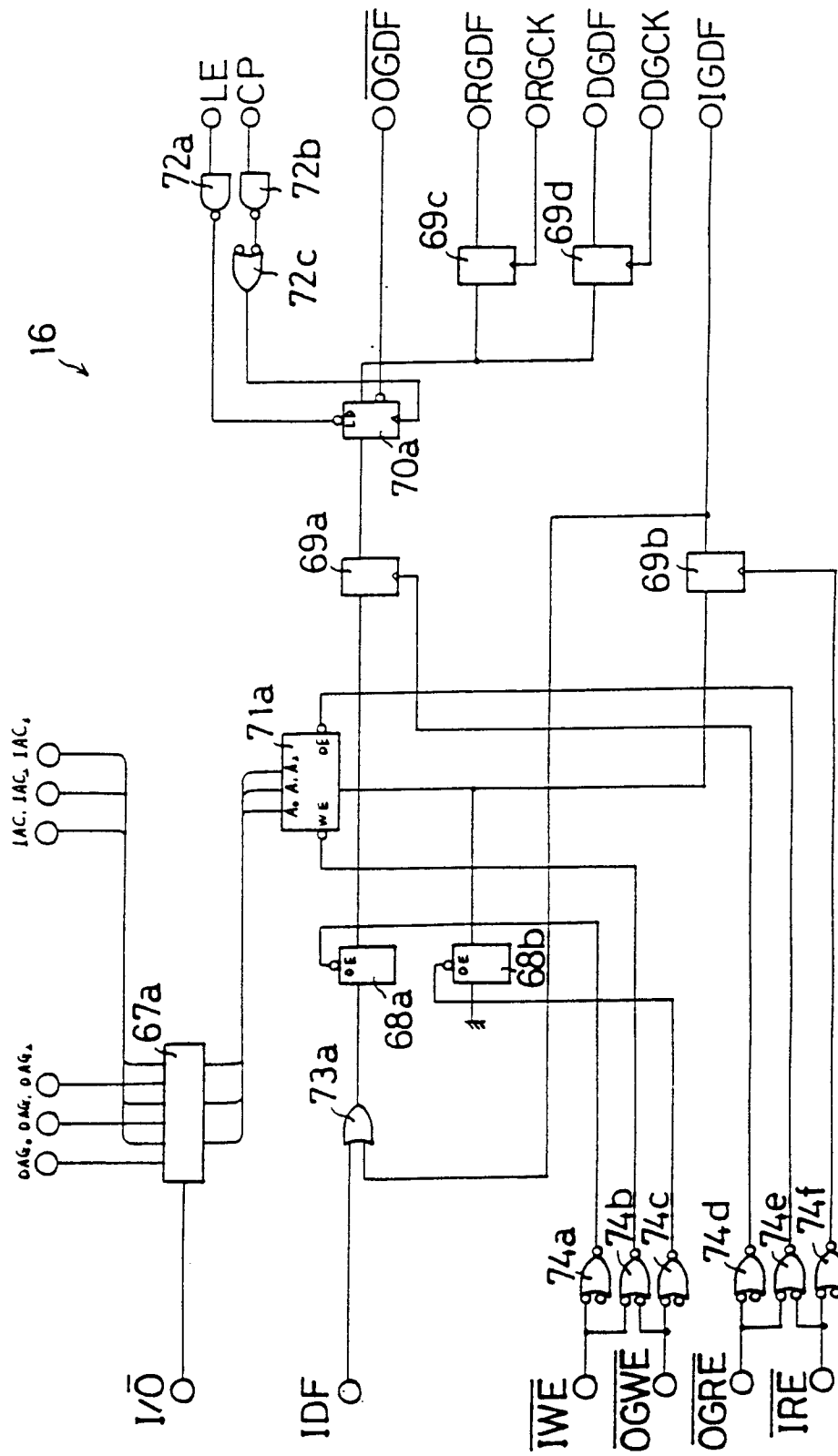


FIG. 21

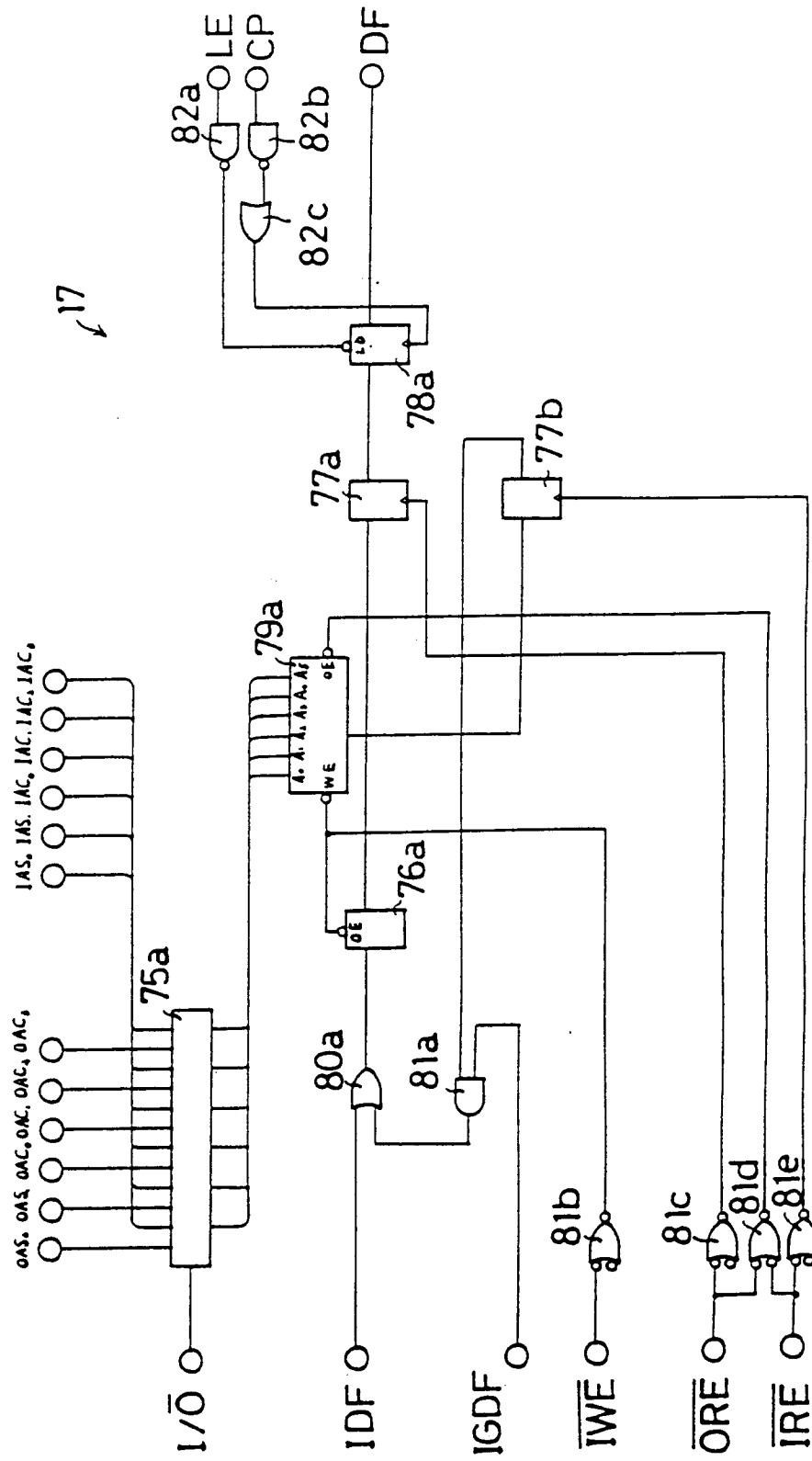


FIG. 22

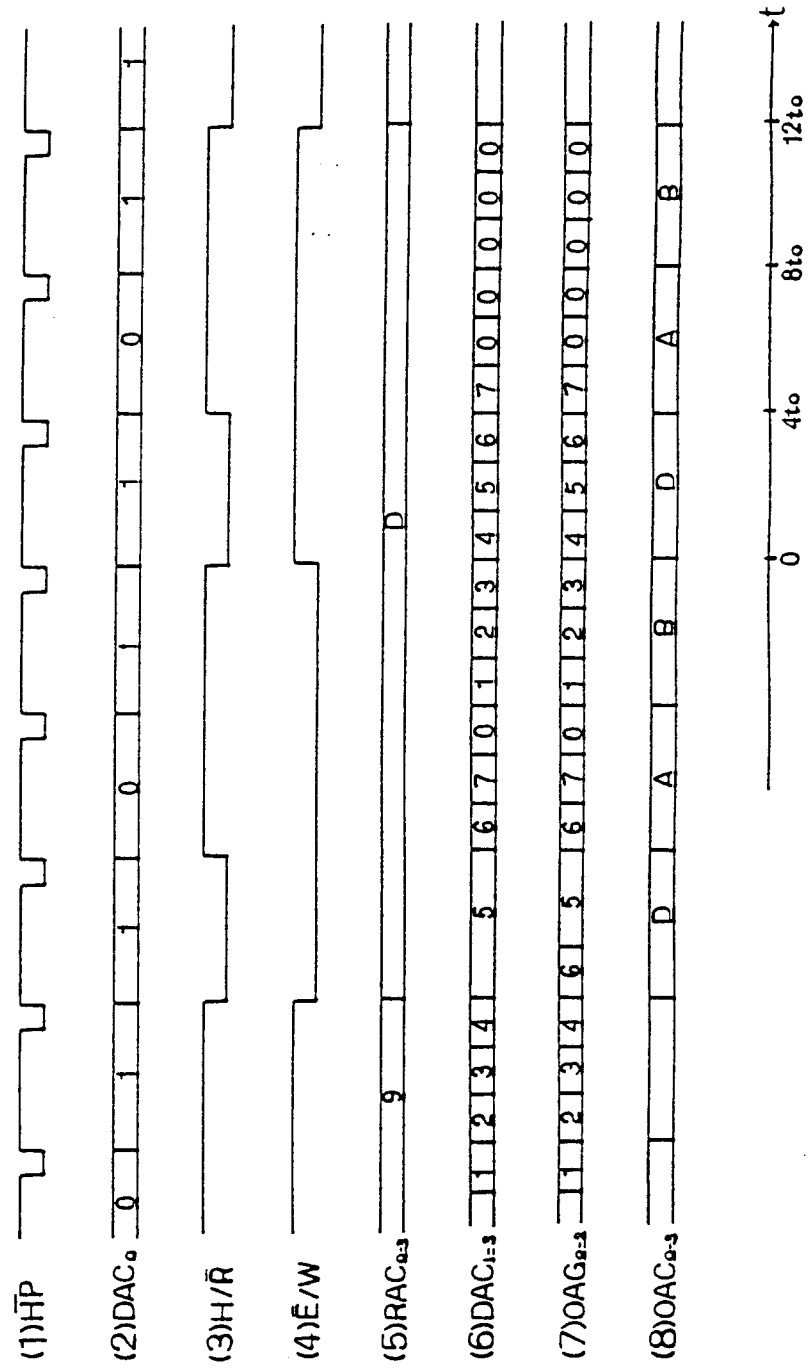


FIG. 23

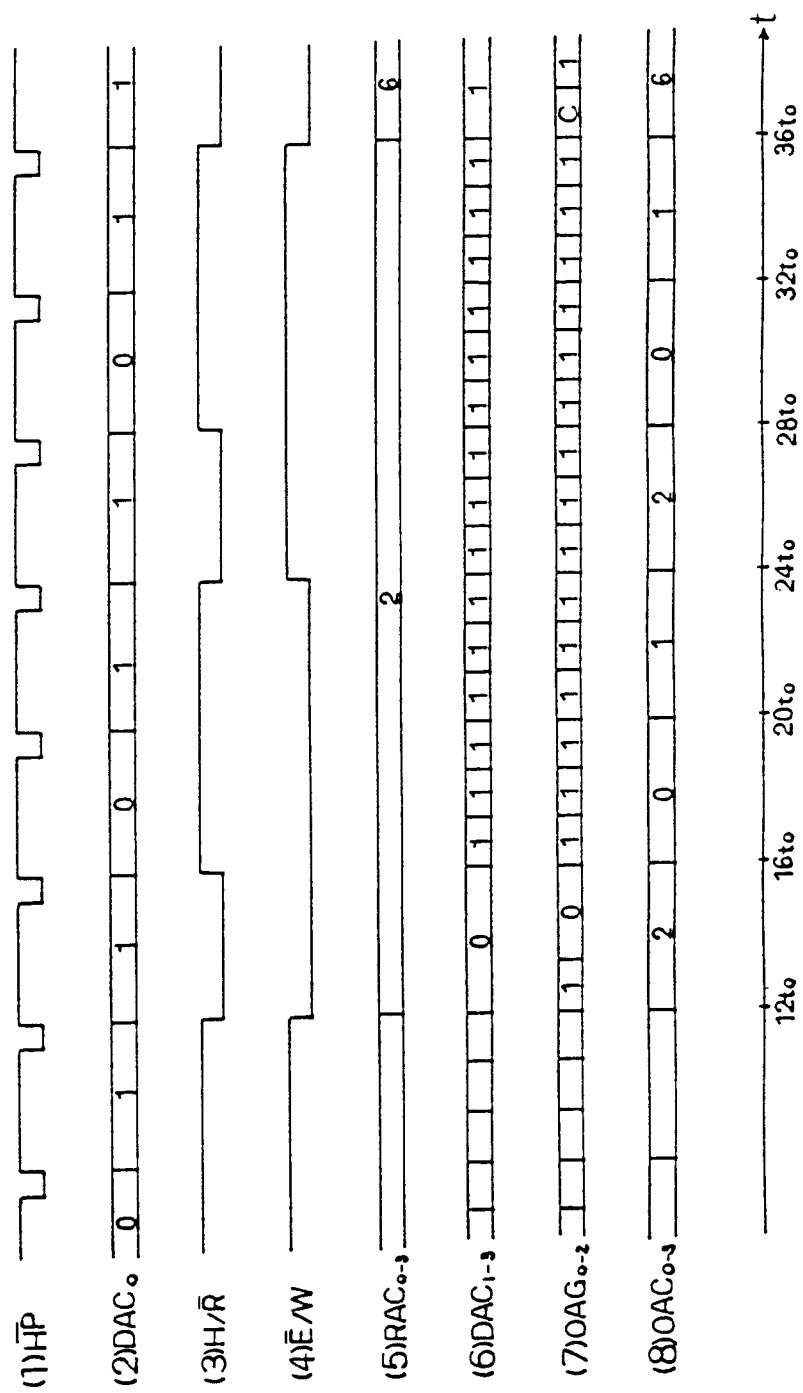


FIG. 24

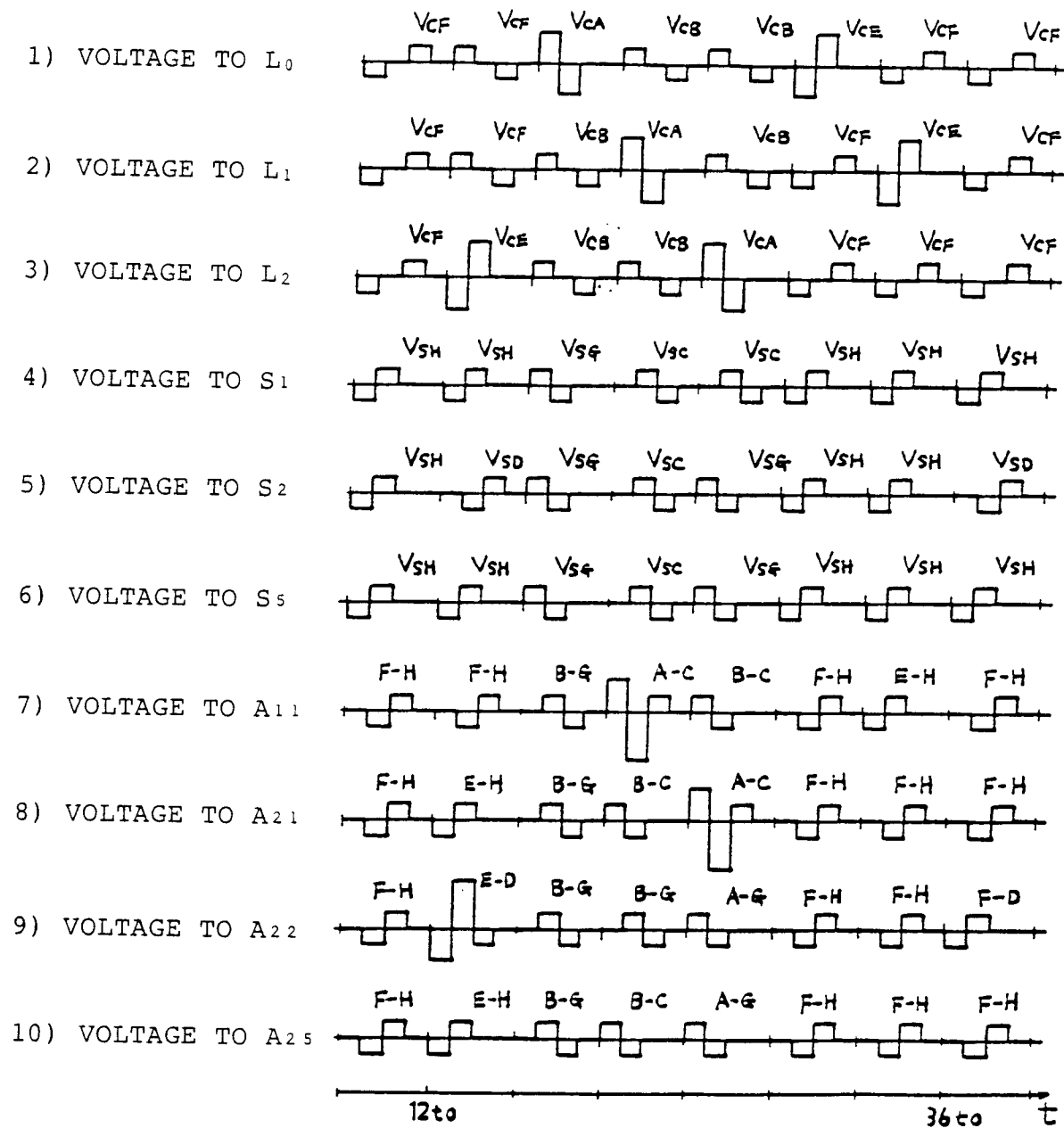


FIG. 25

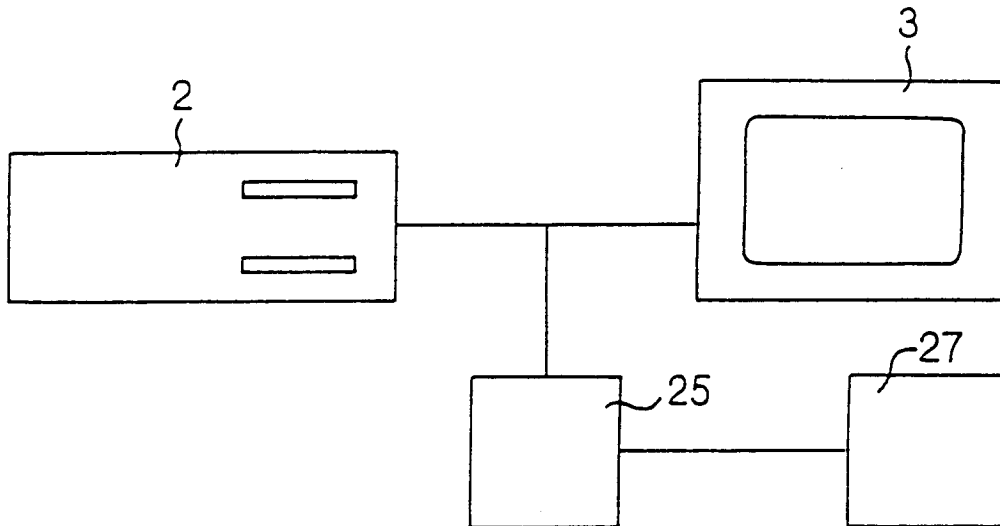


FIG. 26

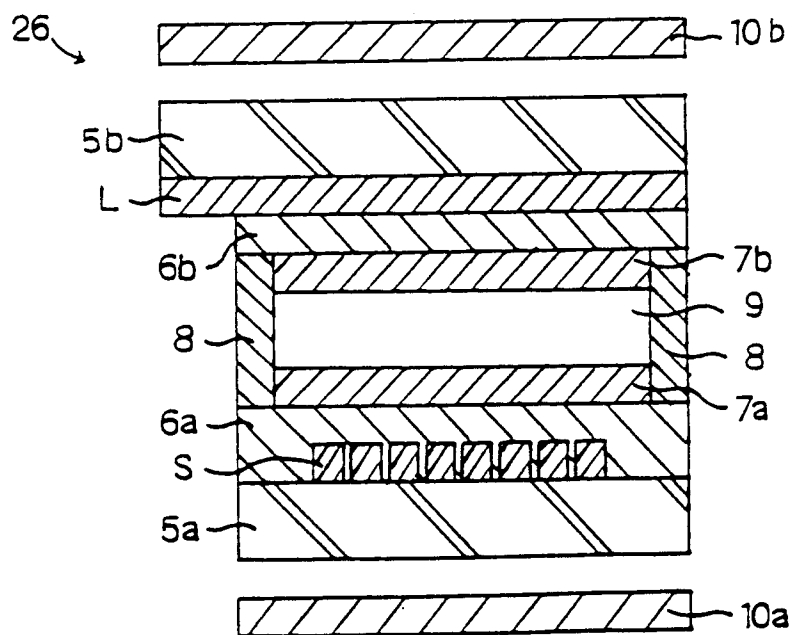


FIG. 27

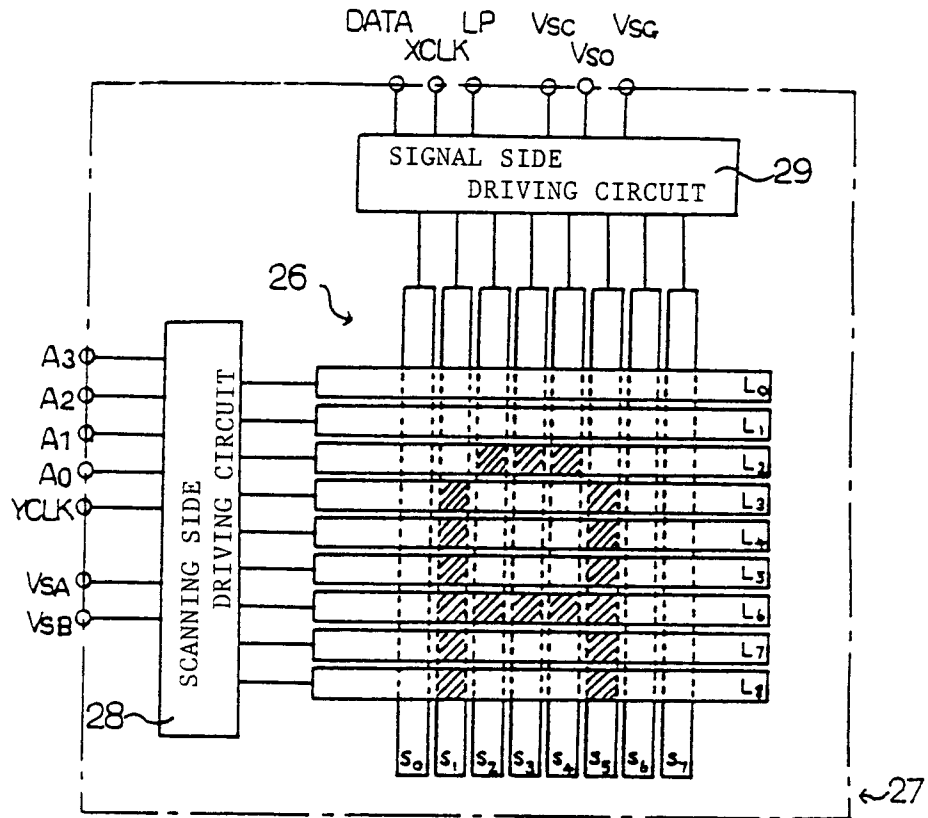


FIG. 28

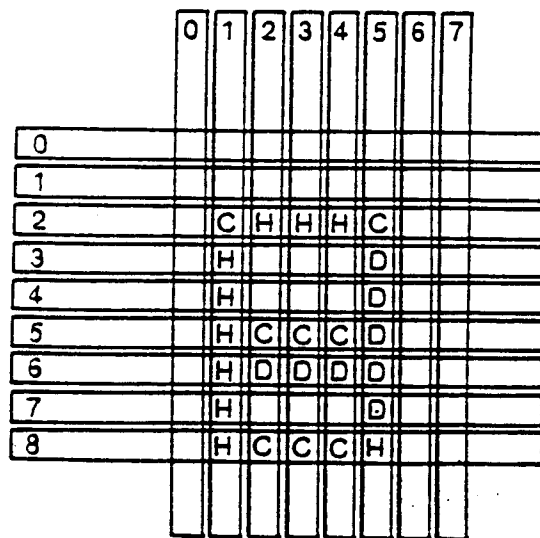


FIG. 29

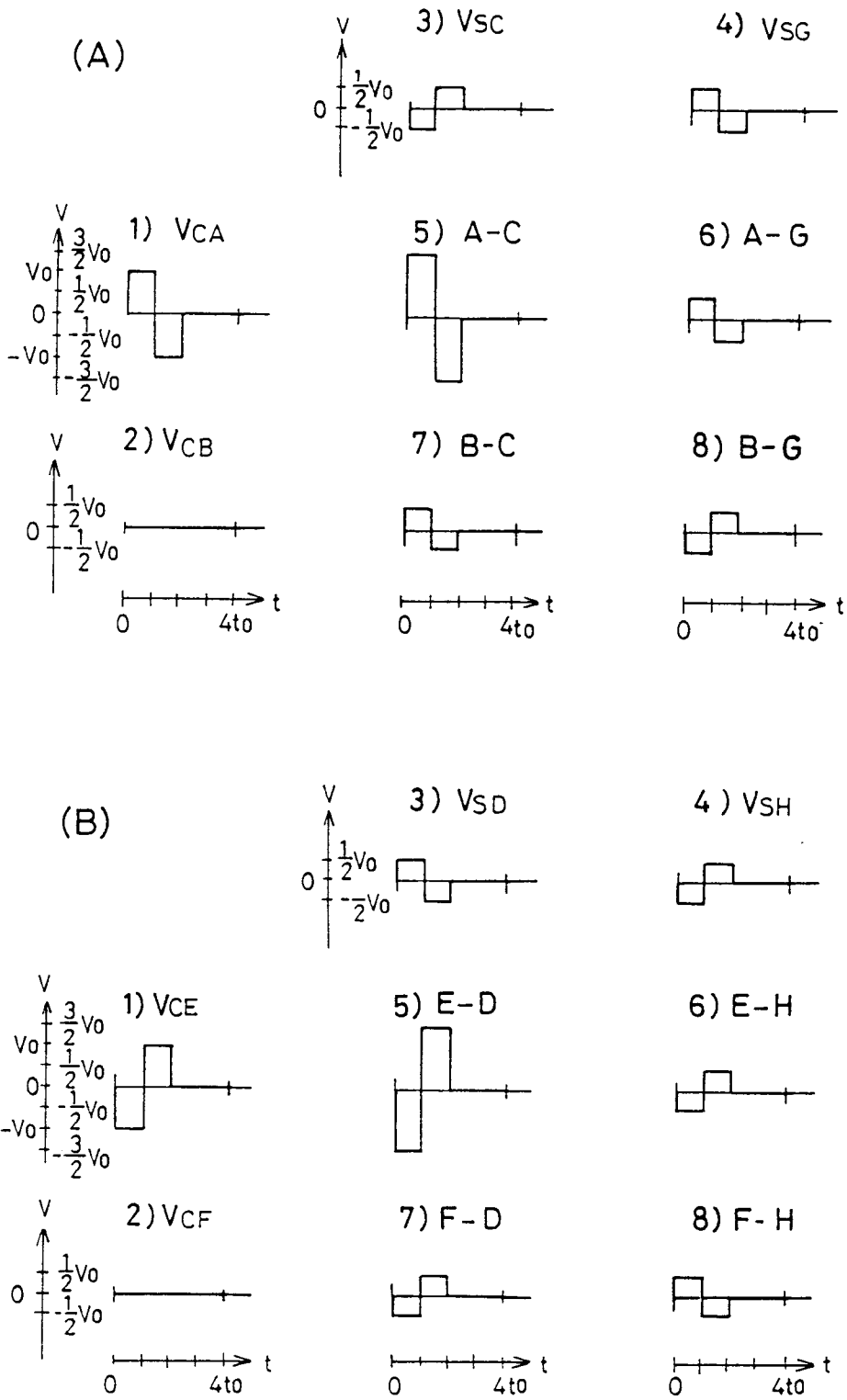


FIG. 30

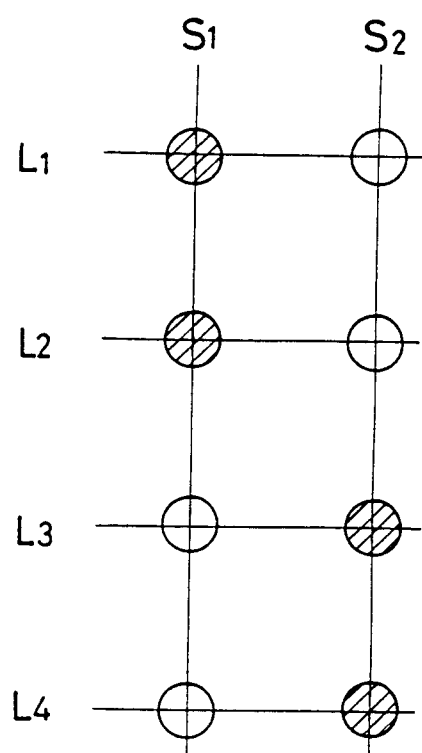


FIG. 31

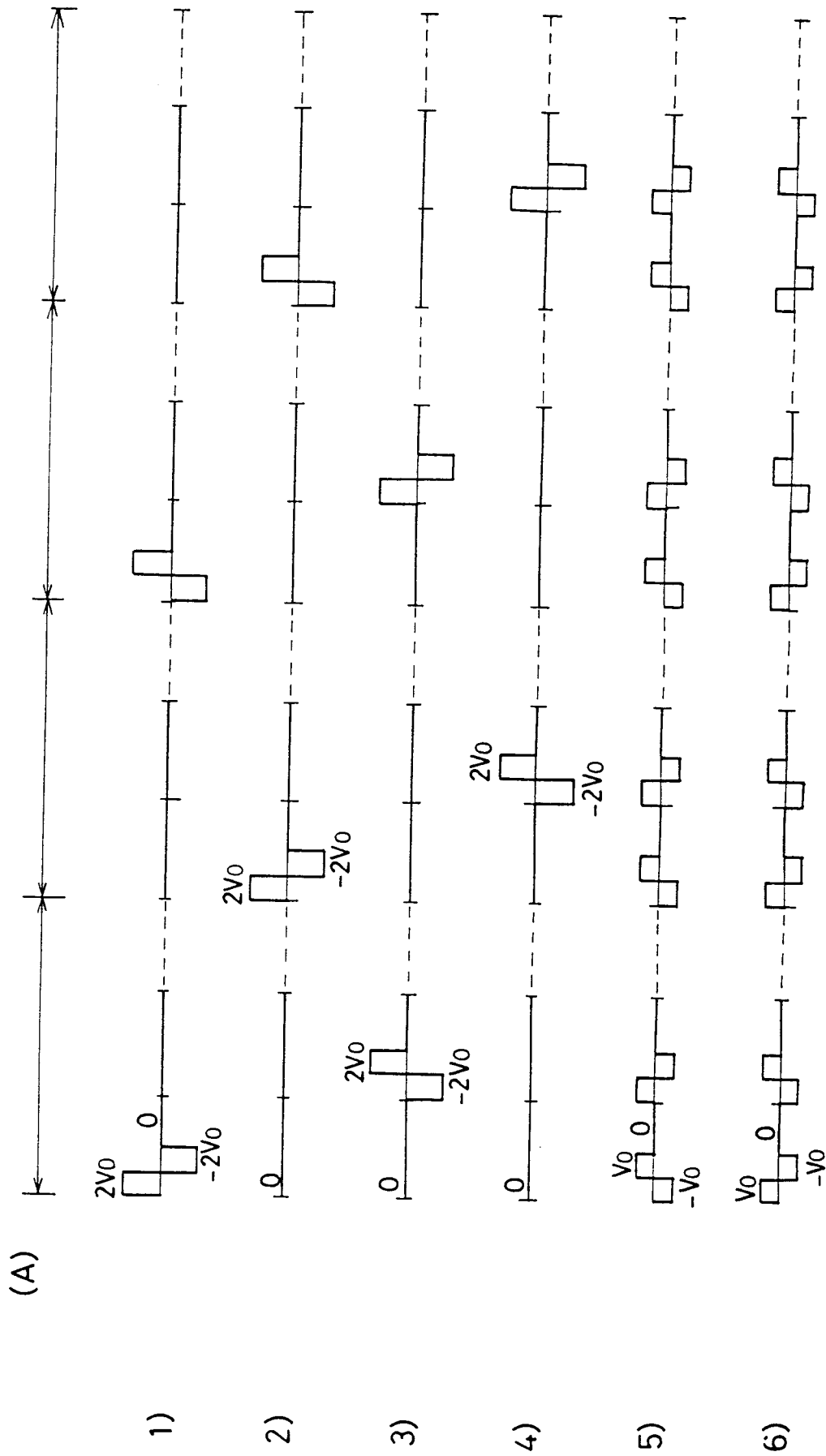


FIG. 32

(B)

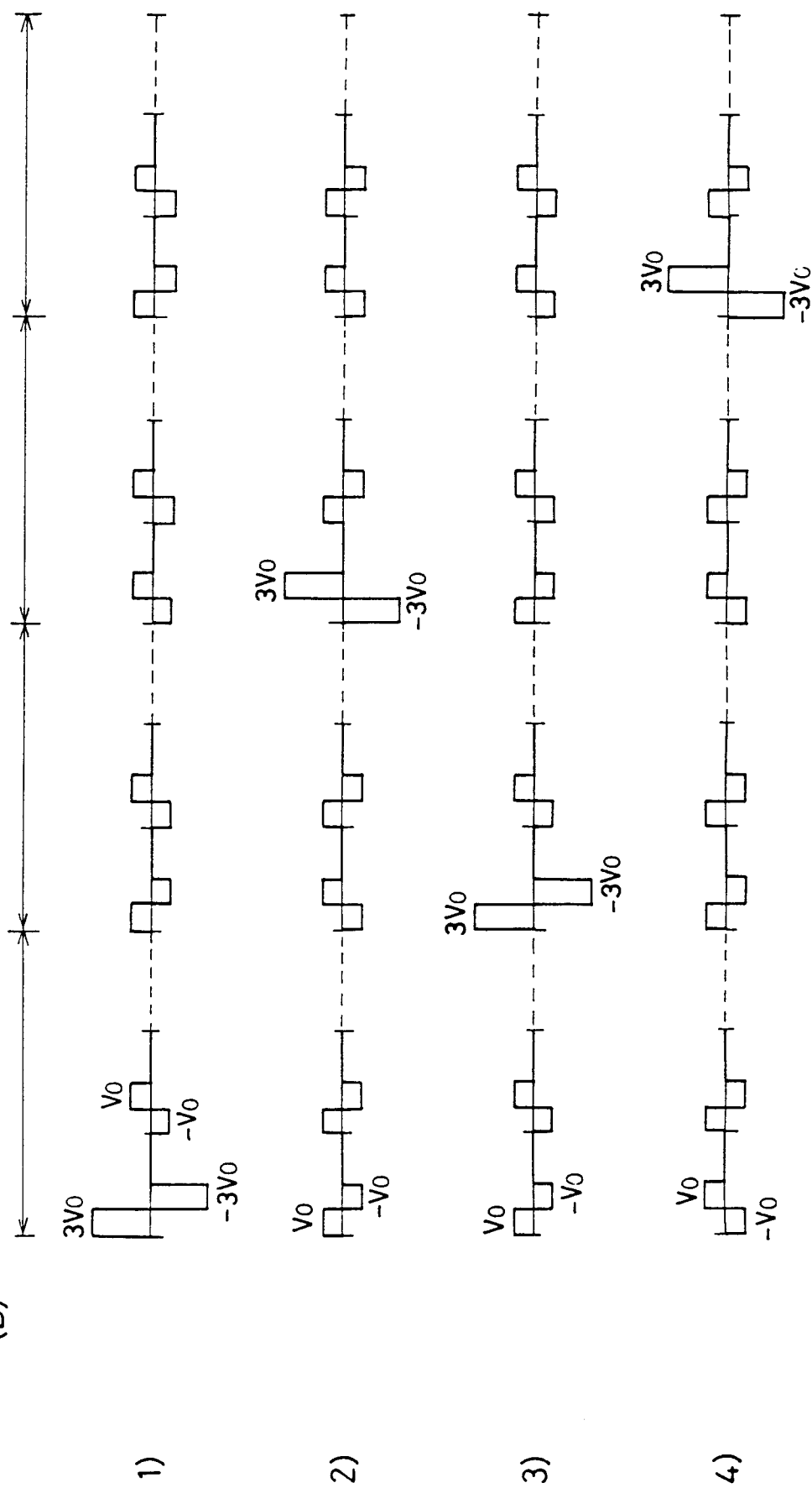


FIG. 33

(A)

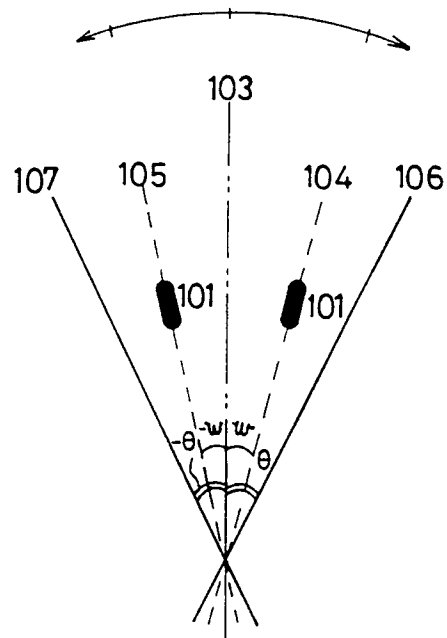


FIG. 34

(B)

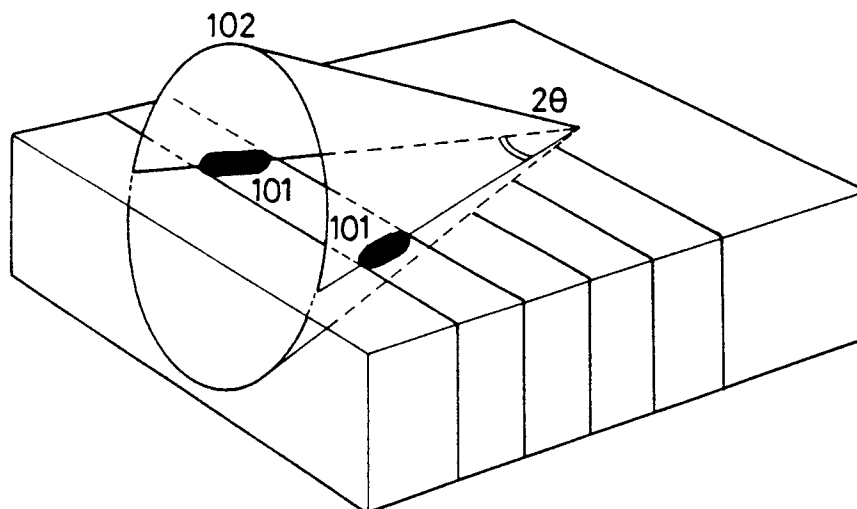


FIG. 35

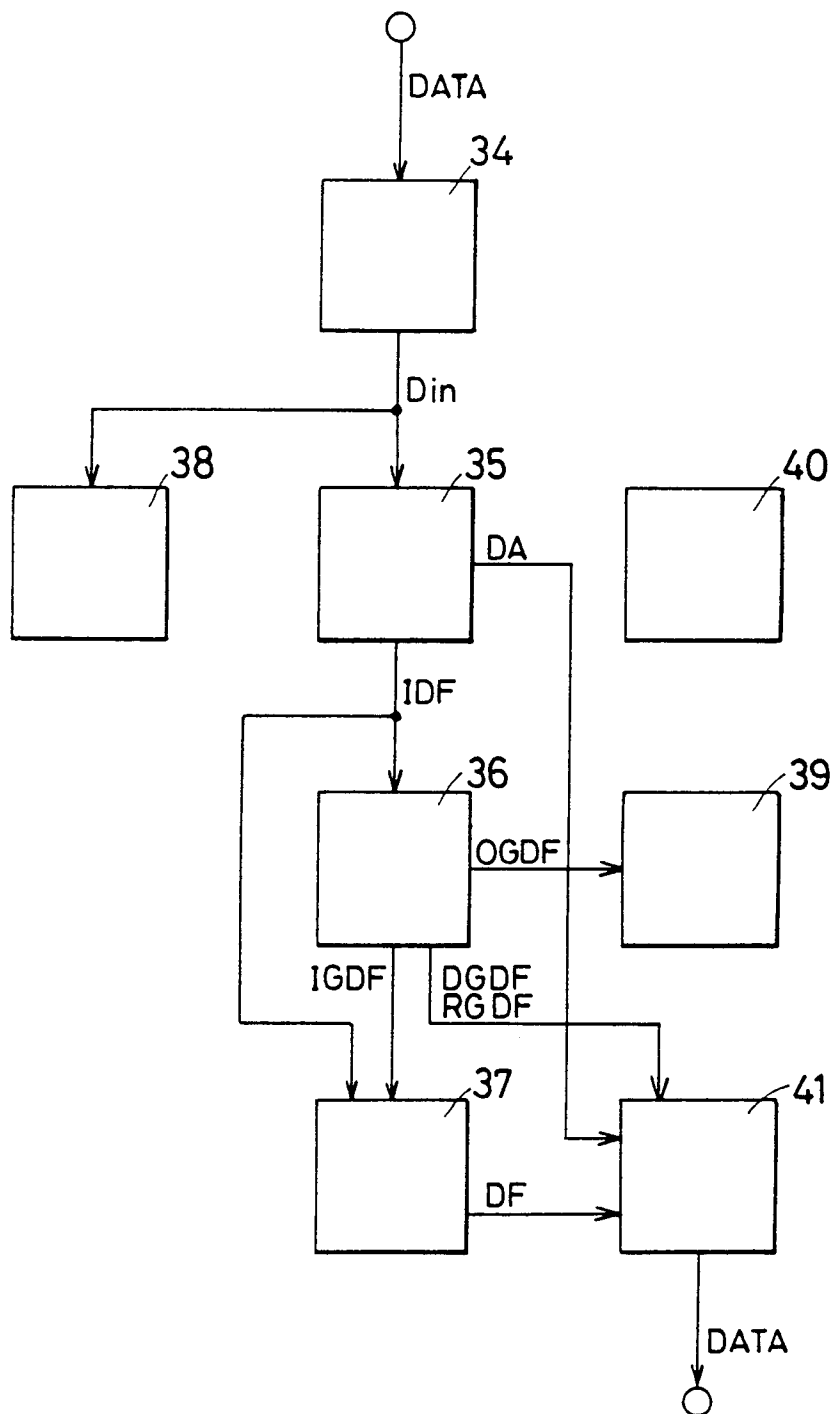


FIG. 36

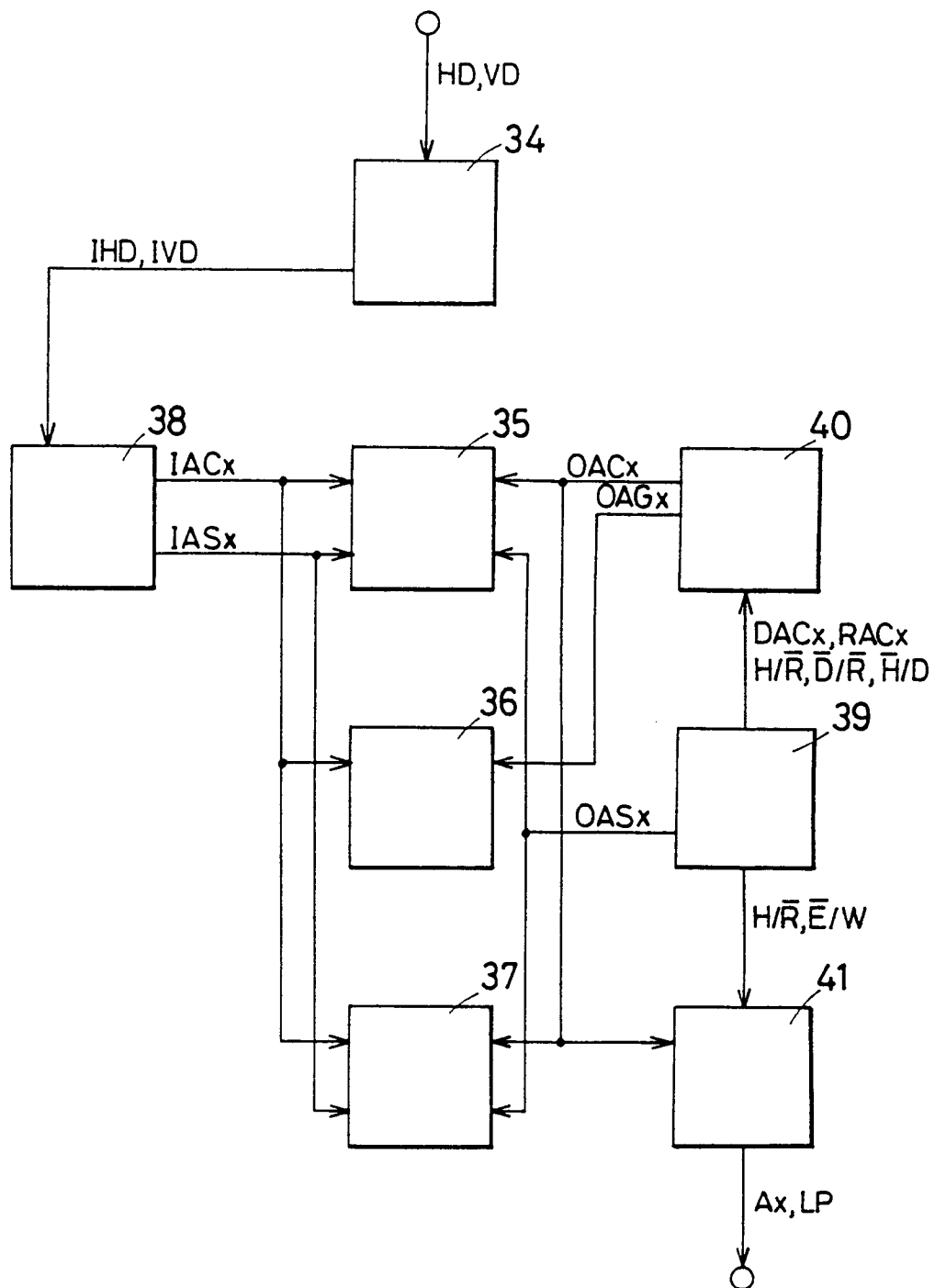


FIG. 37

	IGDF	OGDF	
0			
1			
2			
3			
4			
5			
6			
7			

FIG. 38

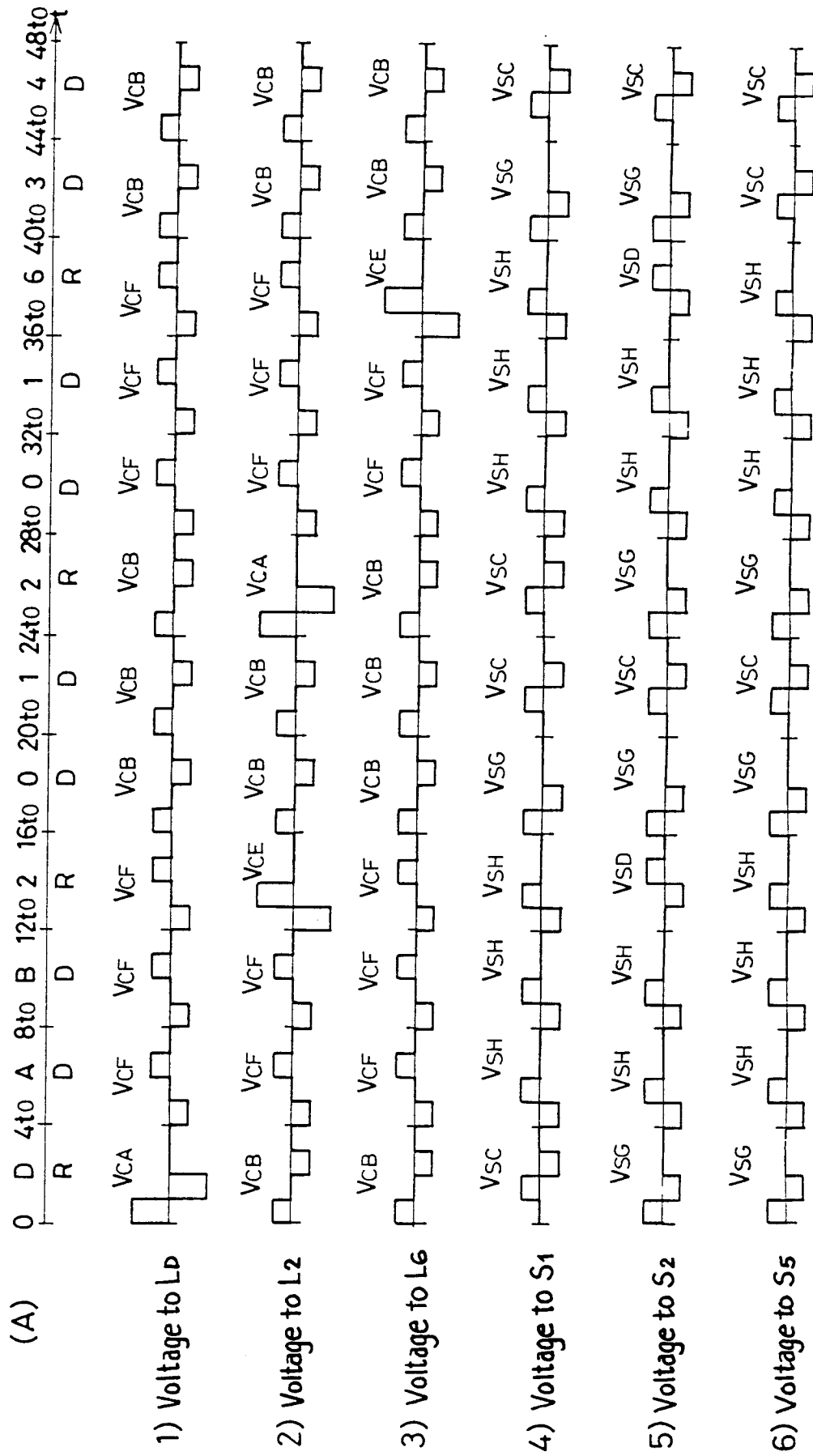


FIG. 39

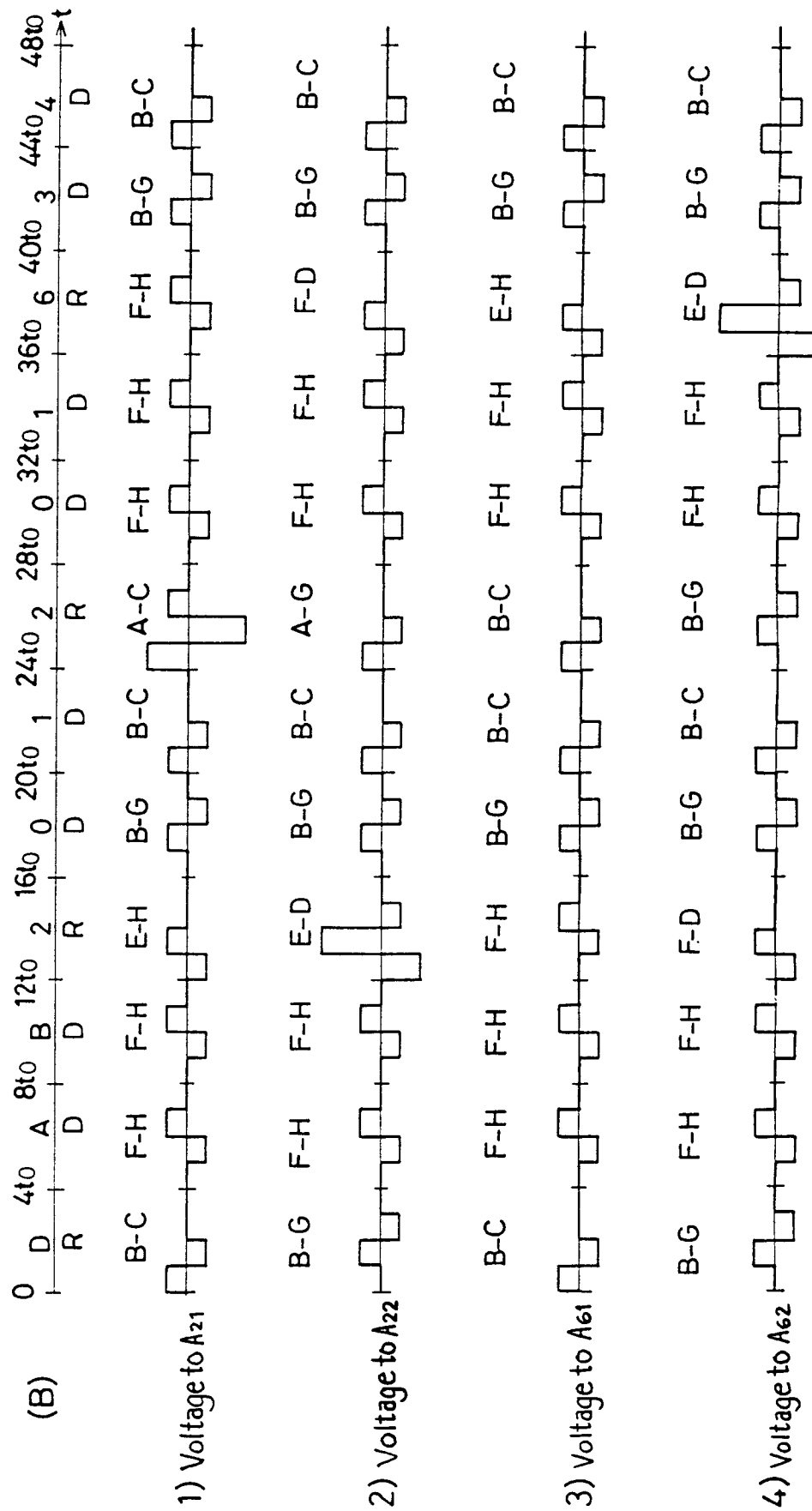


FIG. 40

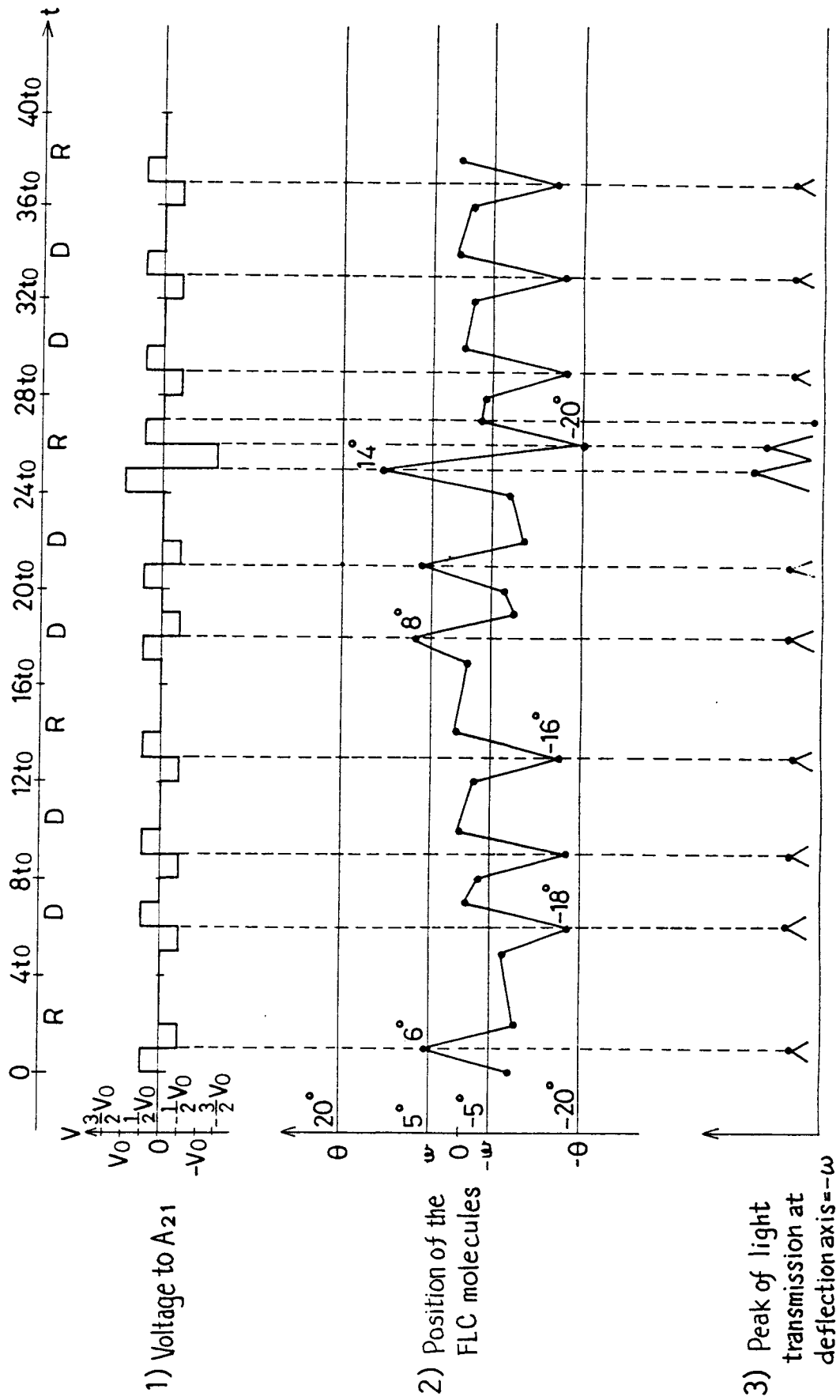


FIG. 41

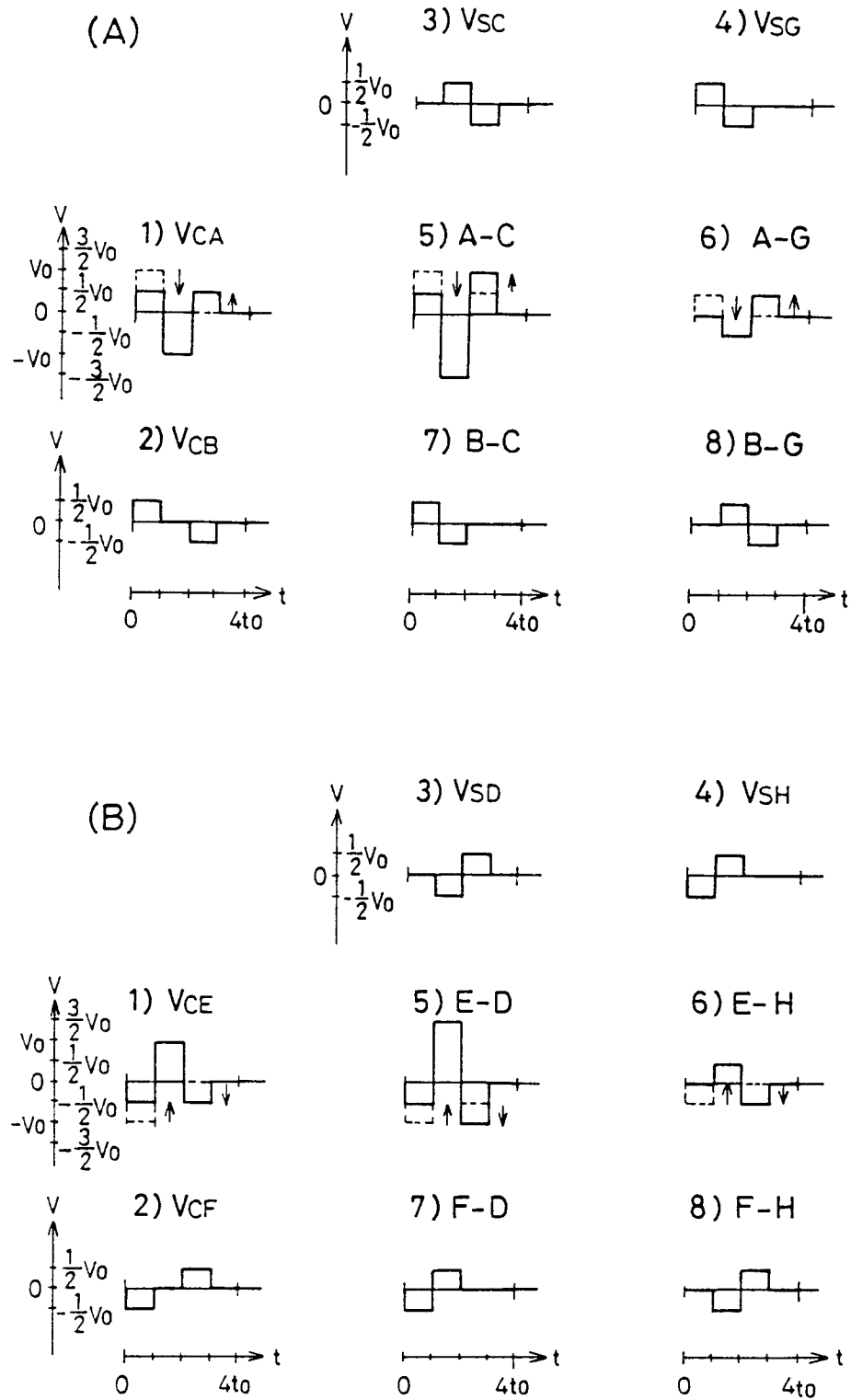


FIG. 42

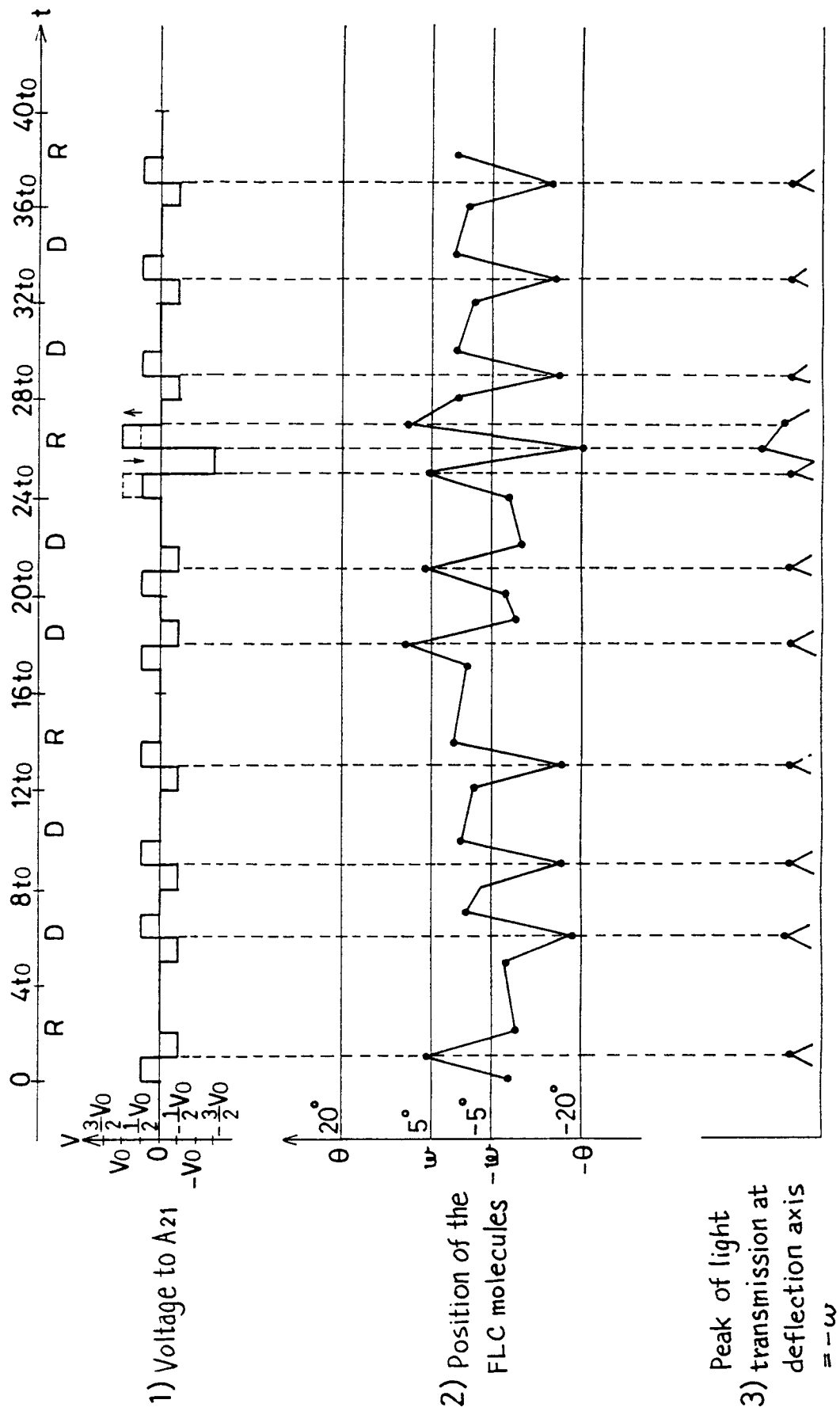


FIG. 43

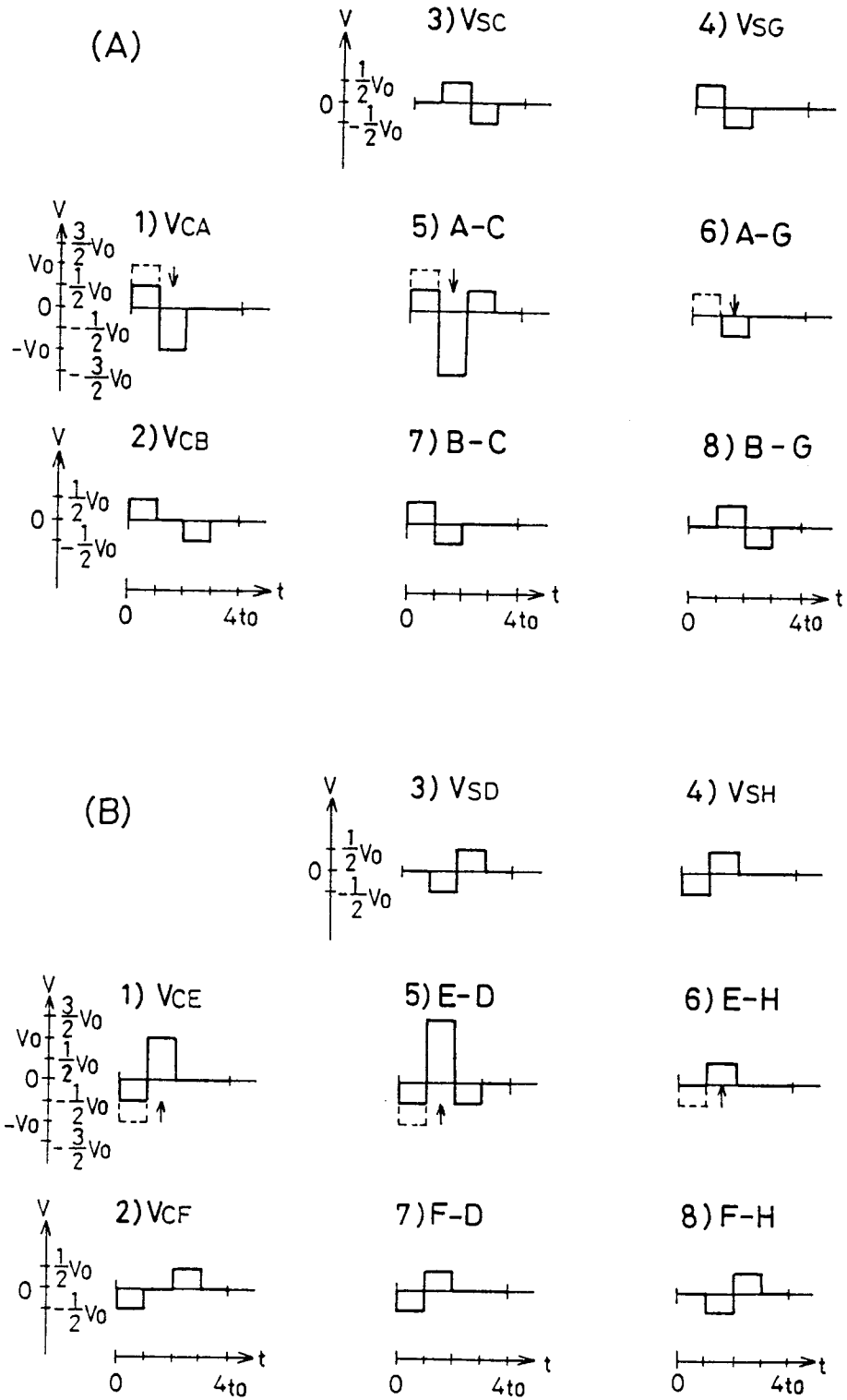
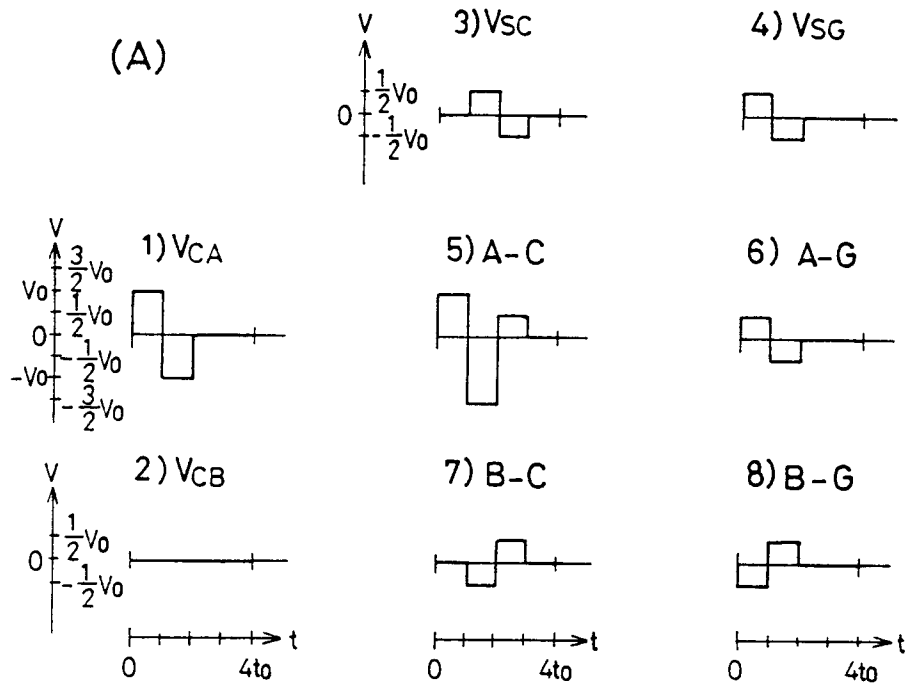


FIG. 44

(A)



(B)

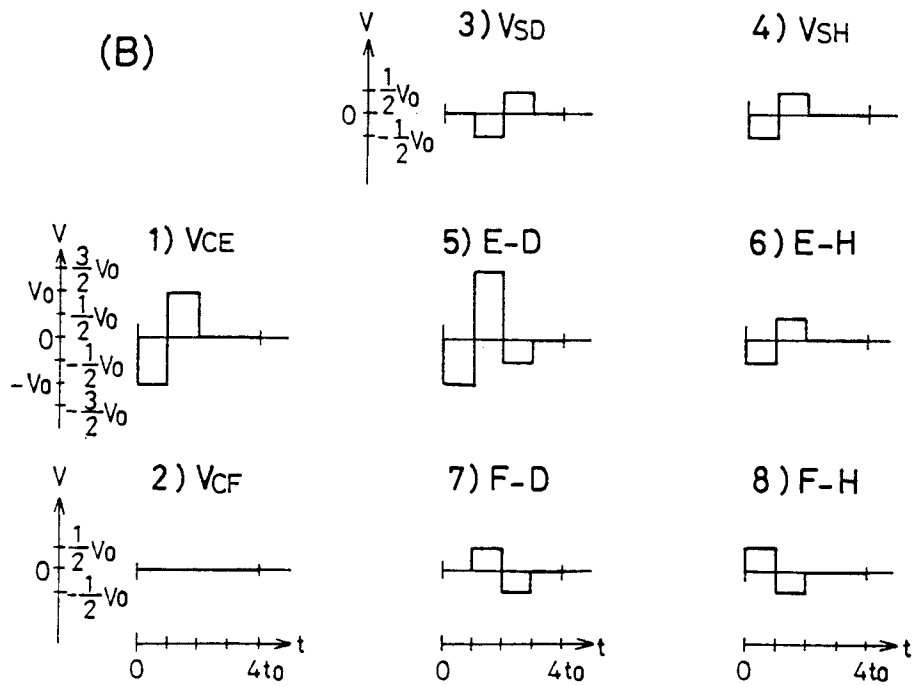


FIG. 45

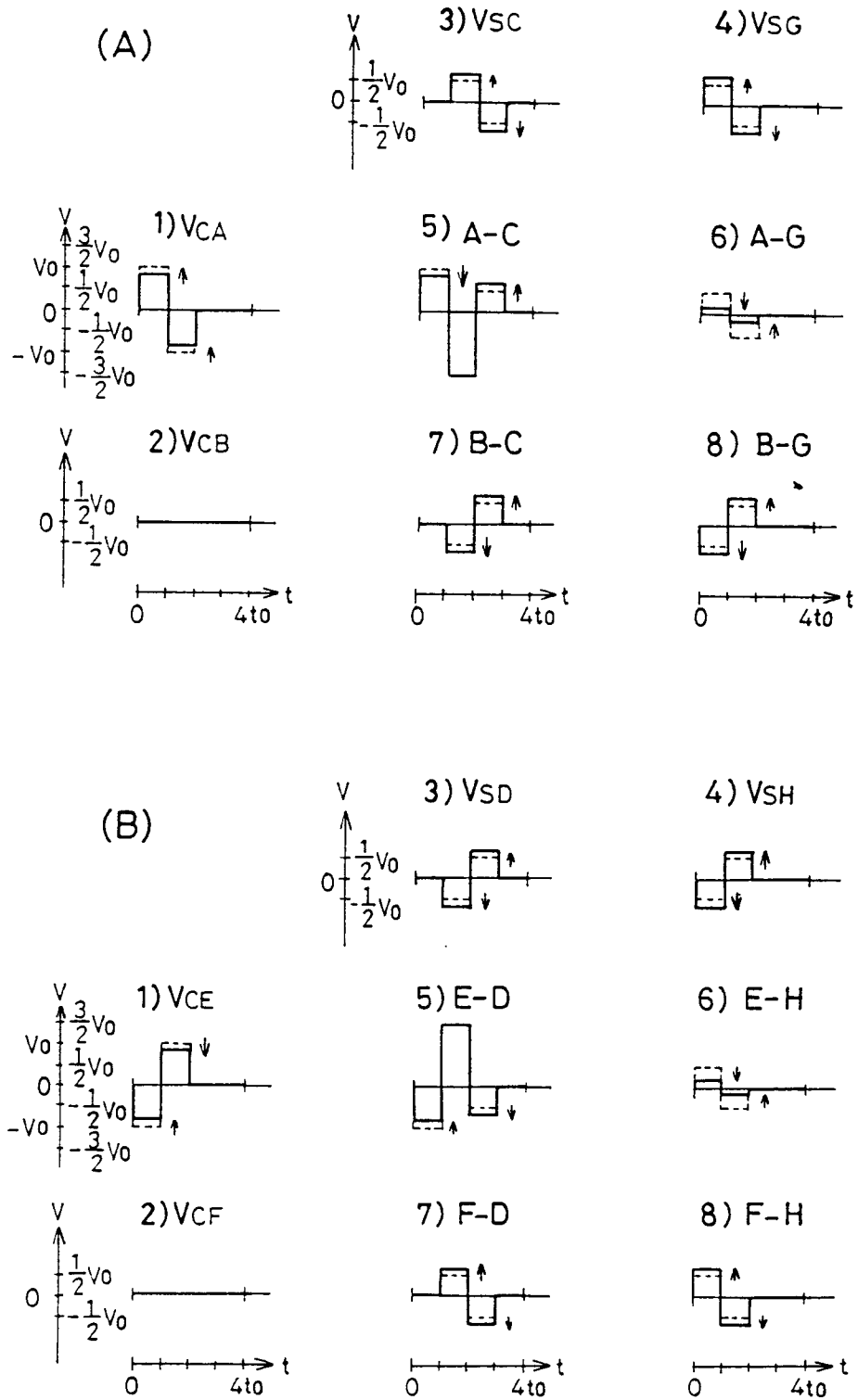


FIG. 46

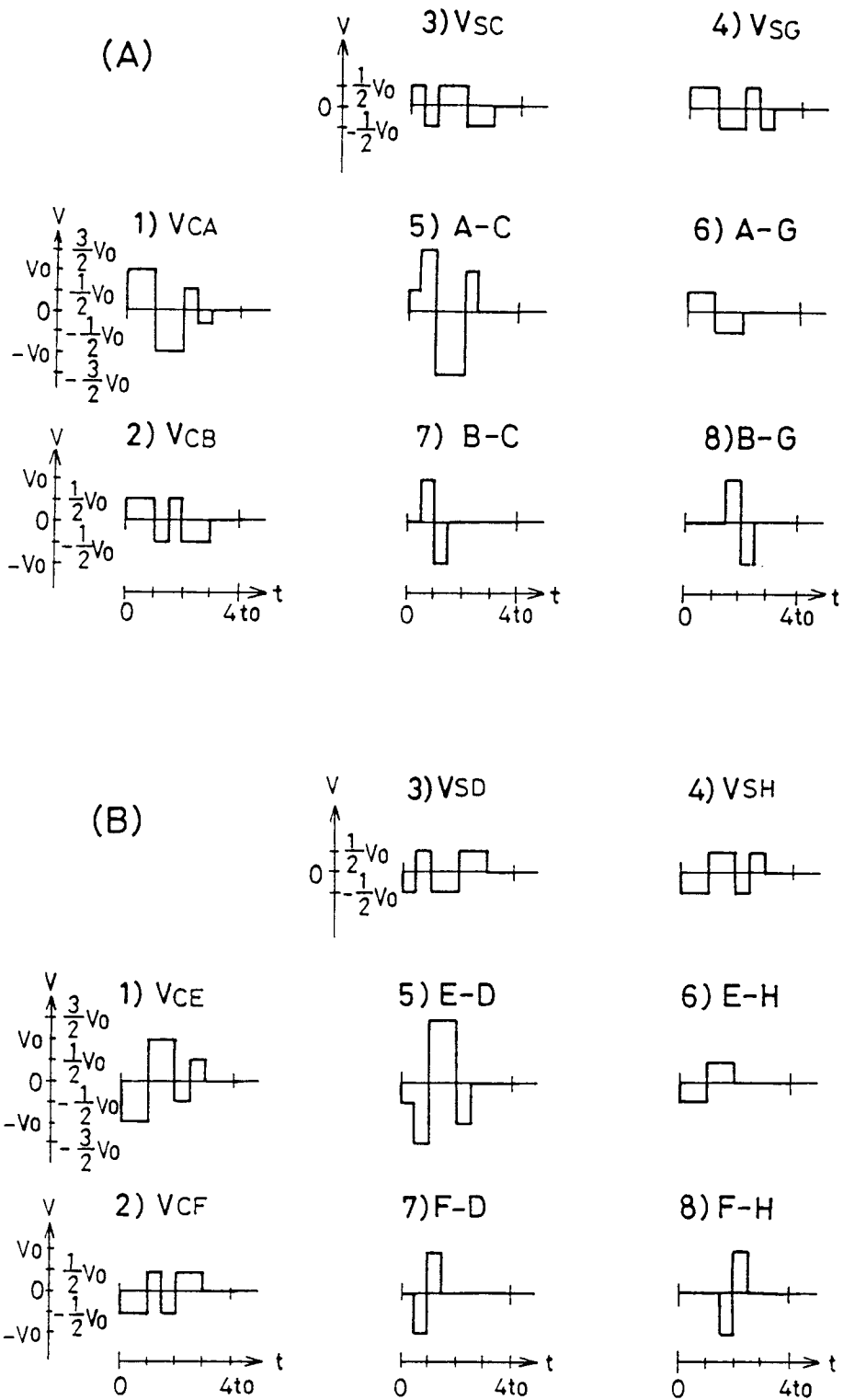


FIG. 47

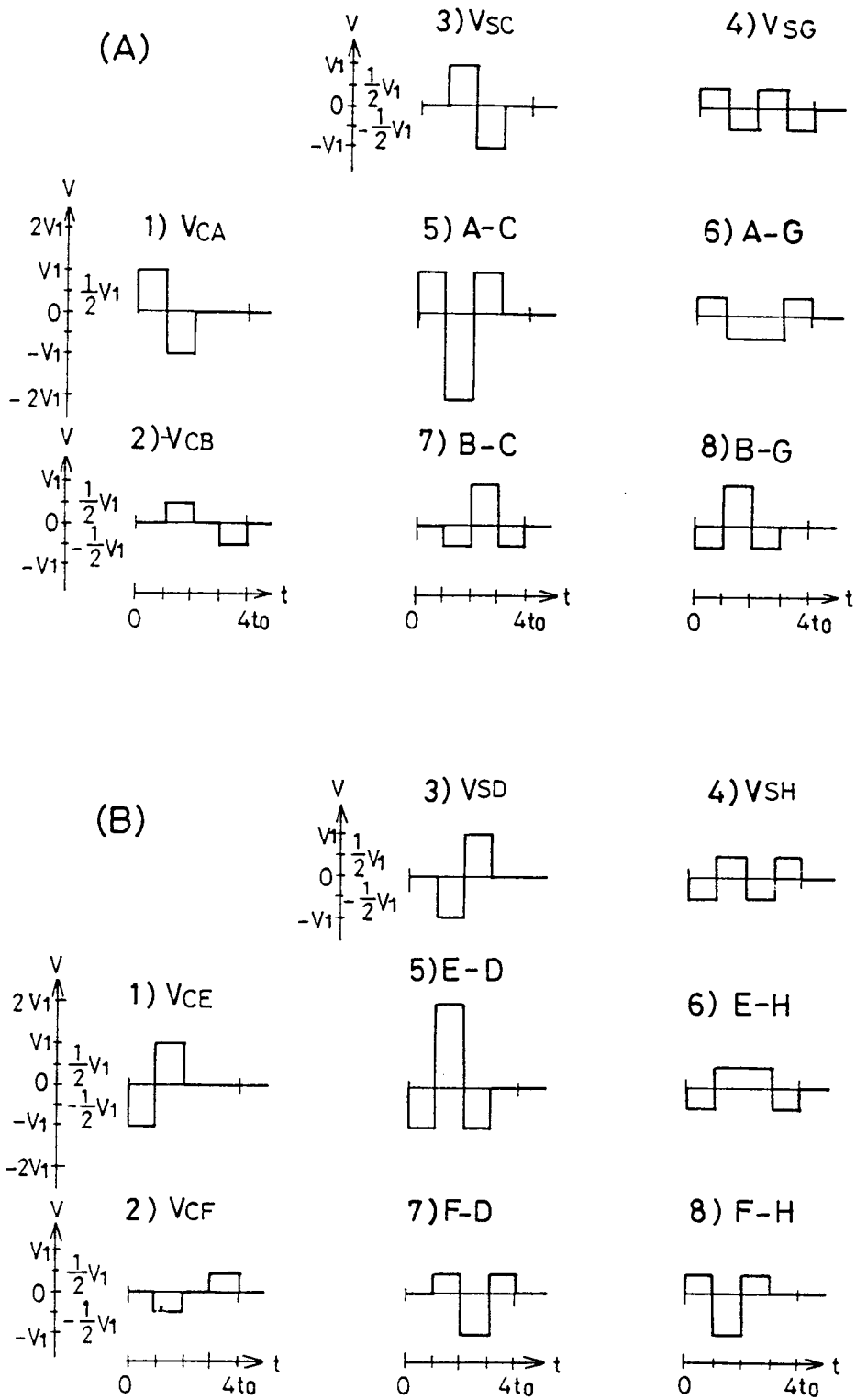


FIG. 48

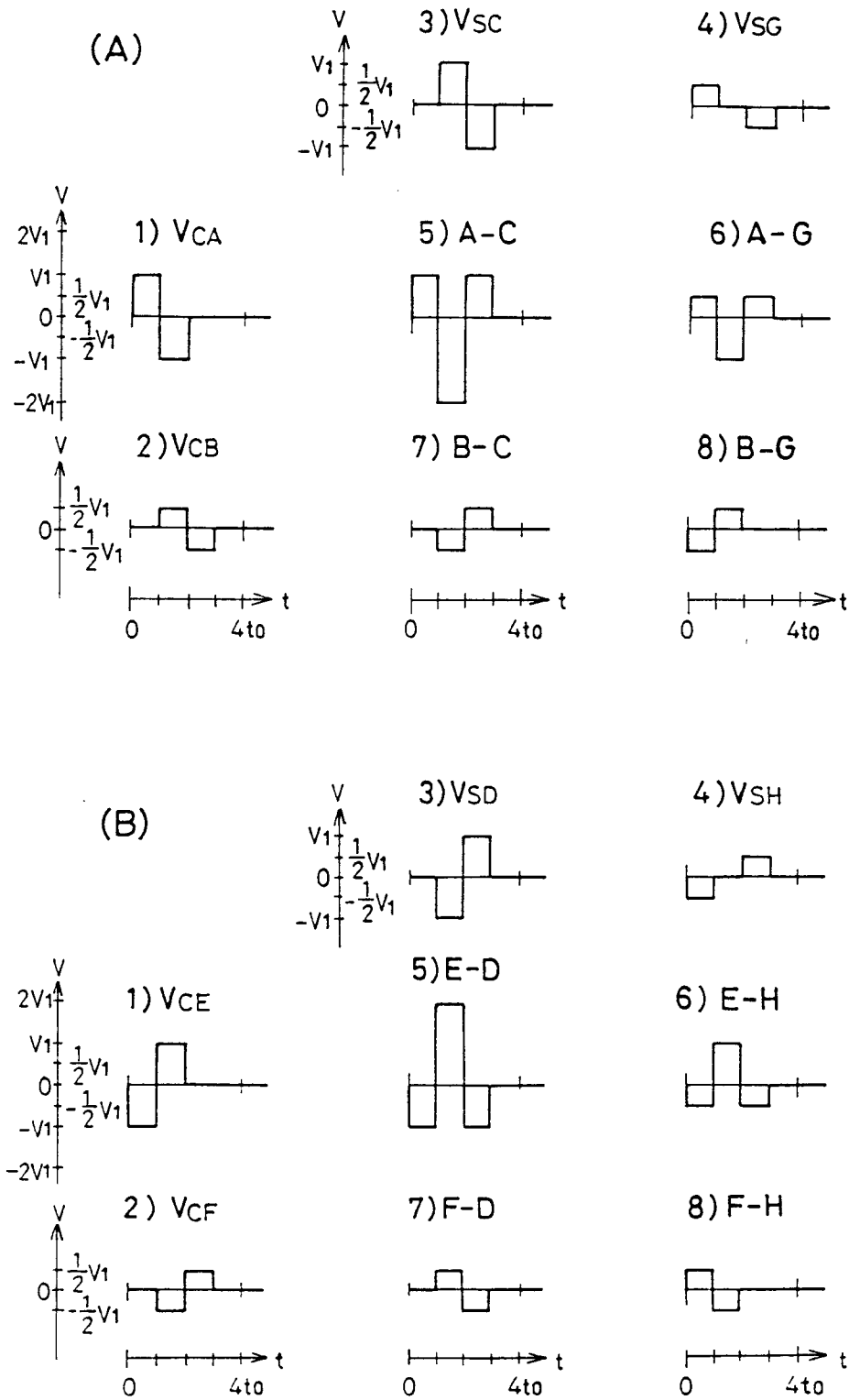


FIG. 49

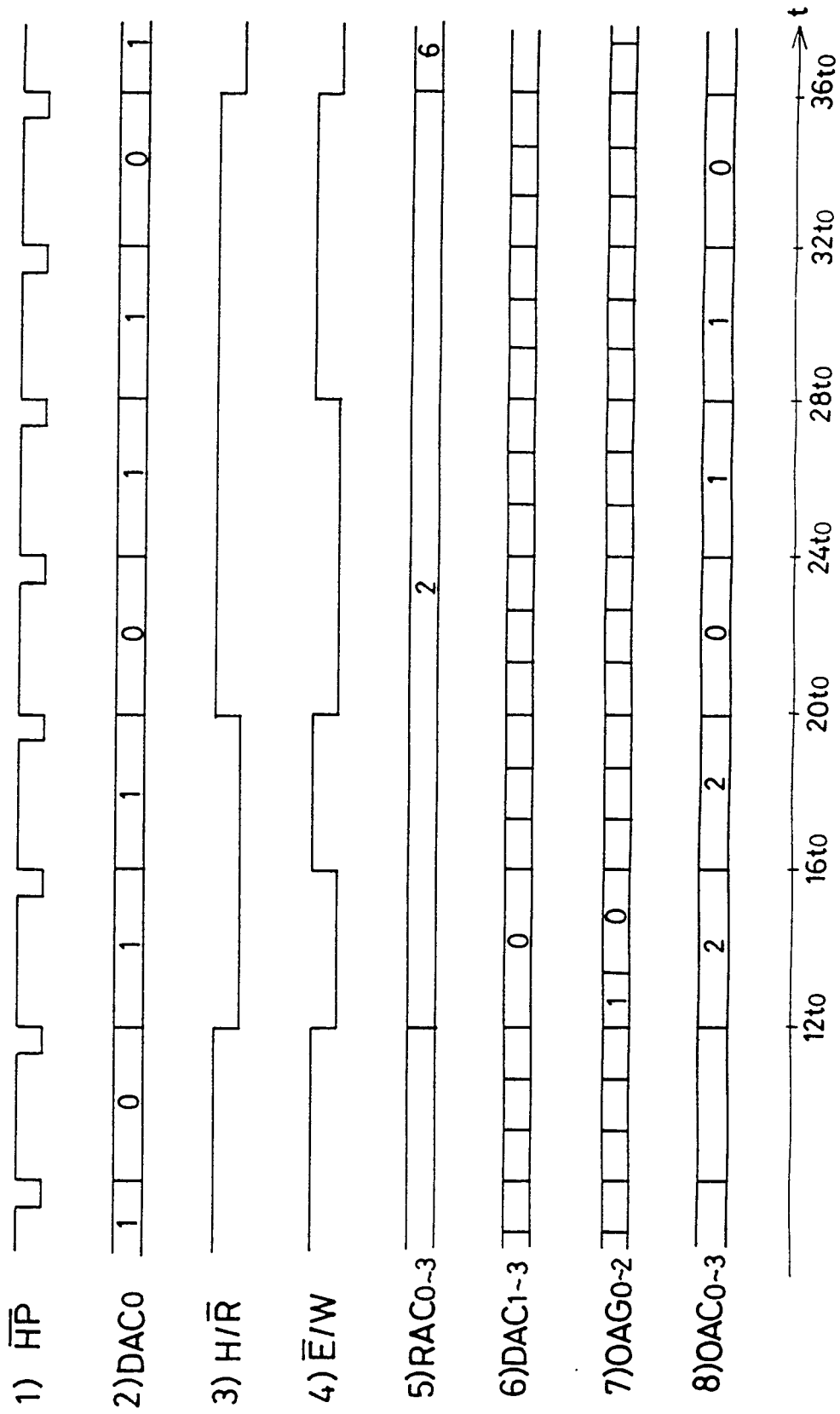


FIG. 50

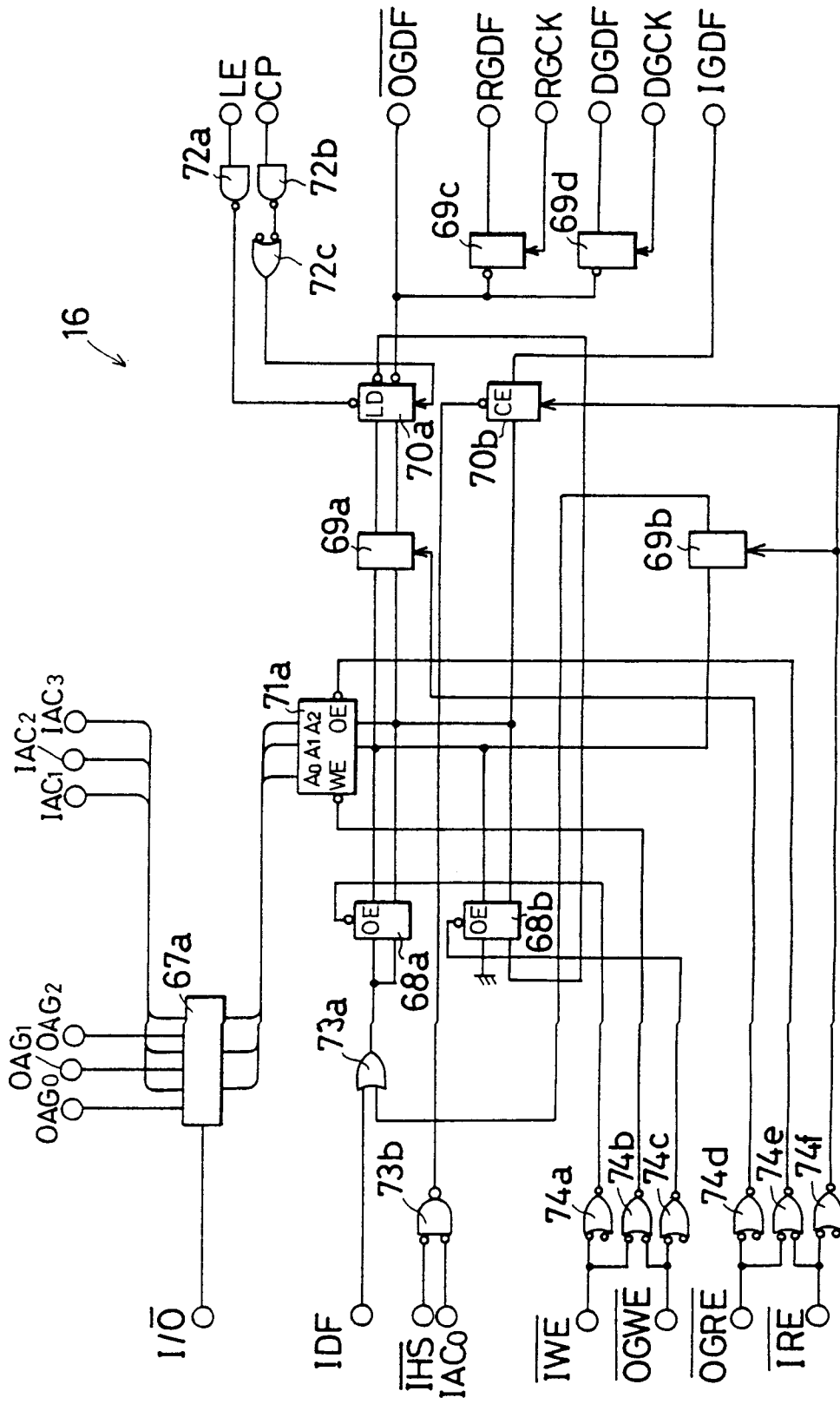


FIG. 51

