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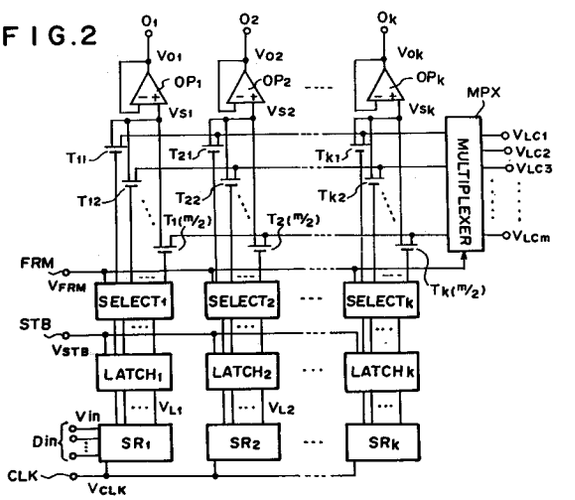
(54) **Driver circuit for liquid crystal display.**

(57) A driver circuit for a liquid crystal display comprises a multiplexer (MPX) which selectively outputs m/2 kinds of drive source voltages among m kinds of different drive source voltages ($V_{LC1}$ ~ $V_{LC\overline{m}}$), necessary for m/2 display gradations, according to a frame selection signal ($V_{FRM}$) supplied from a frame selection terminal (FRM). The number of transistor switches ($T_{11}$ ~ $T_{k(m/2)}$) which are divided into a plurality of switch groups can thus be reduced to one half that in the conventional LCD driver circuit. The LCD driver circuit comprises operational amplifiers ($OP_1$ ~ $OP_k$) each arranged between each of the switch groups and the liquid crystal display, which supply LCD drive voltages ($VO_1$ ~ $VO_k$) of high drive current capacity to the liquid crystal display according to the drive source voltages supplied via the transistor switches. As no large current flows through each of the transistor switches, it is possible to reduce the transistor size. The LCD driver circuit of the invention is suited to the LCD requiring a number of display gradations and permits high density integration and cost reduction.

FIG.2

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## BACKGROUND OF THE INVENTION

(1) Field of the invention:

The present invention relates to a driver circuit for a liquid crystal display (hereinafter referred to as an "LCD") which requires a number of display gradations.

(2) Description of the related art:

Fig. 1 is a block diagram showing a conventional driver circuit for a liquid crystal display. This LCD driver circuit comprises k (k being 2 or a greater integer) shift registers $SR_1$ ~ $SR_k$, k latch circuits $LATCH_1$ ~ $LATCH_k$, k select circuits $SELECT_1$ ~ $SELECT_k$ and a transistor switch group 2.

Digital image data input voltages $V_{in}$ inputted to image data input terminals $D_{in}$ are supplied to the shift registers $SR_1$ ~ $SR_k$, to which a clock pulse $V_{CLK}$ is also supplied commonly from a clock pulse input terminal CLK.

The outputs of the shift registers $SR_1$ ~ $SR_k$ are supplied to the corresponding latch circuits $LATCH_1$ ~ $LATCH_k$, to which a latch pulse $V_{STB}$ is also supplied commonly from a latch pulse input terminal STB.

The outputs of the latch circuits $LATCH_1$ ~ $LATCH_k$ are supplied to the corresponding select circuits $SELECT_1$ ~ $SELECT_k$, to which a frame selection signal $V_{FRM}$ is also supplied commonly from a frame selection terminal FRM. Each of the select circuits $SELECT_1$ ~ $SELECT_k$ has a plurality of output terminals and provides a switch selection signal at a specific output terminal based on the frame selection signal $V_{FRM}$ and also the outputs of the corresponding latch circuit $LATCH_1$ ~ $LATCH_k$.

The transistor switch group 2 comprises a plurality of transistors $T_{11}$ ~ $T_{km}$ in a matrix form. More specifically, the switch group 2 comprises k - (k being 2 or a greater integer) transistor groups, each group comprising m (m being 2 or a greater integer) transistors. These transistors $T_{11}$ ~ $T_{km}$ are on/off operated according to the switch selection signals outputted from the respective select circuits $SELECT_1$ ~ $SELECT_k$, and thus they selectively provide LCD driving voltage: $V_{LC1}$ ~ $V_{LCm}$ to the output terminals $O_1$ ~ $O_k$.

The operation of the conventional LCD driver circuit having the above circuit configuration is as follows.

From the image data input terminals $D_{in}$ are supplied the digital image input voltages $V_{in}$ of n (n being 2 or a greater integer) bits corresponding to the m gradations. The image data input voltages $V_{in}$ are transferred to the k shift registers $SR_1$ ~ $SR_k$ in synchronism with the clock pulse $V_{CLK}$ supplied to the clock pulse input terminal CLK.

Data having been transferred to the shift registers $SR_1$ ~ $SR_k$ are transferred to the corresponding latch circuits $LATCH_1$ ~ $LATCH_k$ in synchronism with the latch pulse $V_{STB}$ supplied to the latch pulse input terminal STB.

Each of the select circuits $SELECT_1$ ~ $SELECT_k$ outputs a switch selection signal according to the frame selection signal $V_{FRM}$ and the data held in the corresponding latch circuit $LATCH_1$ ~ $LATCH_k$, thus selectively turning on a specific transistor in each of the transistors groups $T_{11}$ ~ $T_{1m}$, ..., $T_{k1}$ ~ $T_{km}$. Thus, one of the voltages $V_{LC1}$ ~ $V_{LCm}$ is selectively provided to each of the output terminals $O_1$ ~ $O_k$. In this way, the voltages corresponding to the m gradations are supplied to the LCD.

The conventional LCD driver circuit explained above has the following defects. Where there are many gradations for display on the LCD, it is necessary for the conventional driver circuit that a low impedance buffer circuit having output terminals corresponding in number to the number of gradations is formed on a semiconductor chip. Therefore, if the number of gradations is to be increased, the chip size and the cost of manufacture of the conventional LCD driver circuit are inevitably increased.

## SUMMARY OF THE INVENTION

It is, therefor, an object of the invention to overcome the defects in the conventional LCD driver circuit and to provide an improved LCD driver circuit which permits driving of an LCD in a large number of gradations and which permits high density integration to be realized readily and with a low cost.

To attain this object of the invention, there is provided a driver circuit for a liquid crystal display, the circuit comprises:

a plurality of shift registers for transferring image input data in accordance with a clock pulse;

a plurality of latch circuits for receiving and holding respectively the outputs from the shift registers in accordance with a latch pulse;

a plurality of select circuits each having a plurality of output terminals, each for outputting a switch selection signal to a specific one of the output terminals based on outputs from each of the latch circuits and a frame selection signal;

a multiplexer for receiving m (m being 2 or a greater integer) kinds of drive source voltages whose levels are different from one another and selectively outputting m/2 kinds of drive source voltages based on the frame selection signal;

a plurality of switch groups each having transistor switches for selecting the outputs of the multiplexer based on each of the switch selection

signals outputted from the select circuits; and

a plurality of operational amplifiers each provided between each of the switch groups and the liquid crystal display.

According to the present invention, the multiplexer selectively outputs m/2 kinds of voltages among the m kinds of different LCD drive source voltages according to the frame selection signal, and the switch groups select specific ones of these LCD drive source voltages according to the switch selection signals outputted from the select circuits. Thus, the necessary number of the switches can be reduced to one half as compared to that in the conventional circuit, thus permitting high density integration and cost reduction.

In addition, the amplifiers provided between each of the switch groups and the LCD permit switch size reduction, because currents flowing through the switches do not directly drive the LCD. It is thus possible to permit higher density integration of the LCD driver circuit.

As the switches, MOS transistors, for example, may be used. In this case, if each switch is constructed with a single transistor, its "on" resistance is possibly changed by the voltages supplied from the multiplexer. This change in the "on" resistance of the single transistor switch can be avoided by using as the switch a transfer gate, which may be constructed, for example, with a P- and an N-channel transistor connected in parallel. Accordingly, it is desirable that the switch is a transfer gate constituted by a P-channel translator and an N-channel transistor.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention explained with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram showing a conventional LCD driver circuit;

Fig. 2 is a schematic diagram showing a first embodiment of the LCD driver circuit according to the invention;

Fig. 3 is a timing chart for illustrating the operation of the first embodiment of the LCD driver circuit shown in Fig, 2; and

Fig. 4 is a schematic diagram showing a second embodiment of the LCD driver circuit according to the invention.

## PREFERRED EMBODIMENTS OF THE INVENTION

Now, preferred embodiments of the invention will be explained with reference to the accompanying drawings. It should be noted that the elements showing the same or like elements in Fig. 1 are indicated with the same reference numerals or symbols in Figs. 2 to 4.

Fig. 2 is a schematic diagram showing a first embodiment of the LCD driver circuit according to the invention.

This LCD driver circuit comprises a plurality of shift registers $SR_1 \sim SR_k$, latch circuits $LATCH_1 \sim LATCH_k$.select circuits $SELECT_1 \sim SELECT_k$, transistor switches $T_{11} \sim T_{k(m/2)}$, a multiplexer MPX, and a plurality of operational amplifiers $OP_1 \sim OP_k$.

In the same manner as in the prior art, the image data input voltages $V_{in}$ inputted to the image data input terminals $D_{in}$ are transferred to the k shift registers $SR_1 \sim SR_k$ in synchronism with the clock pulse $V_{CLK}$ supplied from the clock pulse input terminal CLK. The latch circuits $LATCH_1 \sim LATCH_k$ hold the respective output signals of the shift registers $SR_1 \sim SR_k$ in synchronism with the latch pulse $V_{STB}$ supplied to the latch pulse input terminal STB. Each of the select circuits $SELECT_1 \sim SELECT_k$ has a plurality of output terminals and outputs a switch selection signal to a specific one of the output terminals based on the frame selection signal $V_{FRM}$ supplied from the frame selection terminal FRM and also the outputs of each of the latch circuits $LATCH_1 \sim LATCH_k$.

To the multiplexer MPX are supplied m kinds of different LCD drive source voltages $V_{LC1} \sim V_{LCm}$. It should be noted that the frame selection signal $V_{FRM}$ is supplied also to the multiplexer MPX. The multiplexer MPX selects m/2 kinds of LCD drive source voltages among the m kinds of different LCD drive source voltages $V_{LC1} \sim V_{LCm}$, necessary for m/2 levels of gradation display of image. The transistor switches $T_{11} \sim T_{k(m/2)}$ constitute k transistor switch groups each group consisting of m/2 transistor switches. These transistor switches are on/off operated by the switch selection signals outputted from the respective select circuits $SELECT_1 \sim SELECT_k$.

The operational amplifiers $OP_1 \sim OP_k$ each forming a voltage follower circuit enhance the drive current capacity of the LCD drive source voltages supplied through the transistor switches $T_{11} \sim T_{k(m/2)}$, and supply to the LCD with these enhanced LCD drive source voltages through the output terminals $O_1 \sim O_k$.

Fig. 3 is a timing chart for illustrating the operation of this embodiment of the LCD drive circuit shown in Fig. 2. The frame selection signal $V_{FRM}$ assumes a high and a low level at a predetermined period or frequency. The latch pulse signal $V_{STB}$ is generated in synchronism with the rising of the frame selection signal $V_{FRM}$.

First, the image data input voltages $V_{in}$ inputted to the image data input terminals $D_{in}$ are trans-

ferred to the shift registers $SR_1 \sim SR_k$ in synchronism with the clock pulse $V_{CLK}$. The latch circuits $LATCH_1 \sim LATCH_k$ receive signals outputted from the corresponding shift registers $SR_1 \sim SR_k$ in synchronism with the latch pulse $V_{STB}$ and hold these input signals as data for the next horizontal scan period.

The select circuits $SELECT_1 \sim SELECT_k$ selectively turn on specific transistor switches in the individual transistor switch groups of transistor switches $T_{11} \sim T_{k(m/2)}$ based on the frame selection signal $V_{FRM}$ and the n-bit data outputted from the latch circuits $LATCH_1 \sim LATCH_k$. The multiplexer MPX selectively outputs m/2 kinds of voltages among the m kinds of different drive source voltages $V_{LCl} \sim \overline{V}_{LCm}$ according to the frame selection signal $V_{FRM}$. These voltages are selectively supplied to the operational amplifiers $OP_1 \sim OP_k$ via the aforementioned specific transistor switches selected by the select circuits $SELECT_1 \sim SELECT_k$. The operational amplifiers $OP_1 \sim OP_k$ provide the output voltages $V_{O1} \sim V_{Ok}$ according to the input voltages $V_{S1} \sim V_{Sk}$.

In the conventional LCD driver circuit without any operational amplifiers, the drive current is small if the dimensions of the transistors constituting the transistor switches are small. To increase the drive current, it has been necessary to increase the dimensions of the switching transistors concerned. In the conventional LCD driver circuit, therefore, with an increase in the number of gradations, the number of transistor switches is correspondingly increased to increase the chip size. To the contrary, in this embodiment, the operational amplifiers $OP_1 \sim OP_k$ are provided as the voltage follower circuits between the transistor switches $T_{11} \sim T_{k(m/2)}$ and the LCD, and they provide drive voltages having large drive current capacity. Therefore, the transistors of the transistor switches $T_{11} \sim T_{k(m/2)}$ may be of smaller dimensions.

Thus, the LCD driver circuit in this embodiment may be of a reduced chip size as compared to that in the prior art.

Further, since the LCD driver circuit of the embodiment incorporates the multiplexer MPX, m gradations may be covered by m/2 transistor switches in each of the groups of transistor switches $T_{11} \sim T_{k(m/2)}$, that is, it is possible to reduce the number of transistors used to one half that in the prior art. It is thus possible to further reduce not only the chip size but also the manufacturing cost.

Fig. 4 is a schematic diagram showing a second embodiment of the LCD driver circuit according to the invention. This embodiment is different from the preceding first embodiment in that a transfer gate consisting of a P- and an N-channel transistor and an inverter is provided in stead of each transistor switch constituted by a single transistor. Since the remainder of the structure is basically the same as in the first embodiment, parts like those in Fig. 2 are designated by like reference symbols, and the explanation therefor is not repeated here.

More specifically, in this second embodiment, a plurality of transfer gates each comprising a P- and an N-channel transistor and an inverter are provided as the switching means.

In the first embodiment, in which each switch is constituted by a single transistor, the "on" resistance of the transistor concerned is changed or influenced by the voltages supplied from the multiplexer MPX due to the back gate voltage dependency of the transistor. To the contrary, in this embodiment, a transfer gate consisting of a P- and an N-channel transistor and an inverter is provided as a transistor switch. Thus, In the LCD driver circuit in this embodiment, the P- and N-channel transistors compensate with each other to avoid the change in the "on" resistance caused by the voltage applied thereto.

As has been described in the foregoing, according to the present invention, since the multiplexer receives m kinds of different LCD drive source voltages and $\overline{\text{and}}$ provides m/2 kinds of voltages according to the frame selection signal, only one half the number of switches are necessary as compared to the conventional driver circuit. Thus, the LCD driver circuit according to the invention is well suited to the LCD requiring a number of display gradations and permits high density integration and cost reduction. Further, since according to the invention the amplifiers are provided between the switch groups and the LCD, no large current passes through the switches. It is thus possible to reduce the switch dimension and permit higher density integration.

While the invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather then limitation and that changes within the purview of the appended claims may be made without departing from the true scope and spirit of the invention in its broader aspects.

## Claims

1. A driver circuit for a liquid crystal display having: a plurality of shift registers ($SR_1 \sim SR_k$) for transferring image input data ($V_{in}$) in accordance with a clock pulse ($V_{CLK}$); a plurality of latch circuits ($LATCH_1 \sim LATCH_k$) for receiving and holding respectively the outputs from said shift registers in accordance with a latch pulse ($V_{STB}$); and a plurality of select circuits ($SELECT_1 \sim SELECT_k$) each having a plurality

of output terminals, each for outputting a switch selection signal to a specific one of said output terminals based on outputs from each of said latch circuits and a frame selection signal ($V_{FRM}$), said driver circuit being characterized by comprising:

a multiplexer (MPX) for receiving m (m being 2 or a greater integer) kinds of drive source voltages ($V_{LC1} \sim V_{LCm}$) whose levels are different from one another and selectively outputting m/2 kinds of drive source voltages ($V_{S1} \sim V_{Sk}$) based on the frame selection signal;

a plurality of switch groups each having switches ($T \sim T_{k(m/2)}$) for selecting the outputs of said multiplexer based on each of said switch selection signals outputted from said select circuits; and

a plurality of amplifiers ($OP_1 \sim OP_k$) each provided between each of said switch groups and said liquid crystal display.

**2.** The driver circuit for a liquid crystal display according to claim 1, wherein each of said switches ($T_{11} \sim T_{k(m/2)}$) is a transfer gate having a P- and an N-channel MOS transistor and an inverter connected between gates of said P- and N-channel MOS transistors.

**3.** The driver circuit for a liquid crystal display according to claim 1, wherein each of said amplifiers ($OP_1 \sim OP_k$) is an operational amplifier whose output terminal and inverting input terminal are directly connected so as to operate as a voltage follower circuit.

FIG.1
PRIOR ART

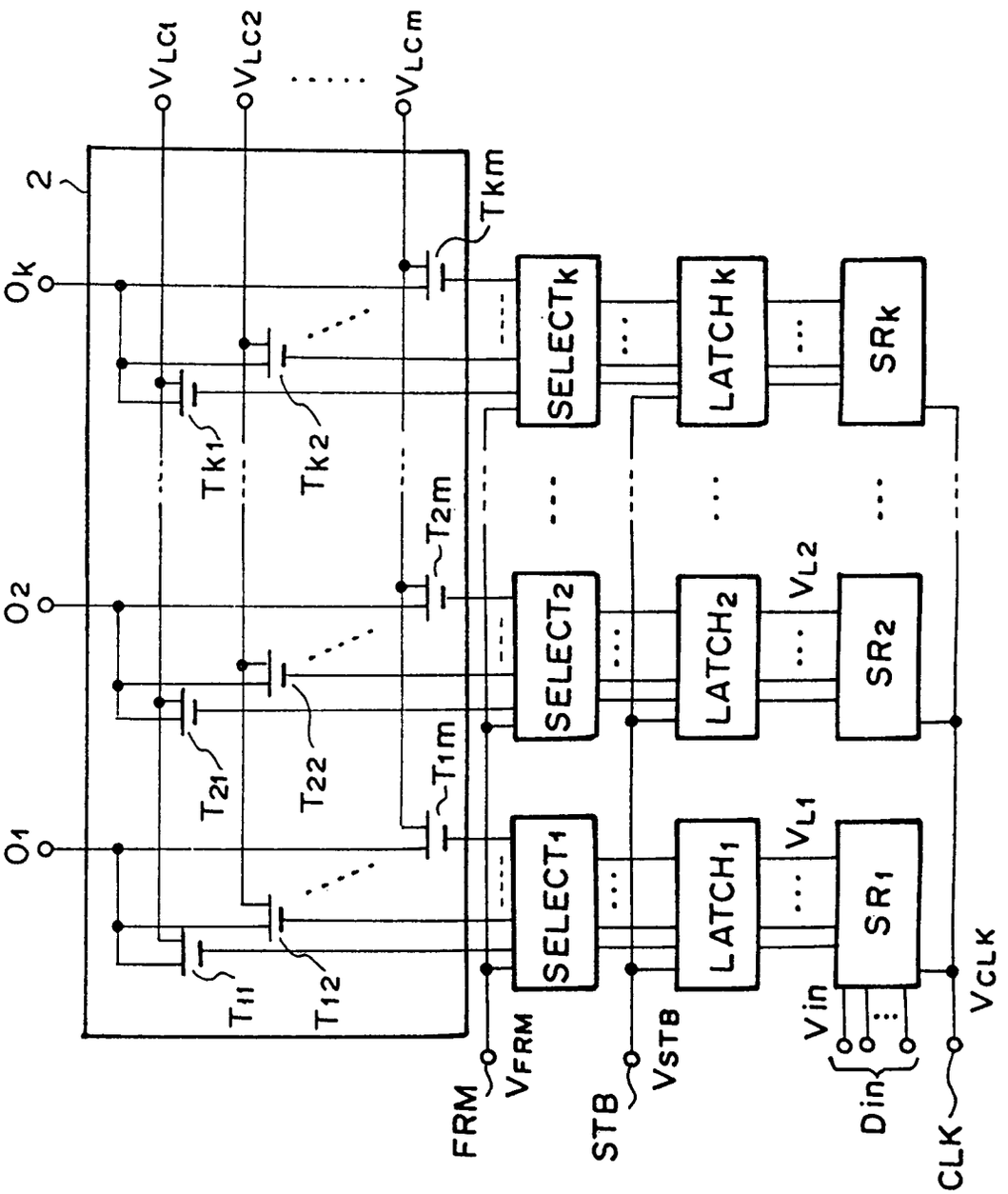
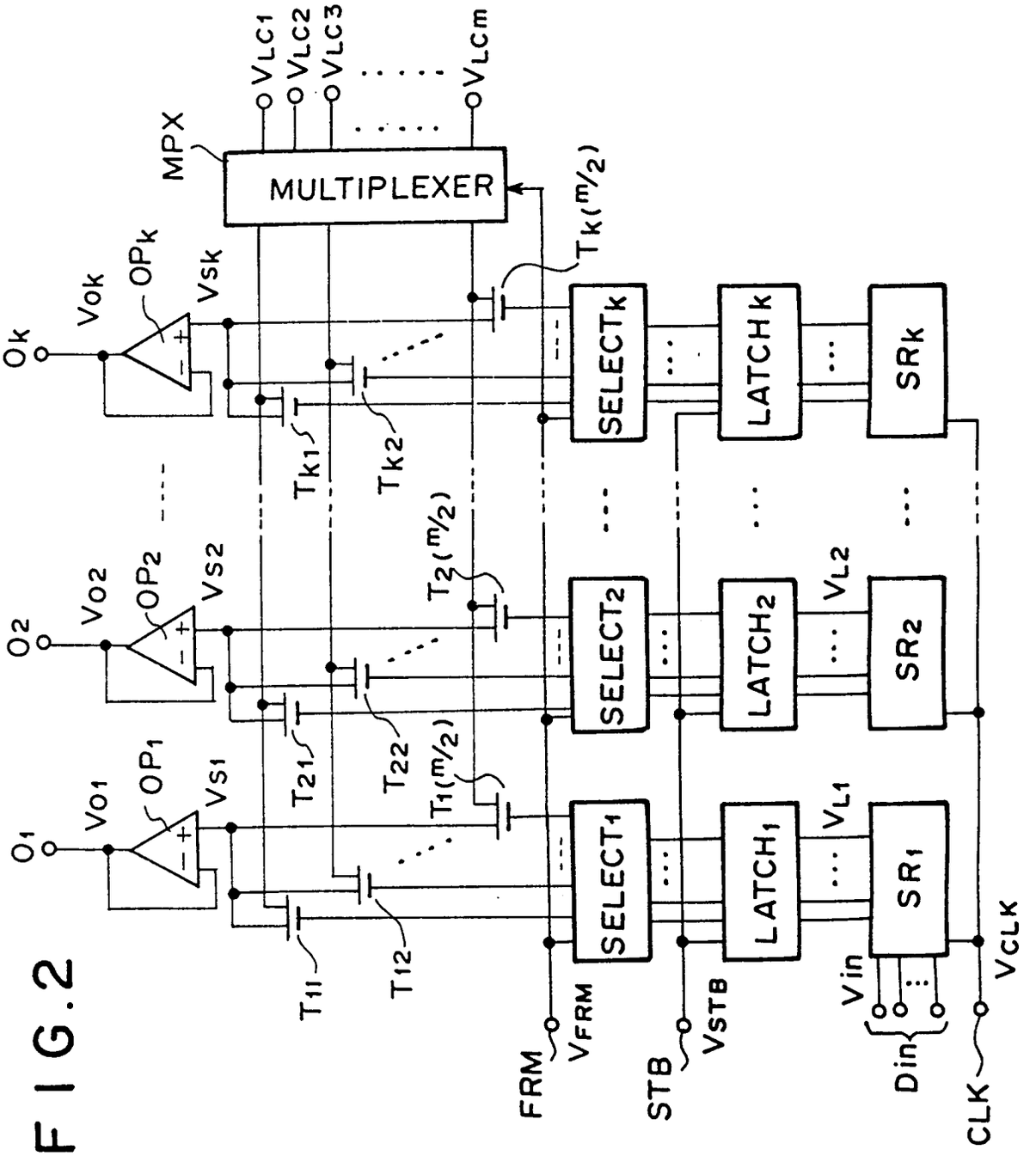


FIG.2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MULTIPLEXER
VLC1
VLC2
VLC3
VLCm
Ok
Vok
OPk
Vsk
O2
Vo2
OP2
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Vo1
OP1
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Tk2
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T21
T22
T2(m/2)
T11
T12
T1(m/2)
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LATCH2
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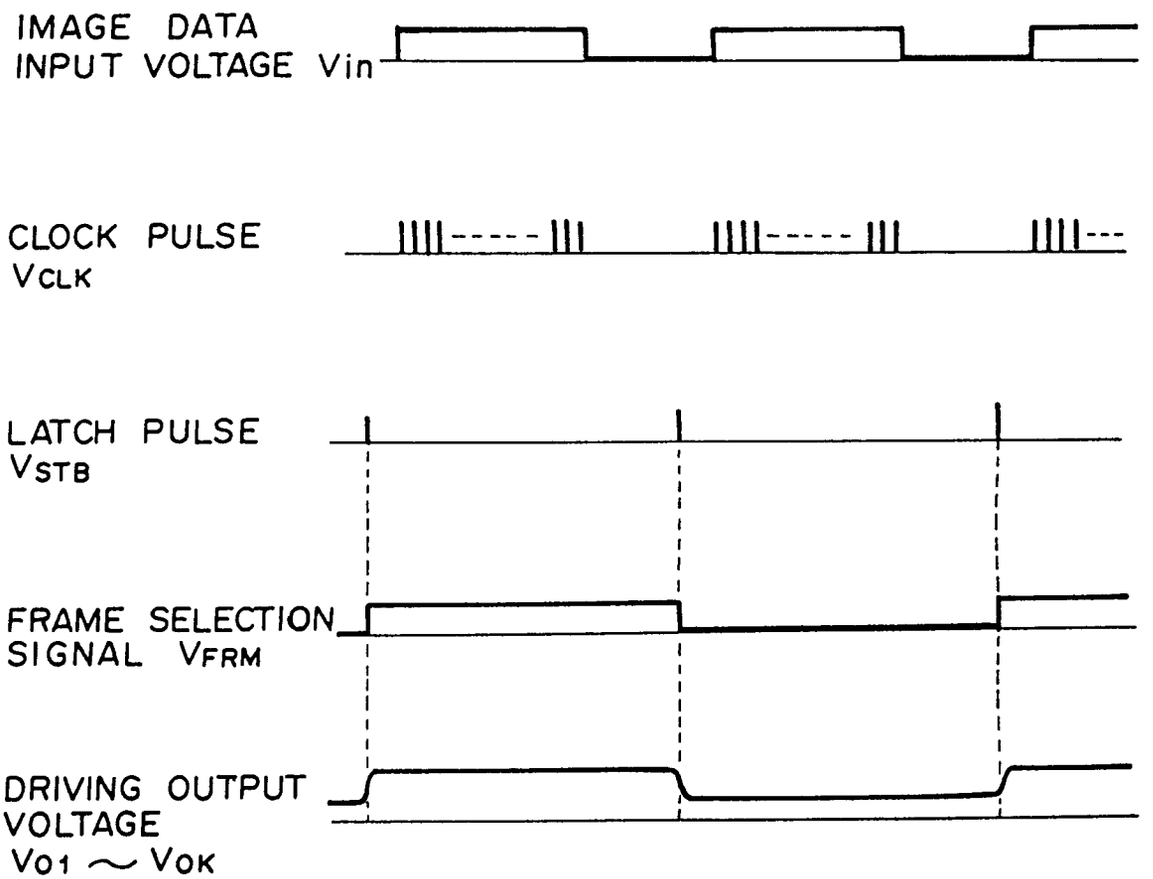
FRM
VFRM
STB
VSTB
Vin
Din
CLK
VCLK

FIG.3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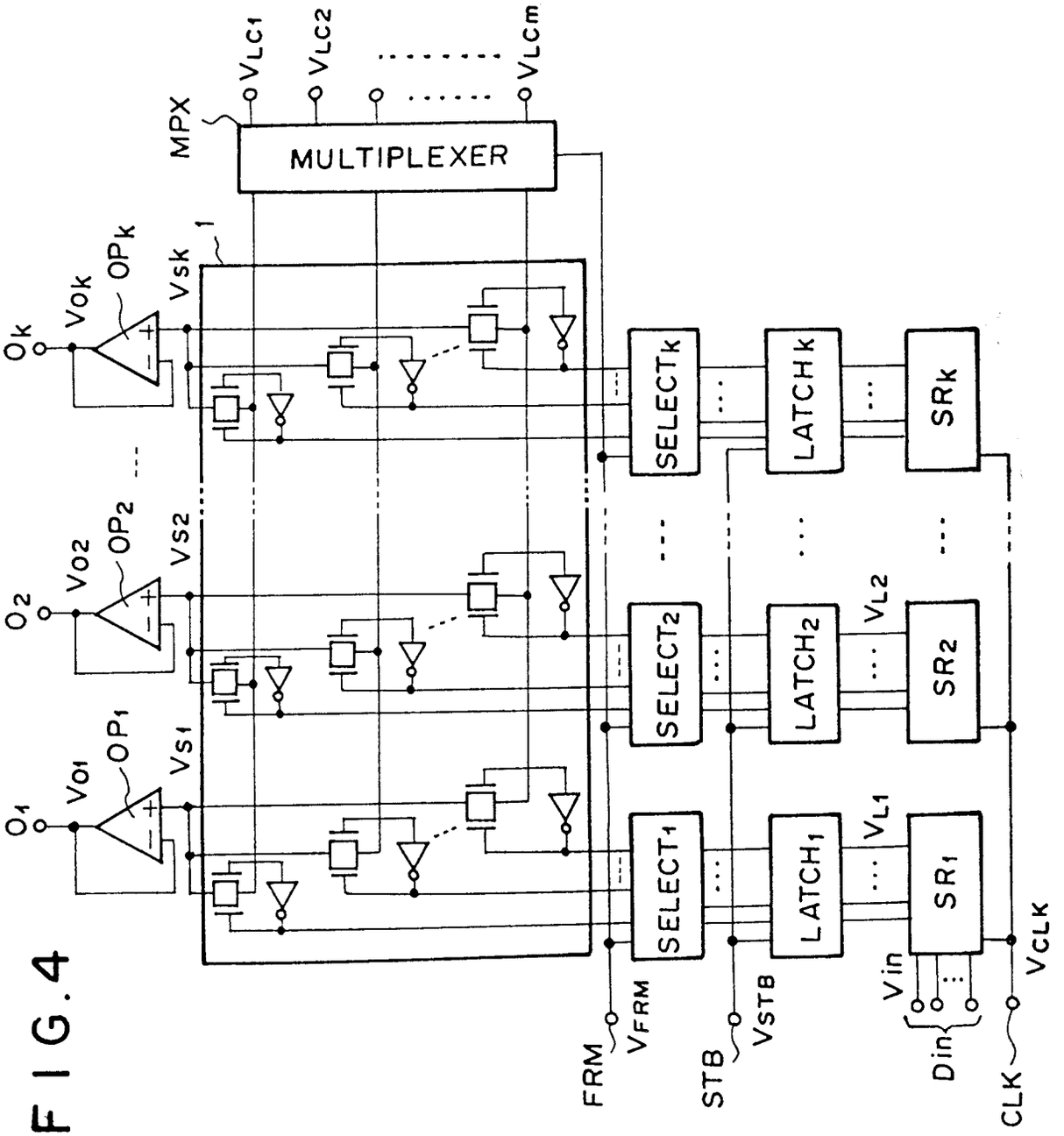
INPUT VOLTAGE Vin
CLOCK PULSE
VCLK
LATCH PULSE
VSTB
FRAME SELECTION
SIGNAL VFRM
DRIVING OUTPUT
VOLTAGE
Vo1 ~ VoK

FIG.4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MULTIPLEXER
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Vo1
OP1
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SR1
VL2
VL1
FRM
VFRM
STB
VSTB
Vin
Din
CLK
VCLK

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 91122321.2

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| A | EP - A - 0 238 867 (CANON) * Abstract * -- | 1 | G 09 G 3/36 |
| A | GB - A - 2 103 003 (SEIKOSHA) * Abstract * ---- | 1 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 02 F 1/00
G 09 G 3/00

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| VIENNA | 14-04-1992 | KUNZE |

CATEGORY OF CITED DOCUMENTS

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