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## (54) A radio pager producing stepwise increasing alert sound.

(57) A POCSAG compatible pager where the output of comparator (17) is a square waveform of fixed pulse repetition frequency and increasing in steps mark/space ratio.

The POCSAG alert tone modulates in an ON/OFF fashion the output of comparator (17) and this results in a sound level that escalates every 6 seconds.

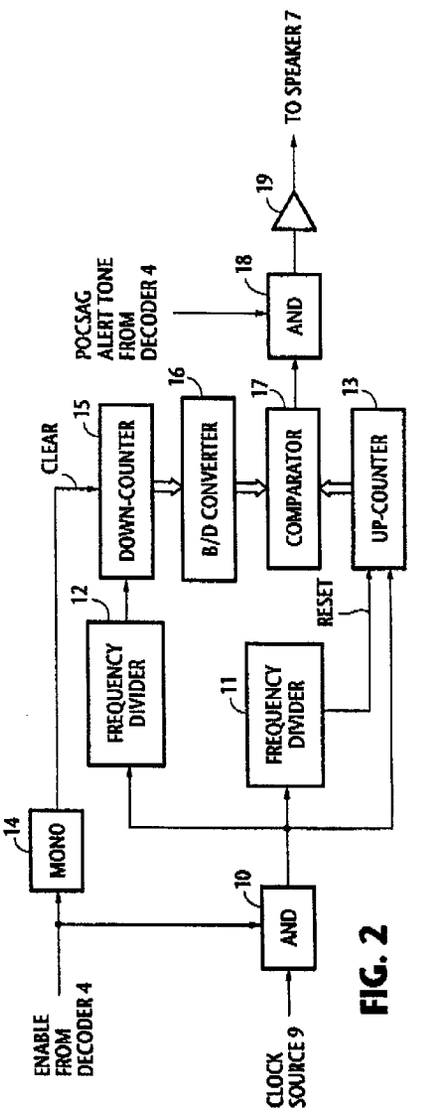


FIG. 2

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## BACKGROUND OF THE INVENTION

The present invention relates generally to radio pagers, and more specifically to a sound alarm circuit for such radio pagers which generates an alert tone of escalating sound levels.

A radio pager having the capability of successively escalating the sound level of an alert tone is described in japanese Patent Publication 63-252030 (Tokkaisho). According to the prior art technique, constant audio frequency pulses are modulated with a variable duty tone pattern that identifies particular incoming pages. The duty ratio of the tone pattern is successively increased to increase the sound level of the tone.

One serious disadvantage of the prior art technique is that since the sound level is controlled by the duty ratio of a tone pattern, the alert tone patterns as standardized by the Post Office Code Standardization Advisory Group (POCSAG) cannot be employed for escalating alert tones.

## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a radio pager that enables internationally standardized alert tone patterns to be employed for alerting users with an escalating sound level.

According to the present invention, the radio pager comprises a receiver for receiving a paging signal containing a unique identifier identifying the own radio pager and an alert tone pattern. A pulse generating circuit generates audio-frequency pulses having a duty ratio increasing as a function of time in response to receipt of the paging signal. A modulating means is provided for modulating the variable duty pulses with the alert tone pattern for applying the modulated pulses to a loudspeaker.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a radio pager of the present invention;

Fig. 2 is a block diagram of a sound alarm circuit of this invention;

Fig. 3 is a waveform diagram associated with the sound alarm circuit of Fig. 2;

Fig. 4 is a waveform diagram of the tone pulses modulated with a POCSAG A-code tone pattern;

Fig. 5 is a block diagram of a modified form of the sound alarm circuit;

Fig. 6 is a waveform diagram associated with the sound alarm circuit of Fig. 5;

Fig. 7 is a block diagram of an alternative form of the sound alarm circuit; and

Fig. 8 is a waveform diagram associated with the sound alarm circuit of Fig. 7.

## DETAILED DESCRIPTION

A radio pager of the present invention as represented in Fig. 1 comprises a front end 2 for converting paging signals received by antenna 1 to baseband signals for coupling to a waveshaper 3. The output of waveshaper 3 is applied to a decoder 4 in which the received signal is checked for a coincidence between a pager identifier contained in it and the one stored in a PROM (programmable read only memory) 5. On detecting a coincidence, decoder 4 alerts a sound alarm circuit 6 with a POCSAG (Post Office Code Standardization Advisory Group) alert tone signal having one of predetermined tone patterns or cadences. For example, one such cadence is a cyclic sequence of 7/8-second ON and 1/8-second OFF. Sound alarm circuit 6 modulates the tone signal with a variable duty pulse sequence and activates a loudspeaker 7. A reset switch 8 is connected to the decoder 4 to be operated when the user answers an incoming page.

As shown in Fig. 2, sound alarm circuit 6 comprises an AND gate 10 that is responsive to an enable signal from decoder 4 to pass high-frequency clock pulses from a clock source 9 to frequency dividers 11 and 12, and further to an up-counter 13 during the time the pager is being alerted. As shown in Fig. 3, frequency divider 11 divides the frequency of the clock to produce an output whose frequency determines the pitch of the alert tone, typically at 2.6 kHz, and frequency divider 12 divides that clock frequency so that its output determines the rate at which the duty ratio of the 2.6-kHz pulse sequence is varied. Typically, the duty ratio is stepwisely varied at 6-second intervals. The output of frequency divider 11 is applied to the up-counter 13 as a reset pulse so that its output represents a digital count value which continuously increments in response to the clock pulse until it rapidly drops to zero in response to the reset pulse. On the other hand, the output of frequency divider 12 is applied to a down-counter 15 to produce a decremental binary count value which represents the varying rate of the duty ratio. A monostable multivibrator 14 is provided for producing a pulse for clearing the contents of down-counter 15 as soon as the pager is alerted.

The digital output of down-counter 15 is applied to a binary-to-duty converter 16 which converts it to a digital value representing the duty ratio of the 2.6-kHz pulse sequence for each 6-second interval. In a typical example, binary-to-duty converter 16 successively generates outputs representing duty ratios of 12.5 %, 25 %, 33 % and 50 %. The outputs of binary-to-duty converter 16 and up-counter 13 are applied to a digital comparator 17 in which they are compared

with each other to produce a high-level output when the digital value of counter 13 is greater than the output of binary-to-duty converter 16. It is seen therefore that the output of comparator 17 is a sequence of constant-frequency pulses of a variable duty ratio which increases stepwisely at 6-second intervals as shown in Fig. 3. From the tone quality standpoint, the maximum duty ratio is set 50 % as described above.

The output of comparator 17 is applied to an AND gate 18 to which a POCSAG tone pattern, say A-code pattern, is also applied. In this way, the variable duty 2.6 kHz pulse sequence is modulated by the POCSAG A-code pattern as shown in Fig. 4 and applied through an amplifier 19 to the speaker 7. Loudspeaker 7 has a narrow band of frequency response characteristic. This characteristic is sufficient to suppress the harmonic components of the modulated alert tone pulse which may otherwise cause changes in tone quality with variations of the duty ratio.

Therefore, the POCSAG tone pattern can be used for generating an alert tone with successively escalating sound levels.

A modified form of the sound alarm circuit 6 is shown in Fig. 5. In this modification, a programmable counter 2b is used instead of the up-counter 13 and comparator 17. Programmable counter 20 is clocked by the output of AND gate 10 and reset by the output of frequency divider 11. The output of binary-to-duty converter 16 it applied to programmable counter 20 as a preset count value which decrement at 6-second intervals in response to the output of frequency divider 12 (Fig. 6), and hence the duty ratio of the tone pulses generated by programmable counter 20 increases with the decrease in the preset count value.

Alternatively, the present invention can be further modified as shown in Fig. 7 in which the down-counter is replaced with an up-counter 31 and binary-to-duty converter 32 transforms the stepwisely incremental value of the output of counter 31 to a stepwisely incremental duty ratio. A flip-flop 30 is provided having a set input terminal connected to the output of frequency divider 11 and a reset input terminal connected to the output of programmable counter 34 whose program input is connected to the output of binary-to-duty converter 32. An AND gate 33 is responsive to the output of flip-flop 30 to pass the output of AND gate 10 to the clock input of programmable counter 34. The output of flip-flop 30 is further applied to the reset input of programmabie counter 34 and one input of AND gate 18.

As shown in Fig. 8, flip-flop 30 is triggered into a high-level, set condition in response to each output pulse from frequency divider 11 to allow clock pulses from AND gate 10 to pass through AND gate 33 to the programmable counter 34. The latter produces a high-level output when the duty representing count value is reached and resets the flip-flop 30 to a low-level condition, producing a tone pulse having a stepwisely incremental duty ratio.

The foregoing description shows only one preferred embodiment of the present invention. Various modifications are apparent to those skilled in the art without departing from the scope of the present invention which is only limited by the appended claims. Therefore, the embodiment shown and described is only illustrative, not restrictive.

## Claims

1. A radio pager comprising:
   receive means for receiving a paging signal containing a unique identifier identifying said radio pager and an alert tone pattern;
   pulse generating means for generating constant audio frequency pulses having a duty ratio increasing as a function of time in response to receipt of said paging signal;
   modulating means for modulating said pulses with said alert tone pattern; and
   sound generating means activated by said modulated pulses.

2. A radio pager as claimed in claim 1, wherein said alert tone pattern is a POCSAG (Post Office Code Standardization Advisory Group) tone pattern.

3. A radio pager as claimed in claim 1, wherein said pulse generating means comprises:
   a clock source for generating pulses at a clock frequency;
   a first frequency divider for dividing the clock frequency of said pulses to produce pulses at an audio frequency;
   a second frequency divider for dividing the clock frequency of said pulses to produce pulses at a frequency much lower than said audio-frequency;
   means responsive to each of the audio frequency pulses for generating a series of first digital values which increase synchronously with said clock frequency pulses;
   means for generating second digital values which successively decrease in response to said lower frequency pulses;
   means for comparing said first and second digital values to produce an output signal when said first digital values are greater than said second digital values, said modulating means being coupled to said comparing means.

4. A radio pager as claimed in claim 1, wherein said pulse generating means comprises:
   a clock source for generating pulses at a clock frequency;
   a first frequency divider for dividing the

clock frequency of said pulses to produce pulses at an audio frequency;

a second frequency divider for dividing the clock frequency of said pulses to produce pulses at a frequency much lower than said audio-frequency;

means for generating digital values which successively decrease in response to said lower frequency pulses; and

presettable counter means having a count value successively preset to said digital values, said presettable counter means being responsive to each of the audio frequency pulses for counting said clock frequency pulses to produce an output pulse having a leading edge coinciding with time at which the count of the clock frequency pulses reaches the preset value and a trailing edge coinciding with each of said audio frequency pulses, said modulating means being coupled to said presettable counter means.

**5.** A radio pager as claimed in claim 1, wherein said pulse generating means comprises:

a clock source for generating pulses at a clock frequency;

a first frequency divider for dividing the clock frequency of said pulses to produce pulses at an audio frequency;

a second frequency divider for dividing the clock frequency of said pulses to produce pulses at a frequency much lower than said audio-frequency;

means for generating digital values which successively increase in response to said lower frequency pulses; and

bistable means arranged to be triggered into a first output state in response to each of the audio frequency pulses and triggered into a second output state in response to a reset signal applied thereto, said modulating means being coupled to said bistable means; and

presettable counter means having a count value successively preset to said digital values, said presettable counter means being responsive to the first output state of said bistable means for counting said clock frequency pulses to produce an output pulse to said bistable means as said reset signal the count of the clock frequency pulses reaches the preset value.

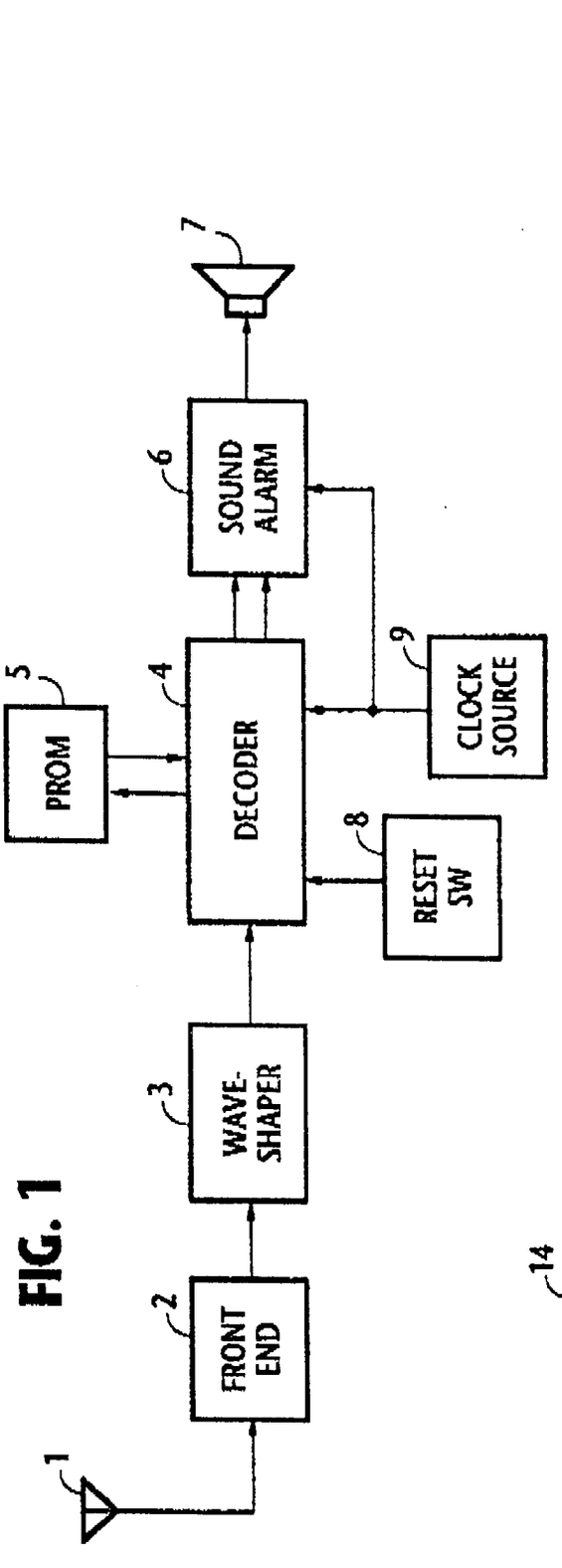

1
FRONT END
2
WAVE-SHAPER
3
DECODER
4
PROM
5
SOUND ALARM
6
7
RESET SW
8
CLOCK SOURCE
9

FIG. 1

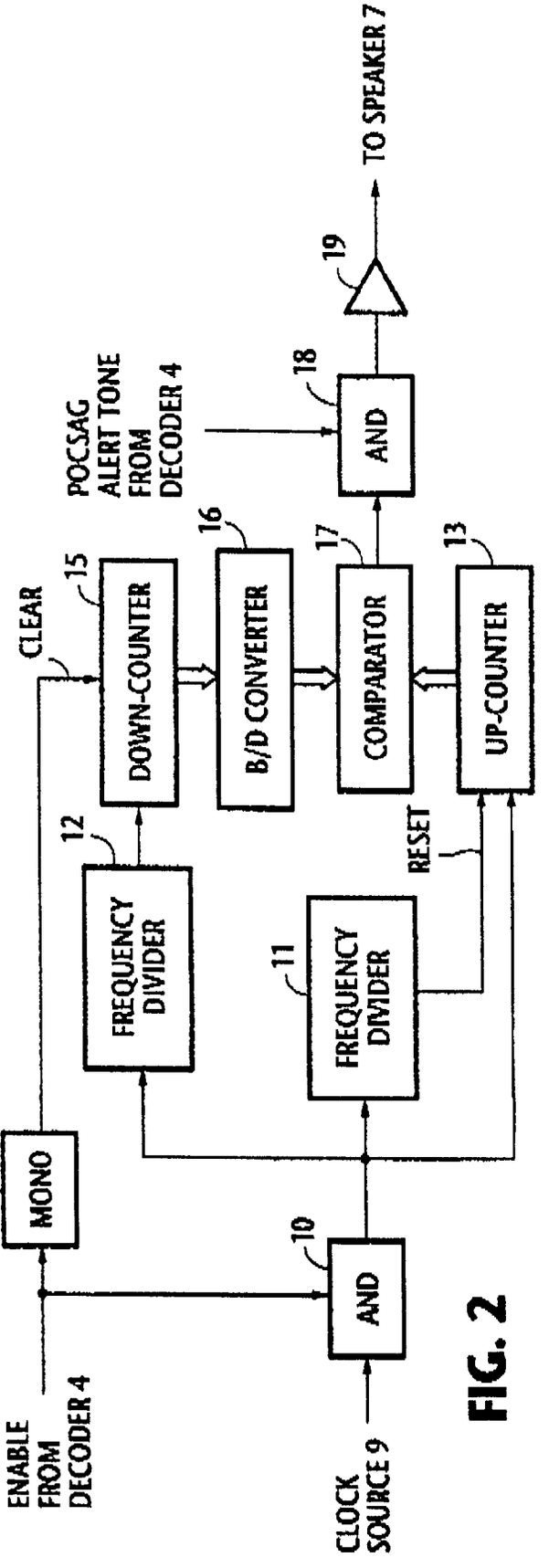

ENABLE FROM DECODER 4
MONO
14
AND
10
CLOCK SOURCE 9
FREQUENCY DIVIDER
12
FREQUENCY DIVIDER
11
CLEAR
DOWN-COUNTER
15
B/D CONVERTER
16
COMPARATOR
17
UP-COUNTER
13
RESET
POCSAG ALERT TONE FROM DECODER 4
AND
18
19
TO SPEAKER 7

FIG. 2

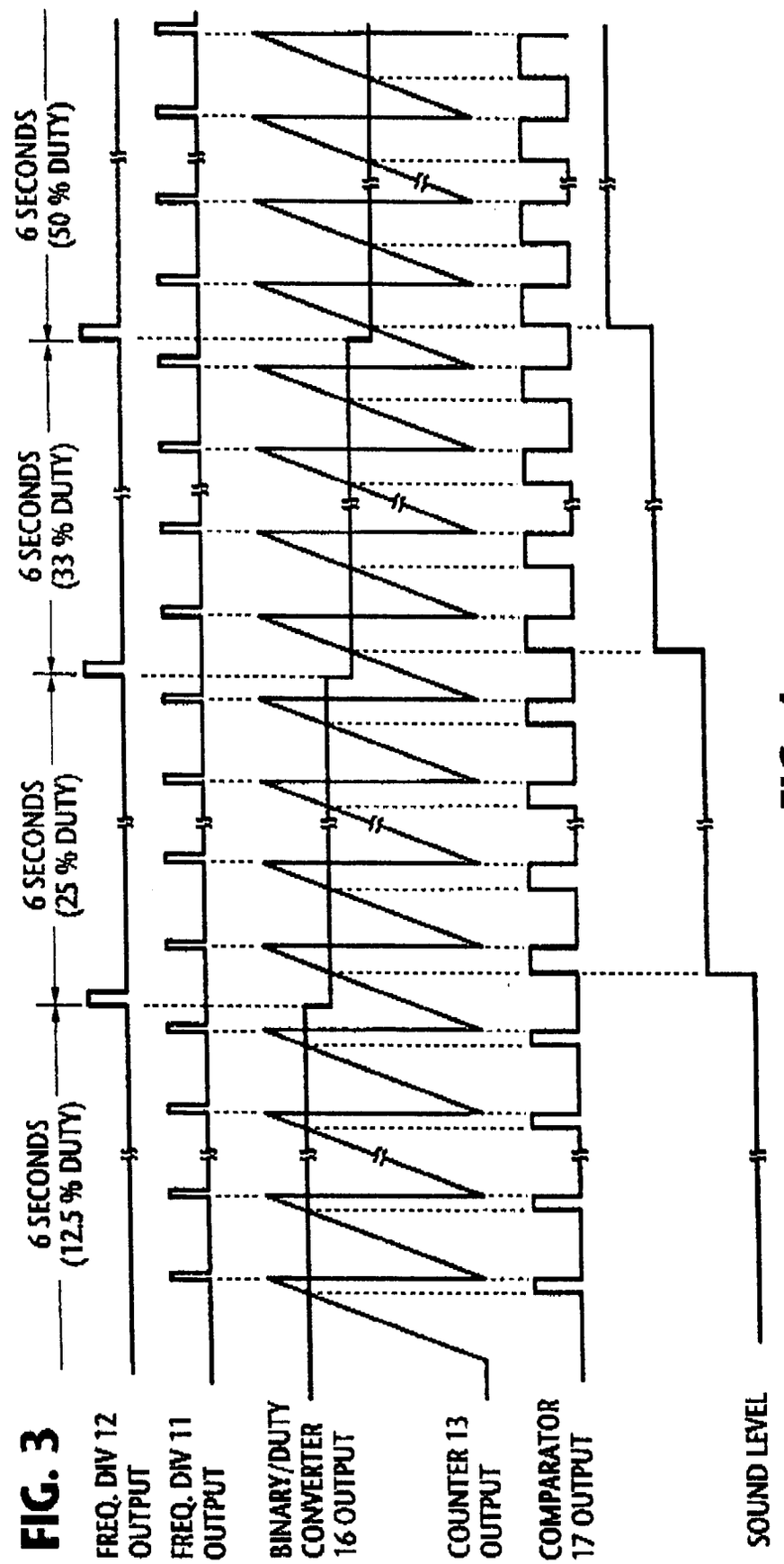

6 SECONDS (12.5 % DUTY)
6 SECONDS (25 % DUTY)
6 SECONDS (33 % DUTY)
6 SECONDS (50 % DUTY)
FREQ. DIV 12 OUTPUT
FREQ. DIV 11 OUTPUT
BINARY/DUTY CONVERTER 16 OUTPUT
COUNTER 13 OUTPUT
COMPARATOR 17 OUTPUT
SOUND LEVEL

FIG. 3


6 SECONDS (12.5 % DUTY)
6 SECONDS (25 % DUTY)
6 SECONDS (33 % DUTY)
1/8 SEC
7/8 SEC
POCSAG A-CODE PATTERN
MODULATED OUTPUT

FIG. 4

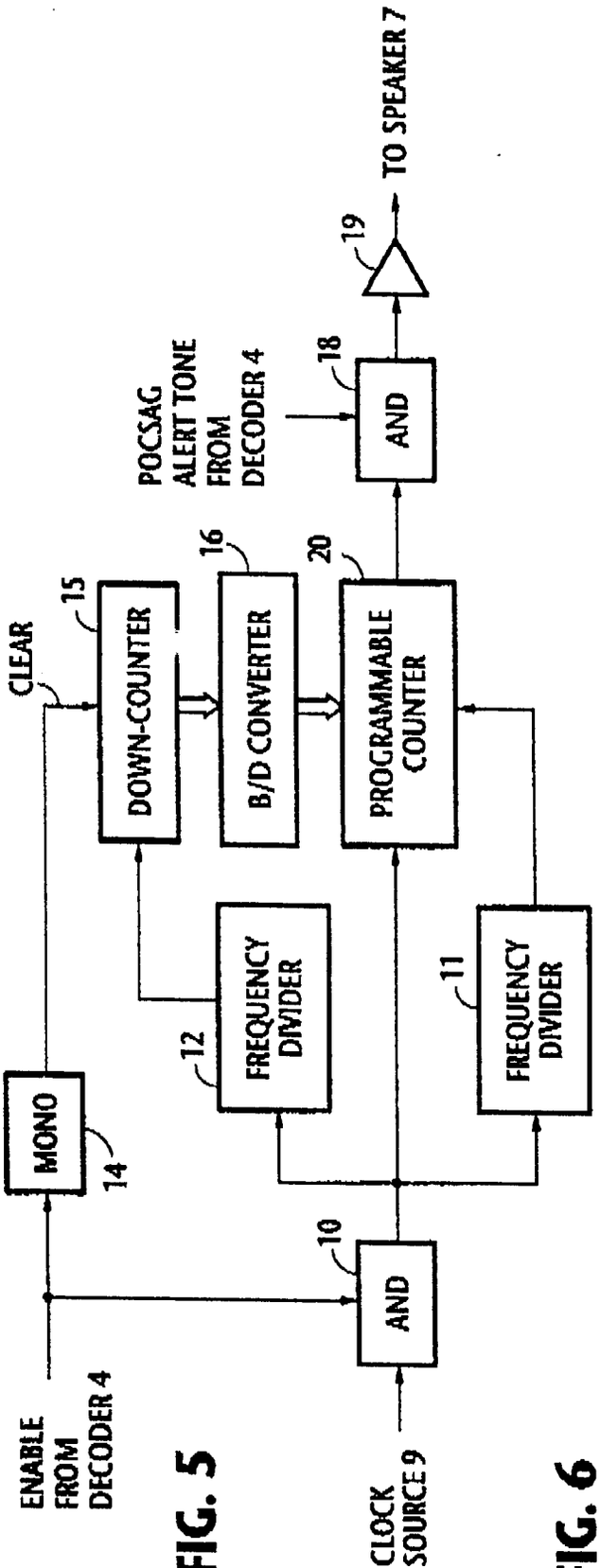

ENABLE FROM DECODER 4
MONO
14
CLEAR
15
DOWN-COUNTER
12
FREQUENCY DIVIDER
16
B/D CONVERTER
POCSAG ALERT TONE FROM DECODER 4
10
AND
CLOCK SOURCE 9
20
PROGRAMMABLE COUNTER
11
FREQUENCY DIVIDER
18
AND
19
TO SPEAKER 7

FIG. 5

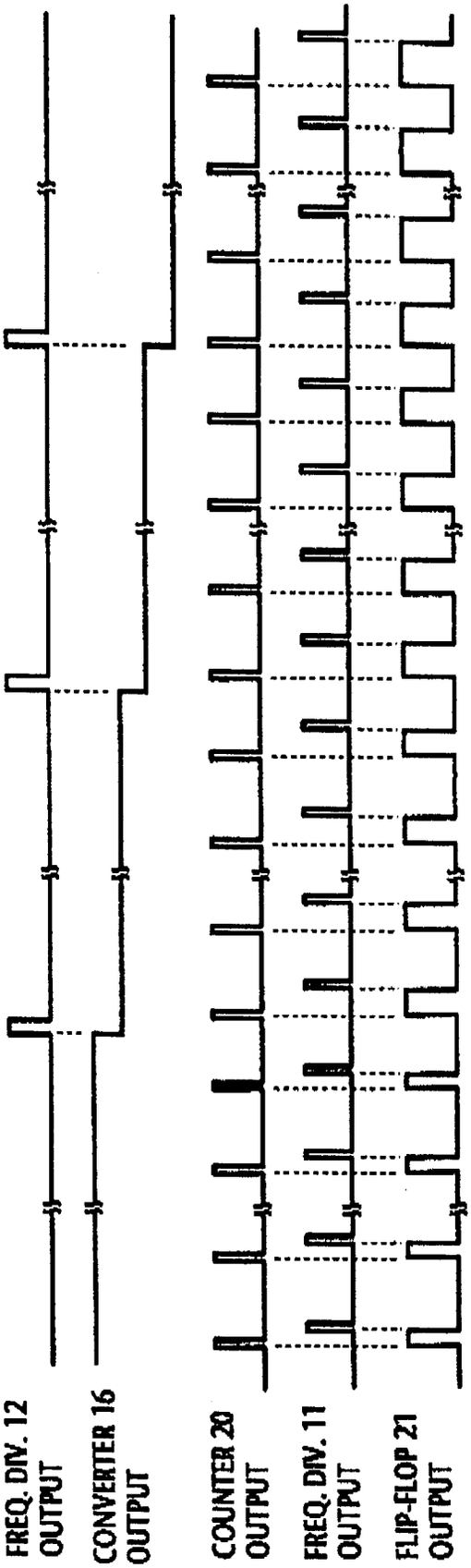

FREQ. DIV. 12 OUTPUT
CONVERTER 16 OUTPUT
COUNTER 20 OUTPUT
FREQ. DIV. 11 OUTPUT
FLIP-FLOP 21 OUTPUT

FIG. 6

FIG. 7

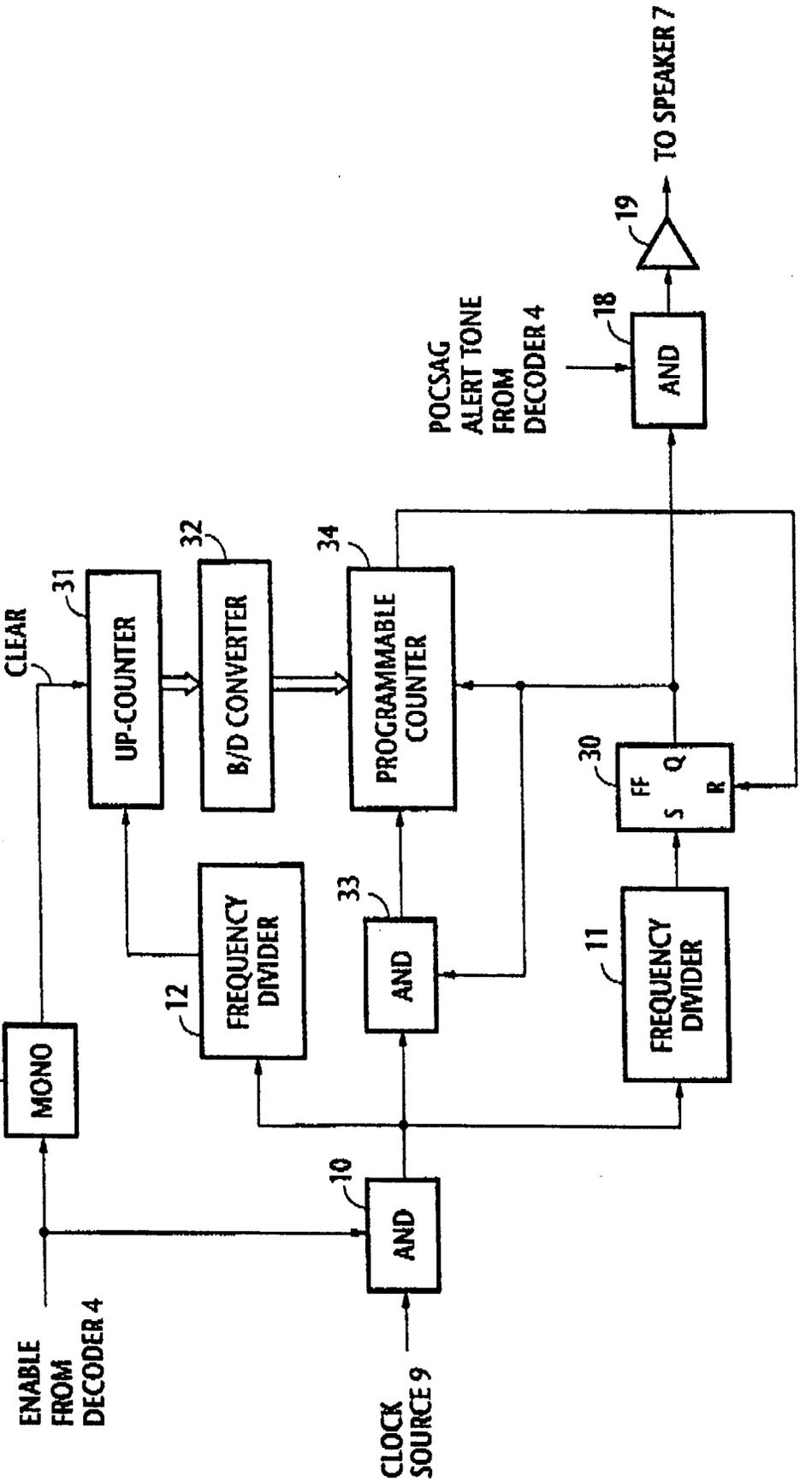
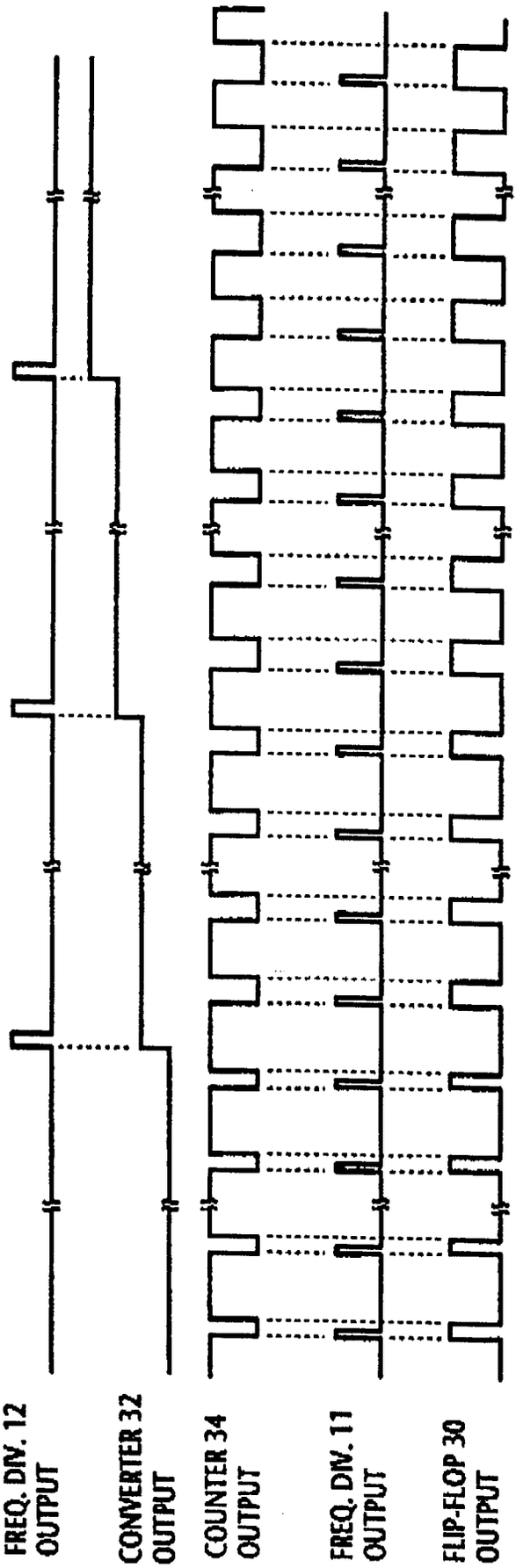

ENABLE FROM DECODER 4
CLOCK SOURCE 9
MONO
14
AND
10
FREQUENCY DIVIDER
12
UP-COUNTER
31
CLEAR
B/D CONVERTER
32
PROGRAMMABLE COUNTER
34
AND
33
FREQUENCY DIVIDER
11
FF
S
Q
R
30
POCSAG ALERT TONE FROM DECODER 4
AND
18
19
TO SPEAKER 7

FIG. 8


FREQ. DIV. 12 OUTPUT
CONVERTER 32 OUTPUT
COUNTER 34 OUTPUT
FREQ. DIV. 11 OUTPUT
FLIP-FLOP 30 OUTPUT

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 91 31 2066

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| P,A | WO-A-9 106 932 (MOTOROLA, INC.)<br>* page 3, line 23 - line 25; figures 2,3 *<br>--- | 1 | G08B3/10<br>H04Q7/02 |
| A | FR-A-2 287 732 (ETABLISSEMENTS DAUMAS S.A.)<br>* page 5, line 17 - line 26; figure 2 *<br>--- | 1 | |
| A | US-A-4 237 448 (WEINBERG)<br>* column 4, line 49 - line 64 *<br>* abstract; figures 2-4 *<br>--- | 1 | |
| A | EP-A-0 265 064 (NEC CORPORATION)<br>* the whole document *<br>----- | | |

| TECHNICAL FIELDS SEARCHED (Int. Cl.5) |
|---|
| G08B<br>H04Q<br>H03G |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 17 MARCH 1992 | DANIELIDIS S. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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L : document cited for other reasons

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