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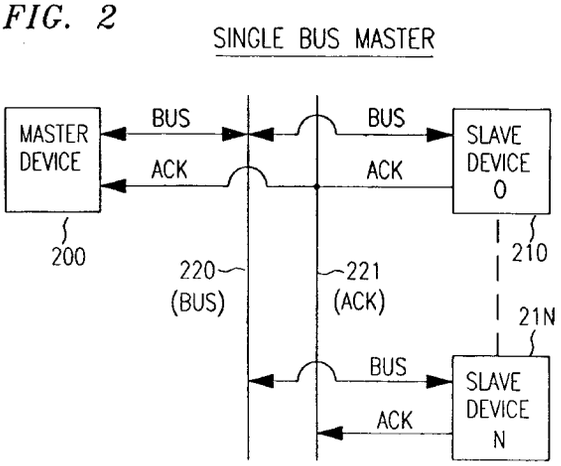
(54) Microprocessor with low power bus.

(57) A microprocessor provides a bus state referred to as "loop-back". This state holds the data bus at valid logic levels, without use of resistors, after a read transaction has been completed and there are no pending bus transactions. When this state is entered, the data just read from the data bus (220) is driven back onto the data bus, and the device (210, 21N) which had provided the data is placed in the tri-state (high--impedance) condition. This loop-back feature, combined with the fact that all other outputs are held at their previous values, provides for near-zero power dissipation on the bus. The inventive technique avoids the use of pull-up resistors (R_1... R_n), which are provided on prior art tri-state busses (C_1 ... C_n) to ensure that the busses do not float and enter the threshold region where high power dissipation occurs.

FIG. 2



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Background of the Invention

Description of the Prior Art

Integrated circuits (ICs) typically communicate with one another by means of one or more multi-conductor busses. For example, a 32-bit microprocessor IC may use 32 conductors to send a 32-bit data word to another integrated circuit, or to an external input/output device. Several busses may be required, with the use of separate busses for data and addresses often being used. In other cases, a given bus may be multiplexed so that it may perform two or more functions at different times. In some cases, the output buffers that drive the bus are always active, so that either a valid logic "1" or "0" is always present on the bus. However, in other cases, the output buffers are capable of being placed in the "tri-state" (high output impedance) condition. In that case, neither a high nor low logic state is provided by the output buffer. Therefore, the bus voltage is free to float when all of the integrated circuits connected to the bus are in the tri-state condition. It is frequently the case that resistors are connected from the bus conductors to a given power supply voltage, in order to prevent the bus from floating. This is especially true in busses that connect to devices having field effect transistor input stages. For example, CMOS input buffers having serially connected p-channel and n-channel input transistors which have their gates coupled to the input node may draw a large current when the input node floats in the vicinity of the buffer switching point (typically about 1/2 V_{DD}).

An illustrative prior art bus is shown in Fig. 1, wherein the resistors R_1 ... R_n pull the bus conductors 1 .... n to the V_{DD} power supply voltage level when all the output buffers O_1 ... O_n connected to the bus are placed in the tri-state condition. As noted above, it is desirable to avoid allowing the conductors to float at an intermediate state between power supply voltage levels, as that could allow the field effect transistor input buffers I_1 ... I_n to draw excessive currents. However, the pull-up resistors R_1 ... R_n themselves cause some power dissipation to occur when the bus is active. That is, when an output buffer places a "0" (i.e., low voltage) on a given conductor, current flows through the corresponding resistor. (Alternatively, the resistors could connect the bus to V_{SS}, in which case the current flow would occur when a "1" is driven onto the bus). Since the value of the resistors are typically in the range of from about 1 k ohm to 10 k ohms, several milliamps of current may flow when the bus is active.

It has become especially desirable to minimize the current drain associated with integrated circuits that are used in battery-powered devices. These include, for example, laptop and notebook computers, cellular phones, video terminals, etc. In many cases, the amount of power dissipated in the bus resistors (R_1 ... R_n) is a significant portion of the total power dissipation. Furthermore, as the size of on-chip cache memories increase, the number of bus transactions to external memories tends to be reduced. Therefore, the idle time on the external bus tends to increase, and power dissipation on a floating bus (due primarily to current flow in input buffers) would also increase. Hence, the necessity of using resistors in an attempt to limit the dissipation also tends to increase in prior art bus schemes.

Summary of the Invention

I have invented an integrated circuit as set out in the claims that reduces the power dissipation required to drive a bus.

Brief Description of the Drawings

Fig. 1 shows a prior-art bus with pull-up resistors.

Fig. 2 shows a bus arrangement having a single master device.

Fig. 3 shows a bus arrangement having two master devices.

Fig. 4 shows a timing diagram for the bus arrangement of Fig. 2.

Fig. 5 shows a timing diagram for the bus arrangement of Fig. 3.

Fig. 6 shows one embodiment of circuitry according to the present invention.

Fig. 7 shows an alternate embodiment of circuitry according to the present invention.

Detailed Description

The present detailed description relates to an improved technique for communicating data over an integrated circuit bus, whereby the power dissipation may be reduced. Referring to Fig. 2, an illustrative bus arrangement suitable for use with the inventive technique is shown. This arrangement is of a type well known in the art, but note that no external resistors are necessary. The "master device" 200 is typically a microprocessor, but may alternatively be a digital signal processor (DSP), arithmetic unit (ALU), or other type of logic device that initiates bus transactions. The "slave devices" 210 to 21N are typically memory or peripheral devices, including, for example, video displays, keyboards, disc drives, or other input/output devices. When the master device initiates a read operation, it sends a signal on the bus (220) that indicates the device to which it desires access. The signal may be of various protocol types, and the read request initiates the transfer of data from the slave to the master over the bus. The transfer typically occurs in one or more bytes of data bits being sent in parallel (i.e., simultaneously) over the bus conductors. After

the designated slave device sends the data, it sends an acknowledgement signal to the master device on the ACK line (221). The output buffers of the designated device connected to the bus then enter the tri-state condition.

In the present invention, the master device 200 enters a "loop-back" state upon receiving the acknowledgement signal when no further transactions are pending. The loop-back state holds valid the data last received by the master device, by actively driving the bus conductors from the master device. This avoids the possibility of floating bus conductors, as would otherwise occur if all the devices connected to the bus were in the tri-state condition. The loop-back state also avoids unnecessary signal transitions, as would occur, for example, if all the outputs were changed to the high state in order to avoid the current flow in the circuit of Fig. 1. Referring to Fig. 4, a timing diagram shows the time period (bus cycles N... N3) during which the slave device drives the data bus with the data requested by the master device. When the data acknowledgement signal ($\overline{ACK}$) is asserted (pulled low) by the slave device, the master device enters the loop-back state, since there are no further transactions pending in the illustrative case. The loop-back state is maintained for bus cycles N+4... N+8. A new transaction is initiated by the master device at bus cycle N+9. The new transaction, which may be either a read or a write operation, terminates the loop-back state, thereby allowing the master device to send the new request over the bus.

The present invention may be implemented using the illustrative circuit diagrams shown in Figs. 6 and 7, with others being possible. These circuits are embodiments of an input/output (I/O) buffer on the master device that is connected to the data bus. There are typically "n" such I/O buffers, where "n" is the number of bus conductors (Fig. 1). In Fig. 6, the data bus is connected to an input buffer 60, which drives an input latch 61 that holds the received data for a specified time period. The output of the latch 61 is provided to the other microprocessor circuitry via the DATA IN line, as in the prior art. However, in addition, the output of the latch 61 is looped-back to the output buffer (tri-state driver 63) through the 2 to 1 multiplexer 62 during the loop-back state. Therefore, in the loop-back state, the data that was last received through the input buffer 60 is latched (held at valid logic levels) back onto the data bus. Note that when the loop-back state is terminated the multiplexer 62 selects the DATA OUT line, thereby breaking the loop. The I/O buffer may then send or receive new data, as required. Note that the multiplexer may be implemented using transmission gate logic, AND/OR logic gates, or a tri-stated inverter, for example, according to principles well known in the art.

An alternate embodiment of an I/O buffer that may be used for implementing the invention is shown in Fig. 7. In that embodiment, the input latch is omitted, and the output of the input buffer 70 is connected directly to the input of the multiplexer 71. The use of an input latch (61 in Fig. 6) aids in ensuring that any data glitches or noise on the bus do not interfere with the loop-back state. Otherwise, the operation of the circuitry of Fig. 7 is comparable to that of Fig. 6. As above, the multiplexer may select the loop-back state, by connecting input buffer 70 to the input of the output buffer (tri-state driver 72), or else may select conventional operation by connecting the DATA OUT line to the input of the driver 72.

The present invention may also be applied to bus architectures that utilize two or more master devices. For example, a microprocessor and floating point processor may communicate over the same bus with various peripheral devices to increase computation speed. In another example, a microprocessor and digital signal processor may share a bus, to provide high-definition graphics, or speech recognition, or other advanced functions. As shown in Fig. 3, a known technique for allowing N master devices (300 ... 30N), and M slave devices (330 ... 33M) to communicate over a bus 341 is shown. For example, when master device 0 desires to initiate a bus transaction, it activates the line $\overline{BREQ0}$ by pulling it to the low state, thereby requesting the bus from the bus arbiter 320. The arbiter 320 grants the request by pulling line $\overline{BGRANT0}$, thereby allowing master device 0 to proceed with the bus transaction. Note that if bus requests from two or more master devices occur simultaneously, the bus arbiter 320 chooses which one is to have access first. The present invention may thus be implemented with this type of architecture, by performing the loop-back with the master device selected by the arbiter to have access at any given time.

For example, referring to Fig. 5, the timing diagram for master device 0 is shown for the above case. In the time period shown, the $\overline{BREQ0}$ line has returned to the high (inactive) state after the above-noted request, indicating no further requests (i.e., no pending transactions) from master device 0. Also as shown, the $\overline{BGRANT0}$ line is initially low (active), thereby granting bus access to master device 0. The data is supplied from the slave device to master device 0 during bus cycles N to N+3, after which the low-going $\overline{ACK}$ line signals the end of the data transfer. The master device 0 then enters the loop-back state during bus cycles N+4 through N+8, as described above. Thereafter, in the illustrative case, another master device with a pending transaction gains access to the bus. When that occurs, the $\overline{BGRANT0}$ line goes high (inactive), so that master device 0 no longer has bus access. Therefore, the loop-back state is terminated for master device 0 at bus cycles N+9. Another way of terminating the loop-back state is when master device 0 itself has a new pending transaction. In that case, a new bus request

is made by pulling $\overline{\text{BREQ0}}$ low, as indicated by the dotted line at bus cycles N+8 and N+9. In that case, the loop-back state terminates at bus cycle N+8, in order to free up the bus for a new data transfer (either send or receive).

The above description has been given in terms of an integrated circuit communicating on an external bus. However, the present invention may alternatively be applied to communicating on an internal bus within an integrated circuit. This approach becomes desirable, for example, as IC chip densities increase, and more functions communicate over an internal bus. It is especially applicable to wafer-scale integrated circuits, where the number of devices communicating over a given bus within the integrated circuit may be large. As described above, the bus is typically a multi-conductor bus having at least 8 conductors, and most typically 16, 32, or 64 conductors in current designs. However, the present invention may also be advantageously used with a single conductor bus. For example, the acknowledgement (ACK) line noted above may be driven in the inventive manner. Furthermore, while the integrated circuits connected to the bus typically include field-effect transistor input stages, the use of the present technique is advantageous for integrated circuits have bipolar input stages in many cases. The output buffer and loop-back circuitry may also be formed with bipolar or field effect devices, depending on the IC technology used. Still other variations and deviations apparent to persons of skill in the art are included herein.

Claims

1. An integrated circuit comprising:
   means (63) for sending data signals, and means (60) for receiving data signals, over a bus (220), and
   means (200) for requesting data to be sent over the bus, and means (221) for receiving acknowledgement of the receipt of data sent over the bus:
   characterized in that said integrated circuit further comprises means (62) for maintaining valid on said bus the last-received data, when said integrated circuit receives the acknowledgement of the receipt of said last-received data and no further bus transactions are pending.

2. The integrated circuit of claim 1 wherein said means for sending data signals comprises a tri-state output buffer (63) and said means for receiving data signals comprises an input buffer (60), and further
   characterized in that said means for maintaining valid on said bus the last-received data comprises multiplexer means (62) for coupling the output of said input buffer to be input of said output buffer.

3. The integrated circuit of claim 2 wherein said means for receiving data signals further comprises an input latch (61), wherein the output of said input buffer is coupled to said multiplexer through said latch.

4. The integrated circuit of any of the preceding claims wherein said means for receiving data signals comprises a field effect transistor input stage.

5. The integrated circuit of claim 4 wherein said field effect transistor input stage includes a CMOS input buffer.

6. The integrated circuit of any of the preceding claims wherein said bus is external to said integrated circuit.

7. The integrated circuit of claim 6 wherein said bus is a multi-conductor bus.

8. The integrated circuit of claim 6 wherein said bus is a single-conductor bus.

9. A data system comprising a first master device (300) and a multiplicity of slave devices (330,33M) that communicate over a bus (341), wherein said master device comprises:
   means (63) for sending data signals, and means (60) for receiving data signals, over said bus, and
   means for requesting data to be sent over the bus, and means (342) for receiving acknowledgement of the transfer of data sent over the bus;
   characterized in that said first master device further comprises means (62) for maintaining valid on said bus the last-received data, when said first master device receives acknowledgement of the transfer of said last-received data and no further bus transactions are pending.

10. The data system of claim 9 further comprising a second master device (30N) that communicates over said bus, wherein said second master device comprises:
    means (63) for sending data signals, and means (60) for receiving data signals, over a bus, and
    means for requesting data to be sent over the bus, and means (342) for receiving acknowledgement of the transfer of data sent over the bus;

and further characterized in that said second master device further comprises means (62) for maintaining valid on said bus the last-received data, when said second master device receives acknowledgement of the transfer of said last-received data and no further bus transations are pending;

and wherein said data system further comprises arbitration means (320) for choosing which of said first (300) and second (30N) master devices has access to said bus (341) at a given time.

11. The data system of claim 9 or claim 10 wherein the or each said means for sending data signals comprises a tri-state output buffer (63) and the or each said means for receiving data signals comprises an input buffer (60), and further

characterized in that the or each said means for maintaining valid on said bus the last-received data comprises multiplexer means (62) for coupling the output of said input buffer to the input of said output buffer.

12. The data system of claim 11 wherein the or each said means for receiving data signals further comprises an input latch (61), wherein the output of said input buffer (60) is coupled to said multiplexer (62) through said latch.

13. The data system of any of claims 9 to 12 wherein the or each said means for receiving data signals comprises a field effect transistor input stage.

14. The data system of claim 13 wherein said field effect transistor input stage includes a CMOS input buffer.

15. The data system of claim 10 wherein said first master device is formed in a first integrated circuit, said second master device is formed in a second integrated circuit, and said bus is external to said first and second integrated circuits.

16. The data system of claim 15 wherein said bus (341) is a multi-conductor bus.

17. The data system of claim 15 wherein said bus (341) is a single-conductor bus.

FIG. 1

(PRIOR ART)

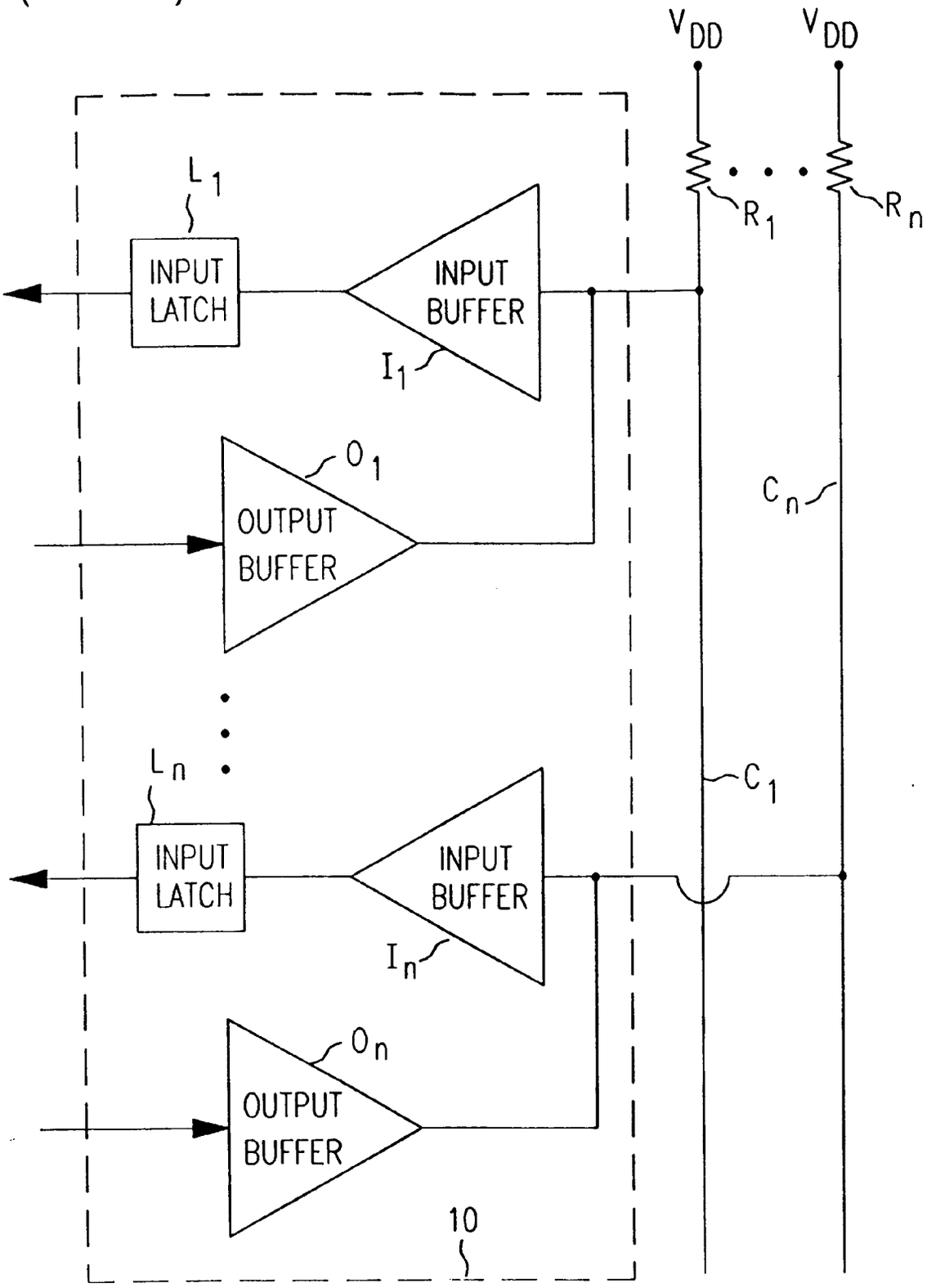


FIG. 2

SINGLE BUS MASTER

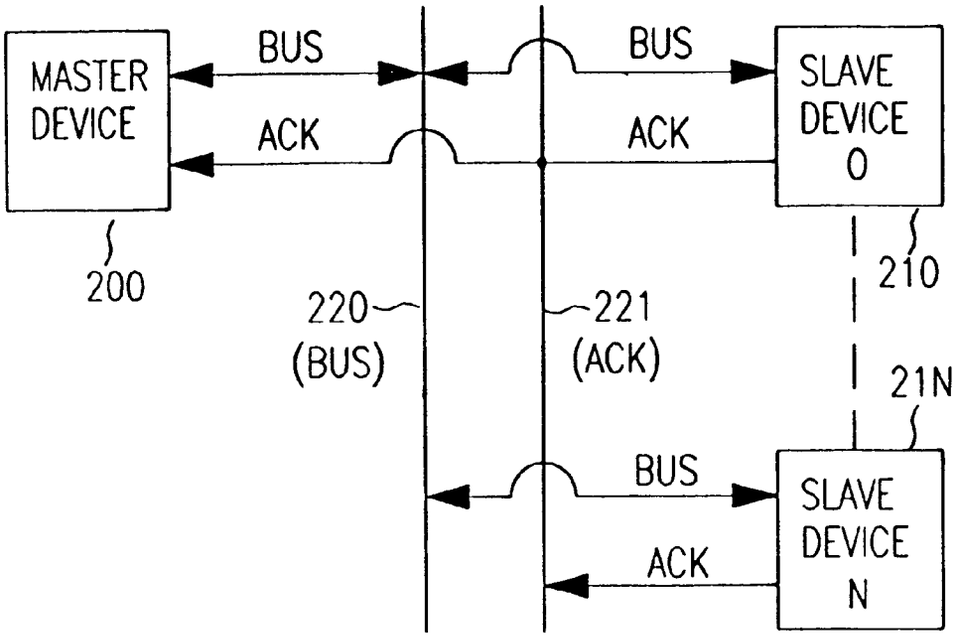


FIG. 3

MULTI PROCESSOR

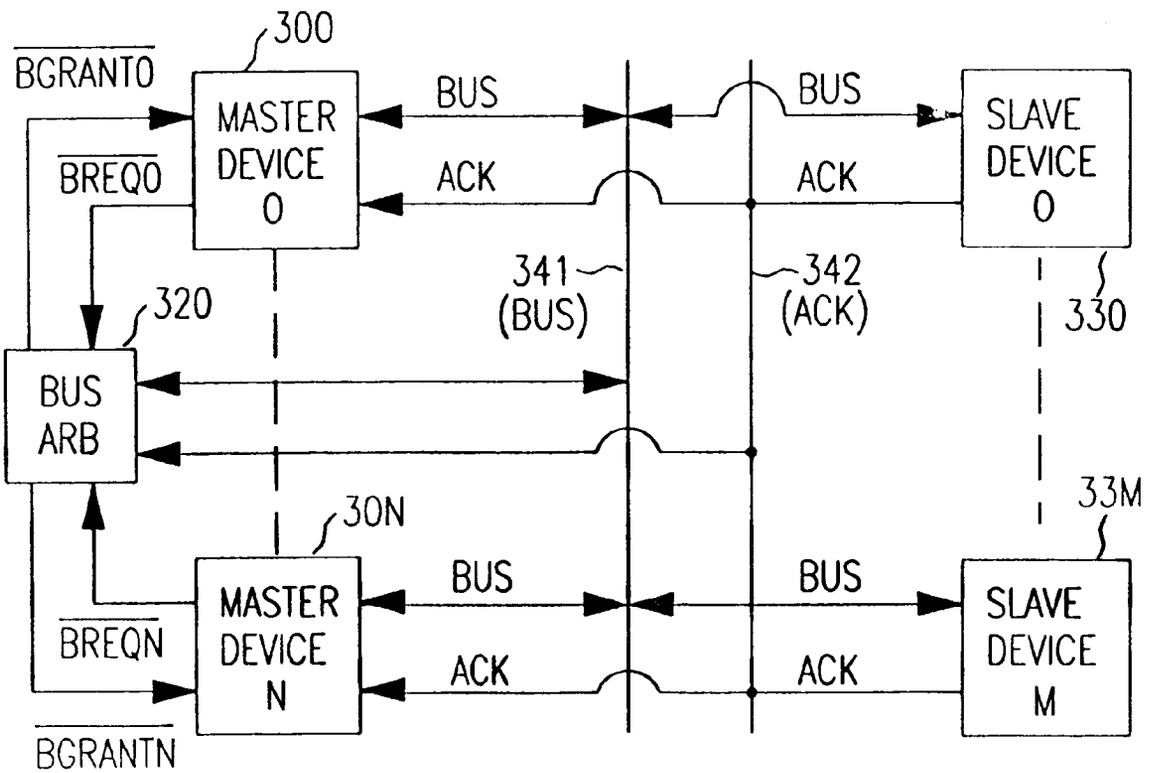


FIG. 4

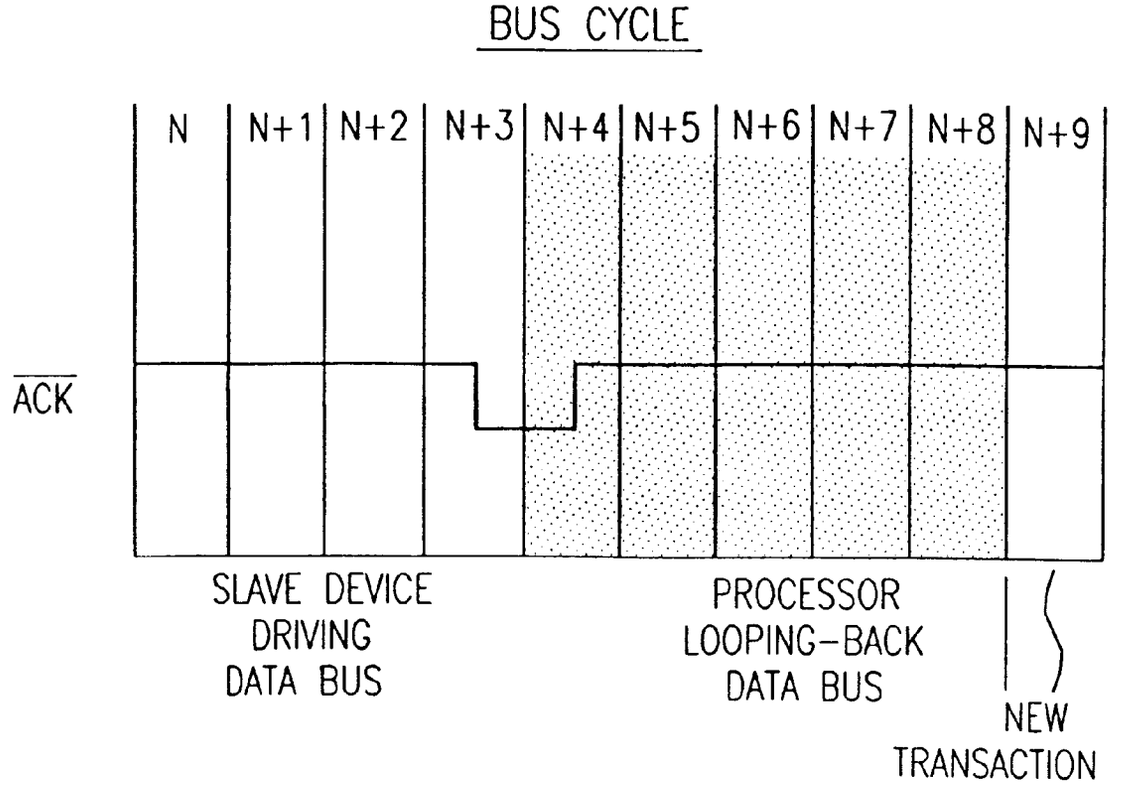

BUS CYCLE
N
N+1
N+2
N+3
N+4
N+5
N+6
N+7
N+8
N+9
ACK
SLAVE DEVICE DRIVING DATA BUS
PROCESSOR LOOPING-BACK DATA BUS
NEW TRANSACTION

FIG. 5

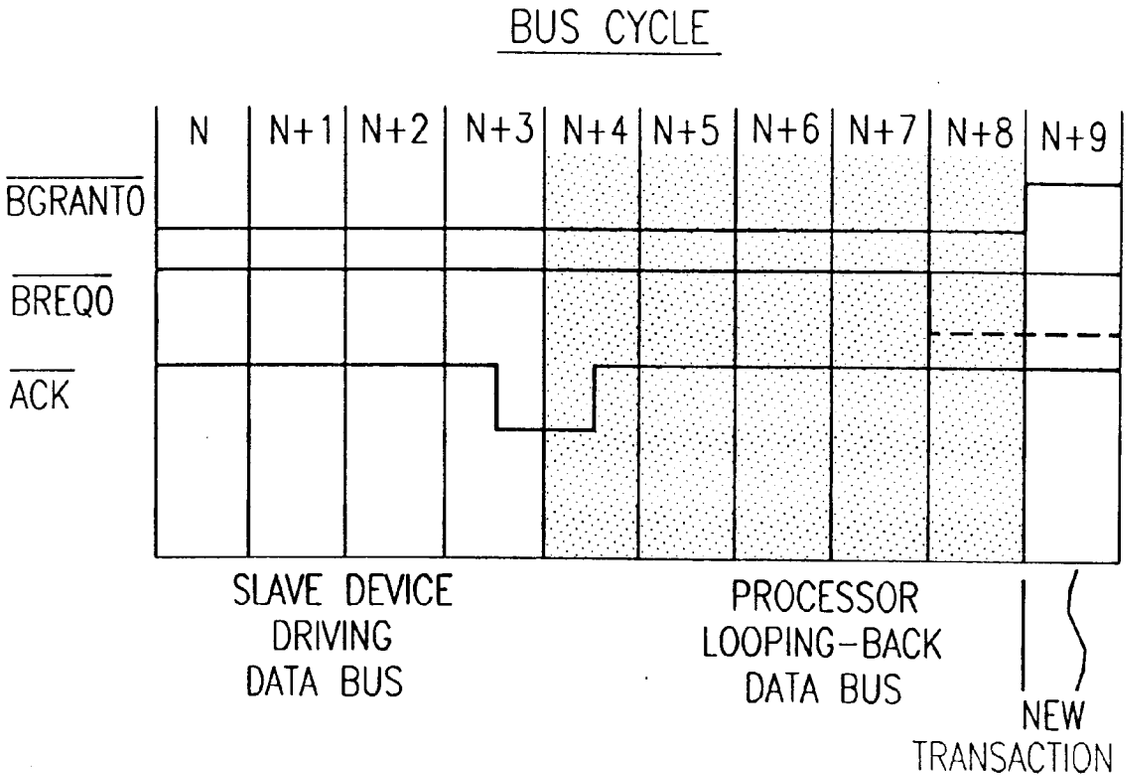

BUS CYCLE
N
N+1
N+2
N+3
N+4
N+5
N+6
N+7
N+8
N+9
BGRANTO
BREQO
ACK
SLAVE DEVICE DRIVING DATA BUS
PROCESSOR LOOPING-BACK DATA BUS
NEW TRANSACTION

FIG. 6

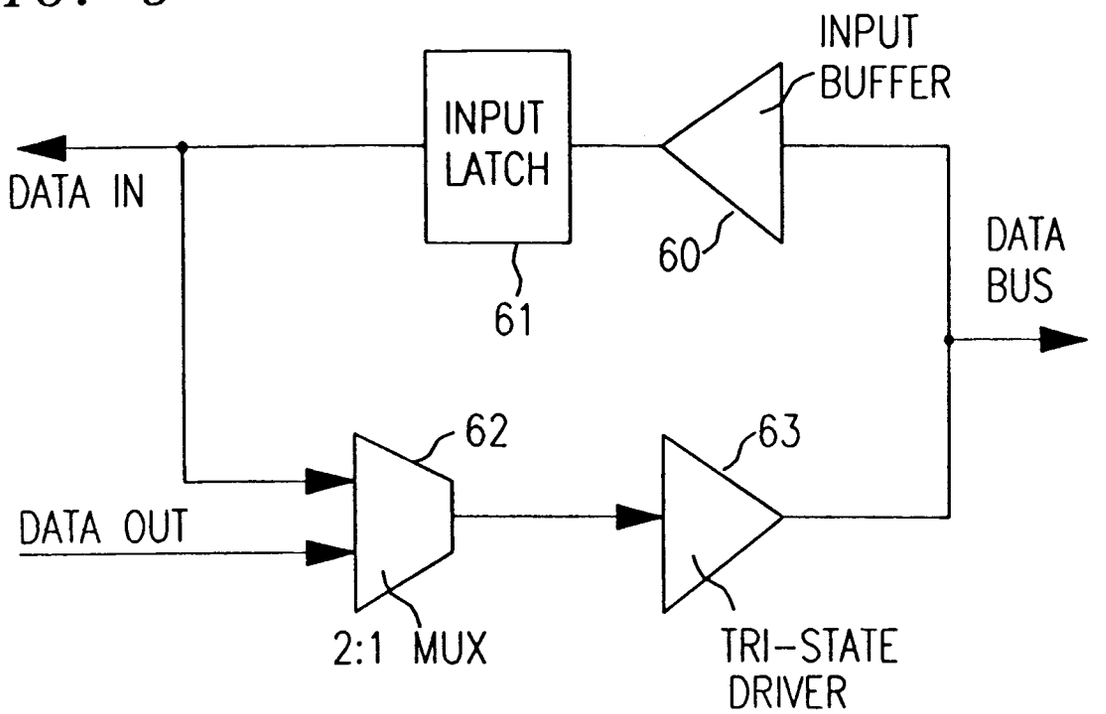
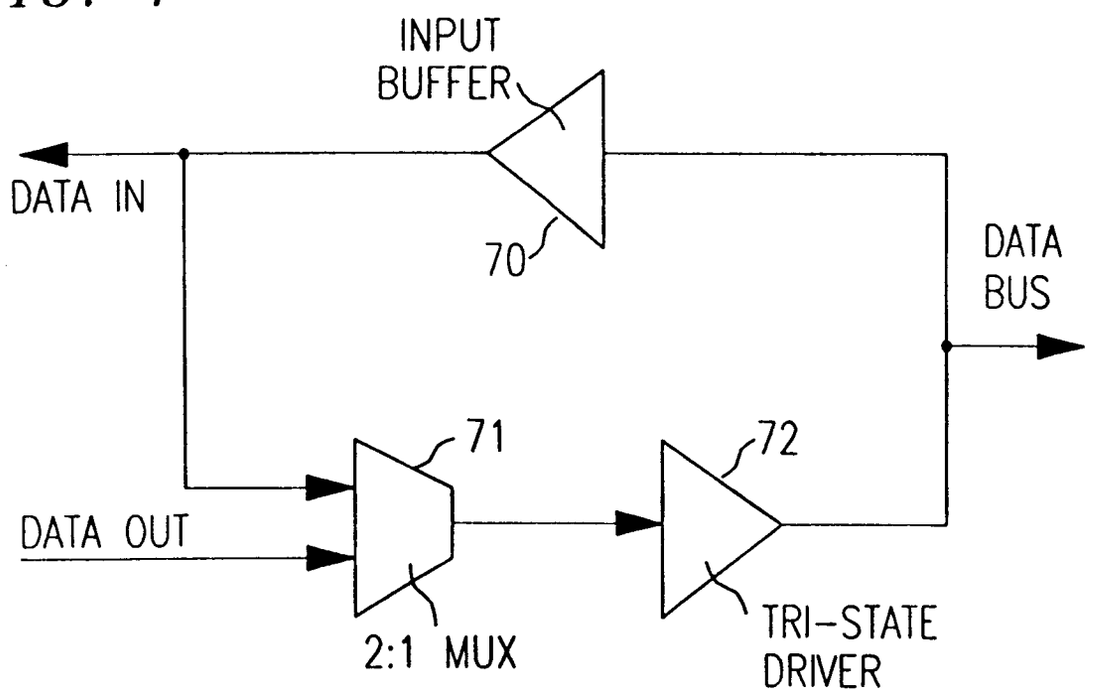

INPUT
BUFFER
INPUT
LATCH
DATA IN
60
61
DATA
BUS
62
63
DATA OUT
2:1 MUX
TRI-STATE
DRIVER

FIG. 7


INPUT
BUFFER
DATA IN
70
DATA
BUS
71
72
DATA OUT
2:1 MUX
TRI-STATE
DRIVER

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 1922

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 10, no. 104 (E-317)(2161) 19 April 1986 & JP-A-60 242 724 (NIPPON DENKI K.K.) 2 December 1985	1-3,9	G06F13/40
A	* abstract *	4-8, 10-12	

X	ELEKTRONIK. vol. 33, no. 7, April 1984, MUNCHEN DE pages 43 - 54; HANS EICHEL: 'Was ist beim Entwurf von CMOS-Mikrocomputern zu beachten?'	1-3,9	
A	* page 53, paragraph 4.1 * * figure 4 *	4-8, 10-12	

A	EP-A-0 341 841 (DIGITAL EQUIPMENT CORPORATION) * column 1, line 21 - line 35 * * column 3, line 22 - line 53 * * column 4, line 34 - line 48 * * figure 1 *	1-15	
	---		TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	US-A-4 551 821 (YOKOUCHI ET AL.) * column 1, line 8 - line 24 * * column 2, line 53 - column 3, line 31 * * claim 1; figure 1 *	1-15	G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 JUNE 1992	NGUYEN Xuan Hiep C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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