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(54) Color palette circuit.

(57) Color palette circuits are disclosed which utilize first and second color look-up tables which use information from a video bit map to address storage locations in the look-up tables, and then combine the information stored in the selected storage locations using digital adder or digital multiplier circuits, the resulting combined signals are then converted to analog signals, which may be used to generate color pixels. The use of a combining means permits the generation of a greater number of displayable colors than the sum of the number of storage locations in the look-up tables.

EP 0 508 626 A2

This invention relates to the field of digital electronics relating to the generation of a color display and more particularly to color palette circuitry utilized in the generation of drive signals for generating color displays.

Description of the Prior Art

Figure 1 illustrates in highly simplified, and block diagram form, a typical prior art approach for a color palette circuit 1. Typically current day CMOS color palette circuits are implemented on integrated circuit chips and the block indicated by reference character 2 denotes the integrated circuit boundary, that is the circuitry within boundary 2 is found on the chip and they indicate inputs and outputs are external. Color palette circuit 1 includes color look-up table 3, which is typically a RAM device having 256 storage locations each 24 bits wide. Each of the storage locations in color look-up table 3 is loaded with digital information from an external source to define a combination of red, green and blue color components to create up to 256 unique colors. The 256 addresses included in color look-up table 3 are accessed by information received from a video bit map over bus 4 having 8 individual lines which is indicated in this figure by the slash through the bus and the number eight adjacent to the slash. With 8, bits of address input, each one of the storage locations may of course be uniquely addressed. In Figure 1, as well as throughout the application, parallel buses are indicated by a line having a slash through it and the number of individual lines in the parallel bus is indicated by the number adjacent to the slash. Color palette circuit 1 further includes red digital-to-analog converter 5, green digital-to-analog converter 6 and blue digital-to-analog converter 7. The term digital-to-analog converter and the acronym "DAC" are used herein to represent a digital to voltage converter or a digital to current converter. When a memory location in color look-up table 3 is addressed, the information contained in the storage location is provided, 8 bits each, to red digital-to-analog converter 5 over bus 8, 8 bits of green color information is provided to green digital-to-analog converter 6 over bus 9 and similarly 8 bits of blue color information is provided to blue digital-to-analog converter 7 over bus 10. The digital information received by each of the digital to analog converters is converted to an analog signal to provide red, green and blue color components, provided respectively at outputs 11, 12 and 13, for use in generating a color pixel. In certain applications it is desirable to be able to provide more than 256 unique colors and the typical prior art approach to doing so is to provide a larger look-up table having additional storage locations. For example, to provide 4096 displayable colors it would be necessary to utilize 12 bits of address information to address 4096 storage locations. It will of course be appreciated that in order to accommodate this significantly increased number of storage locations a substantially larger color look-up table is required, which correspondingly utilizes substantially more area on the integrated circuit chip which may be impractical in view of the other circuitry which is required to be included on the chip.

A typical commercial prior art color palette circuit, which is available from Advanced Micro Devices, Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, California, 94088, is denominated Am81C471/478. This color palette uses a 256X18-(24) color look-up table and a 15X18(24) overlay register and can display 271 colors. In this device, the output from either the color look-up table or the overlay register (which may be considered as another look-up table) is provided to the digital to analog converters to generate red, green and blue drive signals. The circuit does not, however, have the capability of combining information from the color look-up table with information from the overlay register and using the resulting combined information to generate the analog drive signals. It is desirable to be able to provide a significantly increased number of displayable colors without a corresponding substantial increase of the size of the memory required for the color look-up table.

We will describe apparatus to increase the number of colors displayable by a color palette circuit without a proportional increase in the size of the memory required.

We will describe apparatus utilizing a first and a second color look-up table and providing separate address inputs to the first and second color lookup tables, and utilizing combining means to combine the outputs of the first and second look-up tables with the resulting outputs of the combining means provided to a plurality of digital-to-analog converter circuits to provide analog outputs, the combinations of which may be utilized by external circuitry to generate color pixels.

We will also describe color palette circuit capable of producing displayable colors in excess of the number of storage locations may be provide by utilizing a color bit map to address locations in a color look-up table, the output of which is provided to combining means and in addition providing a second input to the combining means from a saturation bit map, with the output of the combining means being converted by digital-to-analog converter circuits to provide the analog drive signals for creating a color pixel.

We will also describe a color palette circuit which produces increased number of displayable colors without an increase in the memory storage

locations by utilizing a first input from a color bit map to address locations of a color look-up table and a second input from an intensity bit map which provides an input to a plurality of combining circuits. Each of the combining circuits includes a second input for receiving information from the color look-up table and the combined results of the information from the intensity bit map and the color bit map are after being combined in the combining means converted to an analog circuit by digital-to-analog converter circuitry.

We will also describe as a variation on the immediately preceding color palette circuit an intensity look-up table is provided for receiving information from the intensity bit map and the output of the intensity look-up table is provided to the combining means, thus achieving a significantly increased number of displayable colors without a corresponding large increase in the number of storage locations required.

We will also describe gamma correction look-up tables between the combining circuits and the digital to analog conversion circuits, these modifications providing adjustments to compensate for non-linearity of the luminosity of the display device, which may be for example a cathrode ray tube monitor, as a function of the analog current input or drive voltage to the display device.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the present invention will become apparent from the study of the specification and drawings in which:

Figure 1 illustrates, in block diagram form, a typical prior art color palette circuit;

Figure 2a illustrates the first embodiment of the present invention;

Figure 2b illustrates mathematically the general case where first and second memories are utilized to increase to total number of displayable colors;

Figure 3 illustrates a second embodiment of the present invention wherein the displayable color is generated using an input from a color bit map and information from a saturation bit map where the combining means are adders;

Figure 4 illustrates a third embodiment of the present invention wherein the displayed color is generated using input from a color bit map and an intensity bit map where the combining means are multipliers;

Figure 5 illustrates a fourth embodiment of the present invention in which information from a color look-up table and an intensity look-up table is digitally combined to generate the color to be displayed;

Figure 6 illustrates a fifth embodiment of the present invention in which the color to be displayed is determined by analogically combining (by multiplication), in output digital-to-analog converters, information from a color look-up table with analog information converted from digital information received from an intensity bit map;

Figure 7 illustrates a sixth embodiment of the present invention wherein the color to be displayed is generated by analog multiplication of color information from a color look-up table and intensity information from an intensity look-up table;

Figure 8 illustrates a seventh embodiment of the present invention wherein gamma correction look-up tables are utilized in conjunction with color information from a color look-up table and intensity information from an intensity bit map (with multipliers used to combine the color information with the intensity information) to generate the color to be displayed;

Figure 9 illustrates an eighth embodiment of the present invention in which gamma correction is provided in conjunction with the combined output from first and second color look-up tables (where the combining is achieved using adder circuits) to generate the color to be displayed;

Figure 10 illustrates a ninth embodiment of the present invention wherein gamma correction is provided in conjunction with a system utilizing the combined information from a color look-up table and an intensity look-up table (where the combining is achieved using multiplier circuits) to generate the color to be displayed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention is illustrated in Figure 2a. As illustrated in Figure 2a, color palette circuit 16 receives color information from a video bit map, not shown, over bus 17 which, as indicated by the number 12 adjacent to the slash, includes twelve lines for providing twelve bits of information to color palette circuit 16. Color palette circuit 16 includes a first color look-up table indicated by reference character 18, also denoted in block diagram form as color look-up table "A". Color look-up table 18 includes 256 storage locations each having a capability of storing 24 bits of information. Color palette circuit 16 also includes a second color look-up table indicated by reference character 19, and denominated within the block as color look-up table "B". Color look-up table 19 includes 16 storage locations, each having the capability of storing 24 bits of information. Color look-up tables 18 and 19 may preferably be RAM solid state memory devices of the type utilized in the

prior art. The information loaded into these color look-up tables is provided from an external source (not shown) and the loading is performed in the same manner as utilized in the prior art. For addressing color look-up table 18, eight of the twelve bits from bus 17 are provided to an address input of color look-up table 18. The remaining four of the twelve lines in bus 17 are coupled to an address input of color look-up table 19 for selecting addresses in color look-up table 19. The outputs from color look-up table 18 and color look-up table 19 are combined by combining circuit means which may be, for example, digital adding circuits or digital multiplying circuits. In the embodiment illustrated in Figure 2a, digital adder 20 is provided for combining the red color component outputs from color look-up table 18 and color look-up table 19; digital adder 21 is utilized to add the resulting outputs from the addressed storage location in color look-up table 18 and the addressed storage location in color look-up table 19 for generating the green color component of the color to be displayed; and similarly digital adder circuit 22 combines the output from color look-up table 18 and color look-up table 19 to generate a digital signal indicative of the blue component of the color of the pixel to be displayed. The sum of the digital information received by digital adder 20 is provided from an output thereof over bus 23 to the digital-to-analog converter 24 which converts the digital information received over bus 23 to an analog signal which is available at terminal 25. Similarly, the output from digital adder 21 is provided to digital-to-analog converter 26 over bus 27 and an analog signal, having a magnitude representative of the digital signal received over bus 27, is provided at output terminal 28. In similar fashion, the resulting digital sum of the portions of the addressed storage locations of color look-up table 18 and color look-up table 19 which are provided to digital adder 22 generate a digital sum which is provided at an output of digital adder 22 over bus 29 to digital-to-analog converter 30 which converts the received digital signal into an analog value representative of the digital information and provides this analog signal at terminal 31. The output from each of the adder circuits (20, 21 and 22) is truncated by one bit.

Color palette circuit 16, by utilizing color look-up table 18 and color look-up table 19 in conjunction with digital adders 20, 21 and 22, permits the display of 4,096 unique colors, achieved by the input of twelve bits of information from the video bit map. However, in contrast to the prior art, color palette circuit 16 requires memory means having a total of 272 addressable storage locations, whereas in the prior art utilizing a single memory means, in order to generate 4,096 unique displayable colors, 4,096 storage locations in a memory means would be required. Thus it will be appreciated that utilizing a plurality of memory means to store color information significantly reduces the overall total storage locations required and hence the space required on an integrated circuit device, for example, on which a color palette circuit is implemented.

Figure 2b illustrates a simplified example for a circuit of the type illustrated in Figure 2a. In this simplified example, color palette circuit 36 will provide the number 2^{a+b} unique colors at output line 37 from combining means 38 when combining means 38 is a multiplier. A first memory, denominated memory A and indicated by reference character 39, includes 2^a storagelocations for storing digital information which is loaded therein from a source not shown. A second memory, memory B, indicated by reference character 40, includes 2^b storage locations for storing digital information. Memory A receives at an address input over bus 41, which includes "a" number of lines of address information to uniquely identify one of the 2^a storage locations. In response to receipt of an address signal memory A provides the information stored in the selected storage location to combining means 38 over line 42. Similarly, memory B, which includes 2^b storage locations, receives address information over bus 43, which includes "b" number of lines to uniquely identify any one of the 2^b storage locations in memory B. The information contained in a selected storage location in memory B is provided at an output of memory B and transferred over line 44 to an input of combining means 38. The identity of the storage location in memory A and memory B to be addressed is provided over bus 45, a parallel bus having individual lines equal in number to a+b. It will of course be appreciated that although the digital address information is provided in the illustration in Figure 2b from a single bus 45 which is subdivided into bus 41 and 43, separate input buses not previously combined may provide the address information. In the prior art, to display the 2^{a+b} individual colors required a single memory $_{means}$ having 2^{a+b} storage locations.

In the prior art, for example as illustrated in Figure 1, the determination of the color pixel to be generated by addressing a storage location within color look-up table 3 came from a predefined video bit map. In the first embodiment of Applicant's invention, as illustrated in Figure 2a, the number of displayable colors is increased without an equal increase in the number of storage locations by dividing the number of bus inputs among memory means 18 and memory means 19, and combining the outputs using combining means and thereafter converting the digital result to an analog value.

An alternative embodiment for providing an in-

creased number of displayable colors without increasing the size of the storage element required is illustrated as the second embodiment of Applicant's invention, shown in Figure 3. Color palette circuit 49 receives color information over bus 50, which includes eight lines, from a color bit map (not shown). A second input to color palette circuit 49 is provided from a saturation bit map (also not shown) over bus 51, having four lines. For a pixel to be displayed, the first portion of the information which determines the color of the to-be-displayed pixel is identified by addressing one of the 256 storage locations in color look-up table 52, which may be for example RAM memory, which in this particular embodiment includes 24 bits of information in each of the 256 storage locations. It will of course be appreciated that the number of storage locations provided in the memory means, as well as the number of bits of information storable in any storage location, may be varied to suit the needs of the particular system. The information stored in the 256 storage locations of color look-up table 52 is loaded from an external source, not shown, and the predetermined information in the storage locations in conjunction with the information received from the saturation bit map determine the color which will be displayed. For each selected storage location in color look-up table 52, eight bits of red, eight bits of green and eight bits of blue color information are provided, with the red color information being provided over bus 53 to a first input to red adder 54, eight additional bits of information for the green component of the color is provided from the selected storage location in color look-up table 52 over bus 55 to one of the inputs of green adder 56. Similarly, eight bits of information indicative of the blue component of the color to be displayed is provided over bus 57 to one input of blue adder 58. To each of a second input of red adder 54, green adder 56 and blue adder 58 information is provided over bus 51 to define a saturation level, which in this particular embodiment is the same for each of the foregoing named adder circuits. In addition, the combining circuits (54, 56 and 58) may be separately programmable from an external source so that the digital operation which they are performing may be modified under program control. Returning to the particular embodiment of color palette circuit 49, the result of the digital addition of the information received by red adder 54 over bus 53 and bus 51, is provided over bus 59, having eight lines, to DAC digital to analog converter 60 which converts the digital information received over bus 59 to an analog signal which is provided at output terminal 61. The least significant bit resulting from the addition in red adder 54 is truncated. The resulting digital signal provided at the output of green adder 56 is provided by bus 62, having eight bits, to digital to analog converter 63 which converts the digital information received over bus 62 to an analog signal which is provided at output terminal 64. The least significant bit of the sum generated by green adder 56 is truncated, therefor only an eight bit output is provided by green adder 56. Similarly, the result of the digital addition in blue adder 58 is provided over bus 65 to digital to analog converter 66 which converts the digital information into an analog signal which is provided at output terminal 67. Truncation of the least significant bit from blue adder 58 is performed to provide an eight bit output from blue adder 58.

With the configuration of color palette circuit 49 the maximum number of uniquely identified color pixels which may be generated using this circuit is equal to 4,096. Alternative embodiments for color palette circuit 49 include increasing the number of bits of information provided by the saturation bit map, increasing the number of bits included in each of the storage locations in color look-up table 52, and/or increasing the number of storage locations in color look-up table 52. Yet another alternative embodiment for color palette circuit 49 involves the inclusion of a gamma correction look-up table between each of the combining means (red adder 54, green adder 56 and blue adder 58) and their respective, associated digital to analog converter. The use of gamma correction look-up tables is also described in connection with the seventh, eighth and ninth embodiments of the invention. As described previously, as well as subsequently, when the luminosity of the display device used in conjunction with the color palette circuit is non-linear with respect to the applied drive voltage or drive current, a more accurate color display is achieved when gamma correction is utilized.

A third embodiment of the present invention is illustrated in Figure 4. In the third embodiment, color palette circuit 70 utilizes a first input from a color bit map (not shown) and a second input from an intensity bit map (also not shown) to define colors to be displayed. Color palette circuit 70 utilizes color look-up table 71 which includes 64 addressable storage locations, each capable of storing 24 bits of information. The characteristics for each color to be defined by the storage locations within color look-up table 71 are loaded into color look-up table 71 from an external source, not shown. Information from the color bit map is utilized to select a predetermined storage location within color look-up table 71 via bus 72, having six lines, which is connected to the address input of color look-up table 71. Upon selection of an address within color look-up table 71, the information in eight of the 24 locations is transmitted over bus 73 to digital multiplier 74 which multiplies that

digital information with the digital information received from intensity bit map, over bus 75, to provide a digital product which is provided over bus 76 to digital-to-analog converter 77 which converts the received digital information to an analog signal which is provided at terminal 78. The resultant analog signal at terminal 78 is used in the generation of the red component of a color pixel to be displayed. In similar fashion, another eight bits from the addressed storage location in color look-up table 71 is provided over bus 79 to digital multiplier 80. Concurrently with the presentation of the eight bits of information to digital multiplier 80 from color look-up table 71, a second input to digital multiplier 80 over bus 75, when multiplied with the digital information received over bus 79 produces a digital product at its output, which product is provided over bus 81 to digital-to-analog converter 82 which converts the received digital information into an analog signal which is provided at terminal 83. To generate the blue component of the color pixel, eight bits of information are provided to digital multiplier 84 over bus 85 from the addressed location in color look-up table 71. The product of the information received by digital multiplier 84 from bus 85 and bus 75 is provided via bus 86 to digital-to-analog converter 87 which converts the digital information into an analog signal which is provided at terminal 88. It will be appreciated that the multiplication of six bits times eight bits produces a product having fourteen bits. In color palette circuit 70, the output of red multiplier 74, green multiplier 80 and blue multiplier 84 are truncated to eight bits by dropping the six least significant bits. By utilizing color palette circuit 70, the maximum number of unique displayable colors is 4,096. Modifications to color palette circuit 70 may include increasing the number of storage locations in the color look-up table, and increasing the bits of information provided from the intensity bit map. The embodiment of the invention illustrated in Figure 4 is particularly desirable because data in the respective bit maps can be conveniently organized to represent chroma and intensity information.

The fourth embodiment of the present invention is illustrated in Figure 5. Color palette circuit 91, utilizes an input from a color bit map and an intensity bit map. As will be appreciated by comparing Figure 4 with Figure 5, in Figure 5 a number of circuit elements are the same as those utilized in Figure 4. More particularly the commonality includes color look-up table 71, digital multipliers 74, 80 and 84, and digital-to-analog converters 77, 82, and 87. In addition to the circuit in Figure 4, color palette circuit 91 has an intensity look-up table, indicated by reference character 92, having 64 addressable storage locations, each capable of storing six bits of information. The information stored in intensity look-up table 92 is loaded from an external source (not shown) using conventional circuitry (also not shown). Information from the intensity bit map is provided over bus 75 to the address input of intensity look-up table 92. The information stored in a selected storage location in intensity look-up table 92 is provided by bus 93 to an input on each of digital multiplier circuits 74, 80 and 84. Color palette circuit 91 is particularly advantageous because the intensity look-up table permits performing a transformation on the intensity information.

A fifth embodiment of the present invention is illustrated in Figure 6 wherein a color palette circuit 97 is illustrated. In this embodiment, the color to be displayed is determined by the combination of information from a color bit map (not shown) and an intensity bit map (not shown). Color palette circuit 97 includes color look-up table 98, which may be any form of memory device, which preferably includes, for this embodiment, 64 addressable storage locations, each capable of storing 24 bits of information. The information regarding the displayable colors is loaded into color look-up table 98 by conventional means and using conventional circuitry. For addressing the storage locations in color look-up table 98, bus 99 having 6 individual lines for providing address information is connected to an address input of color look-up table 98. In this embodiment, multiplying digital-to-analog converter circuits are utilized for combining information received from color look-up table 98 and information received from an intensity bit map. More particularly, multiplying digital-to-analog converter circuit 100 converts the information received and provides at output terminal 101 an analog signal indicative of the drive to be provided for the red component of the color pixel to be displayed. Similarly, multiplying digital-to-analog circuit 102 converts received information into an analog signal to provide an output terminal 103 information for the green drive signal. The blue component of the pixel to be displayed is generated by multiplying digital-to-analog converter circuit 104 which generates, based upon received input, an analog signal at output terminal 105. When a storage location in color look-up table 98 is addressed, 8 bits of information are provided over bus 106 to a digital input of multiplying digital-to-analog converter circuit 100. Information in an additional 8 cells within the storage location addressed is provided over bus 107 to the digital input of multiplying digital-to-analog converter circuit 102 and the information in another 8 storage cells within the addressed storage location is provided over bus 108 to multiplying digital-to-analog converter circuit 104. The information provided over buses 106 through 108 is

utilized to provide a first portion of the information which will be used to ultimately generate an analog signal on output terminals 101, 103 and 105 for generating a color pixel. The source of the second signal component utilized in generating the color pixel to be displayed is an intensity bit map. This second signal component is generated by converting digital information received from the intensity bit map over bus 109 and provided to the input of digital-to-analog converter circuit 110. The analog signal generated by digital-to-analog converter circuit 110, which is non-multiplying digital-to-analog converter circuit, is provided, by line 111 to multiplying digital-to-analog converter circuit 100, by line 112 to multiplying digital-to-analog converter circuit 102 and by line 113 to multiplying digital-to-analog converter circuit 104. In response to receipt of an input from color look-up table 98 and digital-to-analog converter circuit 110, these combined signals produce the analog drive signals at output terminals 101 for the red color component, 103 for the green color component and 105 for the blue color component. Color palette circuit 97 is particularly advantageous because it can be implemented with inexpensive multiplying digital to analog converters.

The sixth embodiment of the present invention is illustrated in Figure 7. As will be appreciated by comparing color palette circuit 97 (in Figure 6) with color palette circuit 115 in Figure 7, certain circuit elements utilized are the same and therefore are indicated by the same reference characters in both circuits. To allow a transformation on the intensity information on intensity look-up table 116 is provided. Intensity look-up table 116 may take the form of any convenient, well known memory means and in this embodiment includes 64 storage locations, each having the ability to store 6 bits of information. The information to be stored in the 64 storage locations of intensity look-up table 116 is loaded by the user from an external source, not shown, and by conventional means. The intensity information received from the intensity bit map is provided over bus 109 to the address input of intensity look-up table 116. When a storage location in intensity look-up table 116 is addressed, the information included in that storage location is provided over bus 117 to digital-to-analog converter circuit 110, which is a non-multiplying digital-to-analog converter circuit. The analog signal produced at the output of digital-to-analog converter circuit 110 is coupled by a line 111 to multiplying digital-to-analog converter circuit 100. The same signal is also coupled to multiplying digital-to-analog circuit 102 by line 112 and similarly is coupled to multiplying digital-to-analog converter circuit 104 by line 113. Color palette circuit 115 provides the advantages over, for example color palette circuit 97 illustrated in Figure 6, in that it allows a transformation on the intensity information. In color palette circuit 97 and color palette circuit 115 the output generating circuitry, and more particularly multiplying digital-to-analog converter circuits 100, 102 and 104, utilize multiplication of the converted analog signals to generate an output voltage at their respective output terminals. It will of course be appreciated that instead of multiplying the generated analog signals, these output generating circuits could, for example, analogically combine the received input signals by adding them together.

The seventh embodiment of the present invention, which is illustrated in Figure 8, comprises color palette circuit 121. In color palette circuit 121 a number of the circuit elements are the same as those utilized in color palette circuit 70 (illustrated in Figure 4) and accordingly like circuit components are indicated by the same reference character used in Figure 4. In some situations it is desirable to provide gamma correction in color palette circuits to compensate for non-linearity of the luminosity of the display device. In color palette circuit 121, gamma correction is achieved by including gamma correction look-up tables, one for each color component being produced, for example, red gamma correction look-up table 122, green gamma correction look-up table 123 and blue gamma correction look-up table 124. In this embodiment each of the gamma correction look-up tables includes 256 separately addressable storage locations, each storage location being 8 bits wide. These gamma correction look-up tables may be implemented using any suitable memory means, such as for example, solid state memory. The information to be utilized to achieve gamma correction is loaded according to the users requirements from external sources by conventional means, not shown. In operation, the input from the color bit map and the input from the intensity bit map generate an output from each of the digital multiplier circuits 74, 80 and 84. Truncation of the six least significant bits of the product generated by multipliers 74, 80 and 84 is performed to thereby provide only an eight output from these multipliers. Bus 76 couples the output of multiplier circuit 74 to an address input of red gamma correction look-up table 122 defines one of the 256 storage locations within red gamma correction look-up table 122 and the information in the selected storage location is provided over bus 125 to an input of digital-to-analog converter 77 which converts the received digital signal into an analog signal at output terminal 78. The output from digital multiplier 80 is provided over bus 81 to the address input of green gamma correction look-up table 123 and the information in the selected storage location is provided from the output of green gamma correction

look-up table 123 over bus 126 to the input of digital to analog converter circuit 82, which circuit converts the received digital signal into an analog signal which is provided at output terminal 83. Similarly, the output from digital multiplier 84 is supplied to the address input of blue gamma correction look-up table 124 over bus 86 and the information in the selected storage location is transmitted to the input of digital-to-analog converter circuit 87 over bus 127. The received digital signal is converted into an analog voltage which is provided at output terminal 88. Color palette circuit 121 is particularly advantageous when used with systems utilizing color intensity information in the representation of colors.

The eighth embodiment of the present invention is illustrated in Figure 9 and comprises color palette circuit 132. Color palette circuit 132 generates analog signals at output terminals 25, 28 and 31 to define respectively the red, green and blue color components for a pixel to be displayed. The color of the pixel to be displayed is generated from an input over bus 17 from a video bit map and in many respects operates similarly to the first embodiment of the present invention which is illustrated in Figure 2a. The circuit components in Figures 2a and 9 which correspond are indicated by corresponding reference characters. Color palette circuit 132 provides improved color rendition over color palette circuit 16 illustrated in Figure 2a by adding gamma correction to the red, green and blue color components. More particularly, gamma correction look-up table 133 is inserted between digital adder 20 and digital-to-analog converted 24. Bus 23 from digital adder 20 provides the address input to gamma correction look-up table 133 and the information contained in the addressed storage location is provided to digital analog converter 24 over bus 134. To provide color correction for the green component of the pixel to be displayed, gamma correction look-up table 135 has its address input connected to bus 27 and the information in the selected storage location in gamma correction look-up table 135 is provided over bus 136 to the input of digital-to-analog converter 26. And finally, gamma correction look-up table 137 which receives at its address input, via bus 29, addresses for selected storage locations and provides the information contained in the selected storage location, via bus 138, to digital-to-analog converter 30. Color palette circuit 132 provides an additional level of sophistication over color palette circuit 16 since by using color palette circuit 132 it is possible to compensate for non-linearity of the luminosity of display device as a function of the analog drive signals provided to the display device.

Color palette circuit 142, illustrated in Figure 10, is illustrative of the ninth embodiment of the present invention. The red, green and blue color components of a pixel to be displayed are generated using color look-up table 71, intensity look-up table 92, combining circuits 74, 80 and 84, which in this embodiment are digital multiplier circuits, with red, green and blue gamma correction being achieved by the use of red gamma correction look-up table 143, green gamma correction look-up table 144 and blue gamma correction look-up table 145, respectively. The digital information appearing on bus 76 for a to be displayed pixel is coupled to the address input of red gamma correction look-up table 143 and the information in the addressed storage location is transferred to digital-to-analog converter 77 over bus 146. To achieve green gamma correction, the digital signal on bus 81 is provided to the address input of green gamma correction look-up table 144 and the resulting output from the selected storage location is provided to digital-to-analog converter 82 over bus 147. Blue gamma correction information stored in blue gamma correction look-up table 145 is provided over bus 148 to digital-to-analog converter 87, the information transferred being that information which is included in the storage location in blue gamma correction look-up table 145 which is addressed based upon the digital information coupled to the address input of blue gamma correction look-up table 145 over bus 86. By comparing color palette circuit 91 with color palette circuit 142 it will be appreciated that a number of the circuit elements are common, and accordingly are identified by like referenced characters. The gamma correction look-up tables utilized in color palette circuit 142 may be comprised of any suitable memory means, such as, for example, solid state memory. The information to be stored in the storage locations within each of the gamma correction look-up tables is determined by other parameters in the system in which color palette circuit 142 will be utilized. Color palette circuit 142 provides greater flexibility in the representation of pixels in the bit map.

The foregoing is illustrative of several embodiments for practicing the invention. It is of course understood that the invention is not limited by the above description, but only by the following claims.

Claims

1. A color palette circuit for receiving digital information from a video bit map and converting said digital information to analog information having n components for use by other means to create a color pixel, said circuit comprising:

a first memory means having a plurality of storage locations for storing digital information, said first memory means having an address input for

receiving digital information from said video bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said video bit map to select storage locations, said first memory means having n output terminals for providing thereat n portions of digital information stored in selected addresses, and means coupling said n portions of said digital information in selected addresses to respective ones of said n output terminals;

a second memory means having a plurality of storage locations for storing digital information, said second memory means having an address input for receiving digital information from said video bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said video bit map to select storage locations, said second memory means having n output terminals for providing thereat n portions of digital information from selected addresses, and means coupling said n portions of said digital information in a selected address to respective ones of said n output terminals;

n digital combining circuits, each having first and second input terminals and an output terminal, and each of said n digital combining circuits including circuit means which is responsive to the receipt of signals at said first and second input terminals to produce and provide at said output terminal a signal which is the result of combining signals received at said first and second input terminals;

means coupling said first input terminal of each of said n digital combining circuits to an output terminal of said first memory means;

means coupling said second input terminal of each of said digital combining circuit means to an output terminal of said second memory means;

n digital to analog conversion circuits, each having an input terminal for receiving signals from an associated one of said n digital combining circuits and an output terminal for providing an analog signal in response to receipt of a digital signal; and

means coupling the input terminal of each of said digital to analog conversion circuits to the output terminal of its associated digital combining circuit.

2. A color palette circuit according to Claim 1, wherein said digital combining circuits are adder circuits.

3. A color palette circuit according to Claim 1, wherein said digital combining circuits are multiplier circuits.

4. A color palette circuit according to any of Claims 1-3, wherein said means coupling the input terminal of said digital to analog conversion circuit to the output of its associated digital combining circuit includes circuit means for providing gamma correction.

5. A color palette circuit having a first input terminal for receiving digital information from a color bit map and a second input terminal for receiving digital information from a saturation bit map and in response thereto generating analog information having n components for use by other means to generate a color pixel, said circuit comprising:

a memory means having a plurality of storage locations for storing digital information indicative of displayable colors, said memory means having an address input coupled to said first input terminal for receiving digital information from said color bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said color bit map to select storage locations, said memory means having n output terminals for providing thereat n portions of digital information stored in selected addresses, and means coupling said n portions of said digital information in selected addresses to respective ones of said n output terminals;

n digital combining circuits, each having first and second input terminals and an output terminal, and each of said n digital combining circuits including circuit means which is responsive to the receipt of signals at said first and second input terminals to produce and provide at said output terminal a signal which is the result of combining signals received at said first and second input terminals;

means coupling the first input terminal of each of said digital combining circuits to an associated one of said n output terminals of said memory means;

means coupling said second input terminal of said color palette circuit to said second input terminal of each of said n digital combining circuits;

n digital to analog conversion circuits, each having an input terminal for receiving signals from an associated one of said digital combining circuits and an output terminal for providing an analog signal in response to receipt of a digital signal; and

means coupling the input terminal of each digital to analog conversion circuit to the output terminal of its associated digital combining circuit.

6. A color palette circuit according to Claim 5, wherein said digital combining circuits are adder circuits.

7. A color palette circuit according to any of Claims 5 or 6, wherein said means coupling the input terminal of each digital to analog conversion circuit to the output terminal of its associated digital combining circuit includes circuit means for providing gamma correction.

8. A color palette circuit having a first input terminal for receiving digital information from a color bit map and a second input terminal for receiving digital information from an intensity bit map and in response thereto generating analog information

having n components for use by other means to generate a color pixel, said circuit comprising:

a memory means having a plurality of storage locations for storing digital information indicative of displayable colors, said memory means having an address input coupled to said first input terminal for receiving digital information from said color bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said color bit map to select storage locations, said memory means having n output terminals for providing thereat n portions of digital information stored in selected addresses, and means coupling said n portions of said digital information in selected addresses to respective ones of said n output terminals;

n digital combining circuits, each having first and second input terminals and an output terminal, and each of said n digital combining circuits including circuit means which is responsive to the receipt of signals at said first and second input terminals to produce and provide at said output terminal a signal which is the result of combining signals received at said first and second input terminals;

means coupling the first input terminal of each of said digital combining circuits to an associated one of said n output terminals of said memory means;

means coupling said second input terminal of said color palette circuit to said second input terminal of each of said n digital combining circuits;

n digital to analog conversion circuits, each having an input terminal for receiving signals from an associated one of said digital combining circuits and an output terminal for providing an analog signal in response to receipt of a digital signal; and

means coupling the input terminal of each digital to analog conversion circuit to the output terminal of its associated digital combining circuit.

9. A color palette circuit according to Claim 8, wherein said digital combining circuits are multiplier circuits.

10. A circuit according to any of Claims 8-9, wherein said means coupling the input terminal of each digital to analog conversion circuit to the output terminal of its associated combining circuit includes circuit means for providing gamma correction.

11. A color palette circuit having a first input terminal for receiving digital information from a color bit map and a second input terminal for receiving digital information from an intensity bit map and converting said digital information to analog information having n components for use by other means to create a color pixel, said circuit comprising:

a first memory means having a plurality of storage locations for storing digital information, said first memory means having an address input coupled to said first input terminal for receiving digital information from said color bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said color bit map to select storage locations, said first memory means having n output terminals for providing thereat n portions of digital information stored in selected addresses, and means coupling said n portions of said digital information in selected addresses to respective ones of said n output terminals;

a second memory means having a plurality of storage locations for storing digital information, said second memory means having an address input coupled to said second input terminal for receiving digital information from said intensity bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said intensity bit map to select storage locations, said second memory means having an output terminal for providing thereat digital information from selected addresses, and means coupling said digital information in a selected address to said output terminal;

n digital combining circuits, each having first and second input terminals and an output terminal, and each of said n digital combining circuits including circuit means which is responsive to the receipt of signals at said first and second input terminals to produce and provide at said output terminal a signal which is the result of combining signals received at said first and second input terminals;

means coupling said first input terminal of each of said n digital combining circuits to an output terminal of said first memory means;

means coupling said second input terminal of each of said digital combining circuit means to said output terminal of said second memory means;

n digital to analog conversion circuits, each having an input terminal for receiving signals from an associated one of said n digital combining circuits and an output terminal for providing an analog signal in response to receipt of a digital signal; and

means coupling the input terminal of each of said digital to analog conversion circuits to the output terminal of its associated digital combining circuit.

13. A color palette circuit according to Claim 11, wherein said digital combining circuits are multiplier circuits.

14. A color palette circuit according to any of Claims 11-12, wherein said means coupling the input terminal of said digital to analog conversion circuit to the output of its associated digital combining circuit includes circuit means for providing gamma correction.

16. A color palette circuit having a first input termi-

nal for receiving digital information from a color bit map and a second input terminal for receiving digital information from an intensity bit map and in response thereto generating analog information having n components for use by other means to generate a color pixel, said circuit comprising:

a memory means having a plurality of storage locations for storing digital information indicative of displayable colors, said memory means having an address input coupled to said first input terminal for receiving digital information from said color bit map and including circuit means, coupled to said address input, which is responsive to receipt of digital information from said color bit map to select storage locations, said memory means having n output terminals for providing thereat portions of digital information stored in selected addresses, and means coupling said n portions of said digital information in selected addresses to respective ones of said n output terminals;

n digital to analog converting and combining circuits, each having first and second input terminals and an output terminal, and each of said n digital to analog converting and combining circuits including circuit means which is responsive to the receipt of signals at said first and second input terminals to produce and provide at said output terminal an analog signal which is the result of combining signals received at said first and second input terminals;

means coupling the first input terminal of each of said digital to analog converting and combining circuits to an associated one of said n output terminals of said memory means;

a digital to analog conversion circuit having an input terminal and an output terminal;

means coupling said second input terminal of said color palette circuit to said input terminal of said digital to analog conversion circuit; and

means coupling said output terminal of said digital to analog conversion circuit to said second input terminal of each of said n digital to analog converting and combining circuits.

15. A color palette circuit according to Claim 14, wherein said means coupling said second input terminal of said color palette circuit to said input terminal of said digital to analog conversion circuit includes a memory means having a plurality of data storage locations for storing color intensity information.

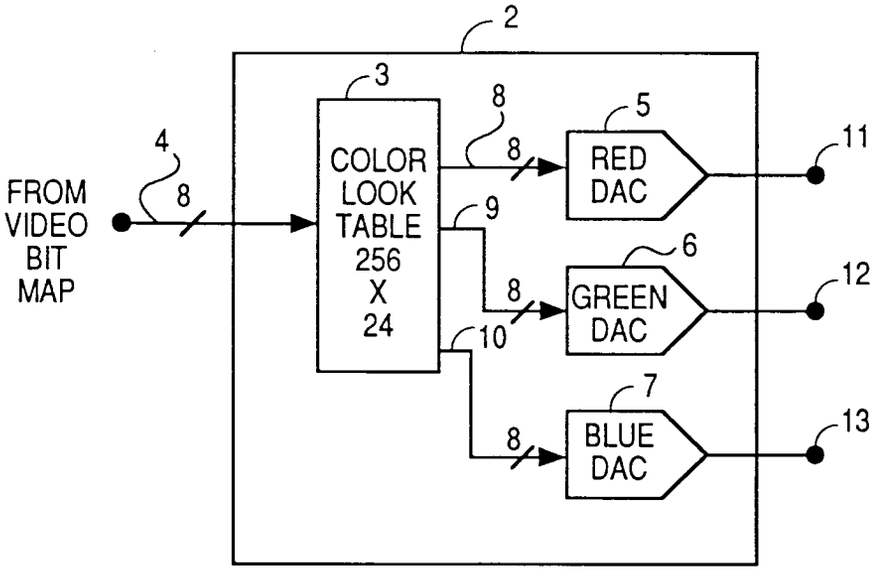


FIG. 1
PRIOR ART

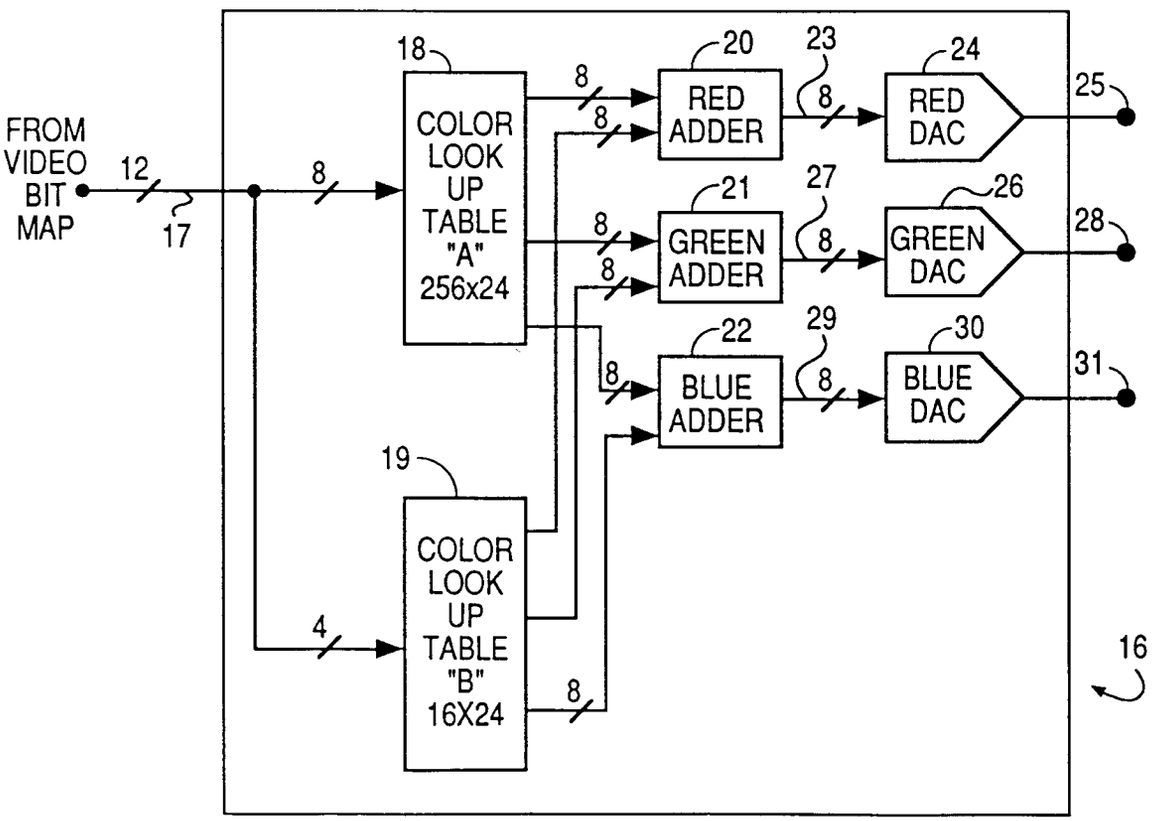
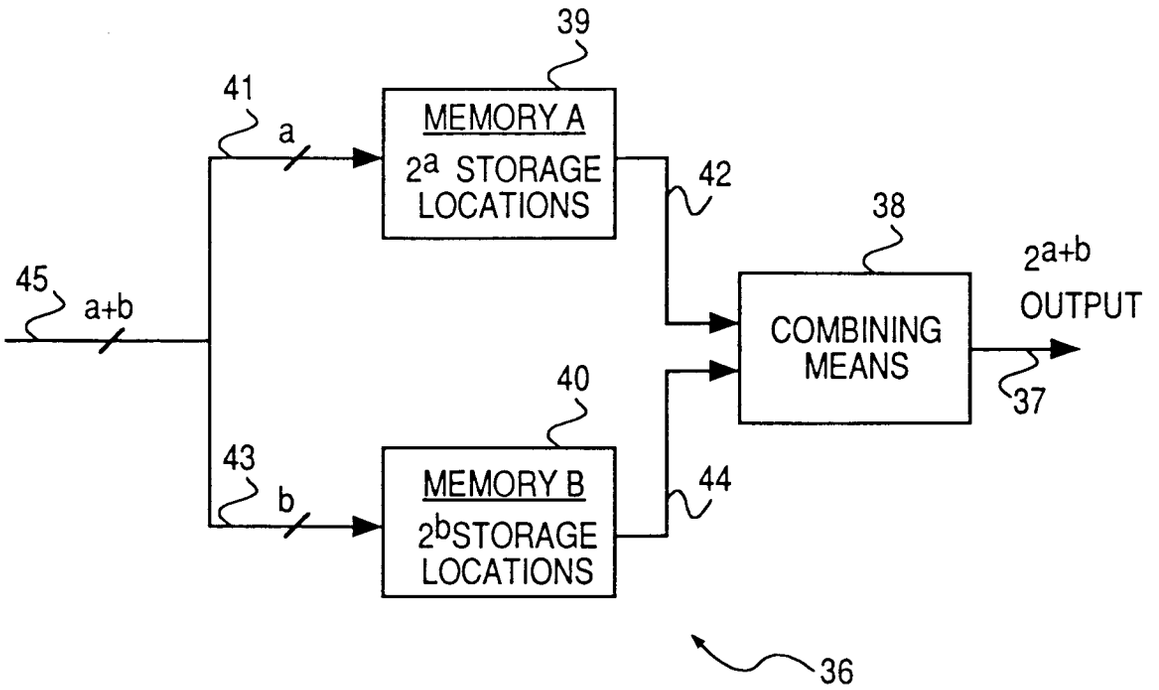


FIG. 2a



a+b = number of address bits at input

POSSIBLE OUTPUT COMBINATIONS = 2^{a+b}

STORAGE LOCATIONS REQUIRED = $2^a + 2^b$

FOR ALL CASES WHERE : 1. $a \geq 1$ and $b \geq 1$ and
2. $a+b > 2$, THEN

$$2^a + 2^b < 2^{a+b}$$

FIG. 2b

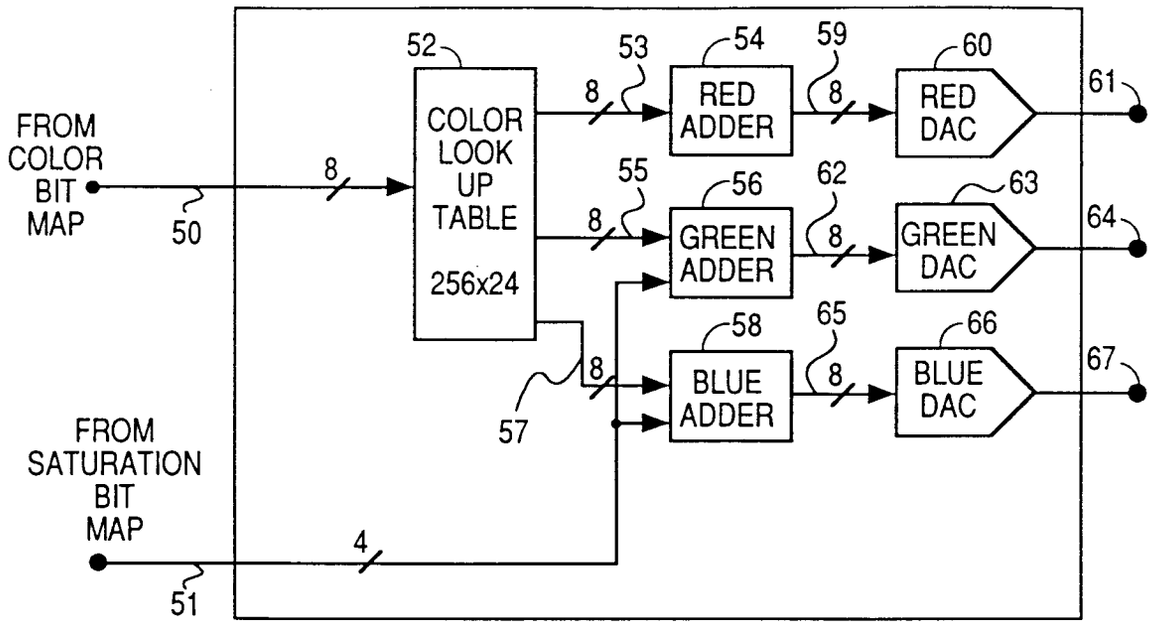

FROM COLOR BIT MAP
50
8
52
COLOR LOOK UP TABLE
256x24
53
8
54
RED ADDER
59
8
60
RED DAC
61
55
8
56
GREEN ADDER
62
8
63
GREEN DAC
64
57
8
58
BLUE ADDER
65
8
66
BLUE DAC
67
FROM SATURATION BIT MAP
51
4
49

FIG. 3

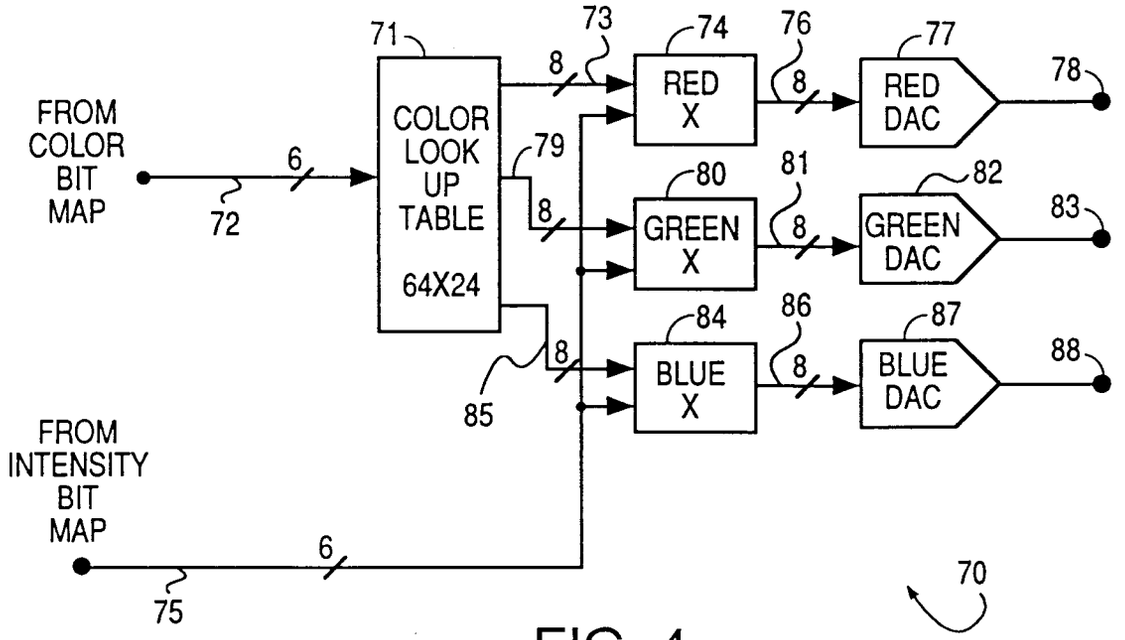

FROM COLOR BIT MAP
72
6
71
COLOR LOOK UP TABLE
64X24
73
8
74
RED X
76
8
77
RED DAC
78
79
8
80
GREEN X
81
8
82
GREEN DAC
83
85
8
84
BLUE X
86
8
87
BLUE DAC
88
FROM INTENSITY BIT MAP
75
6
70

FIG. 4

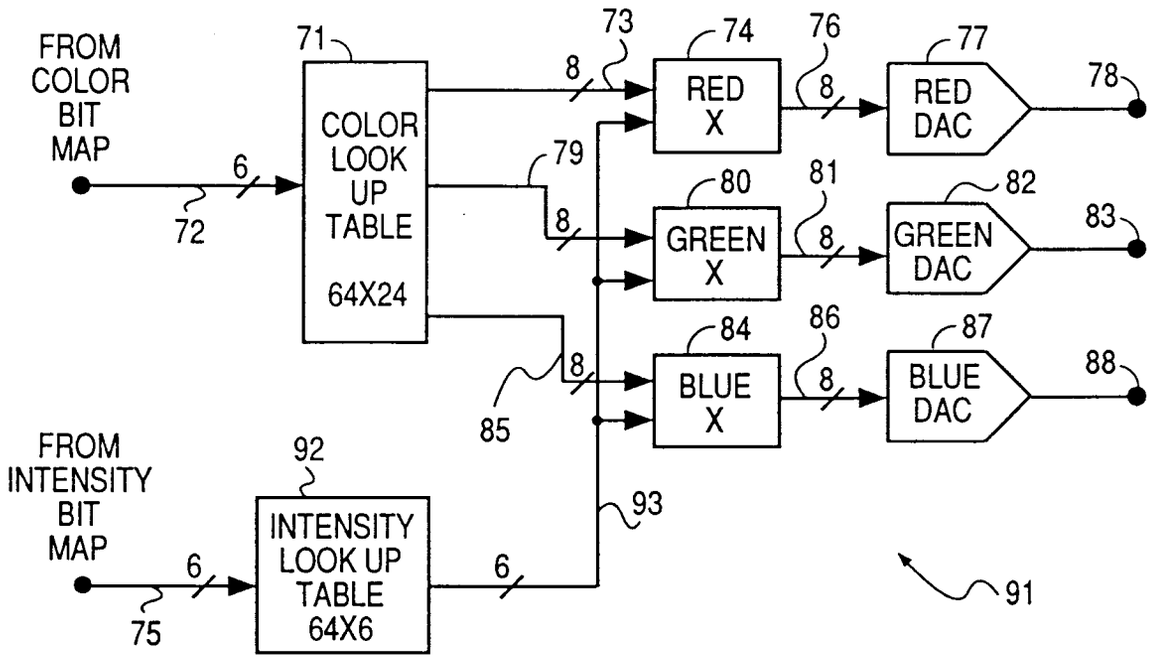

FROM COLOR BIT MAP
71
COLOR LOOK UP TABLE 64X24
72
6
73
8
74
RED X
76
8
77
RED DAC
78
79
8
80
GREEN X
81
8
82
GREEN DAC
83
85
8
84
BLUE X
86
8
87
BLUE DAC
88
FROM INTENSITY BIT MAP
92
INTENSITY LOOK UP TABLE 64X6
75
6
6
93
91

FIG. 5

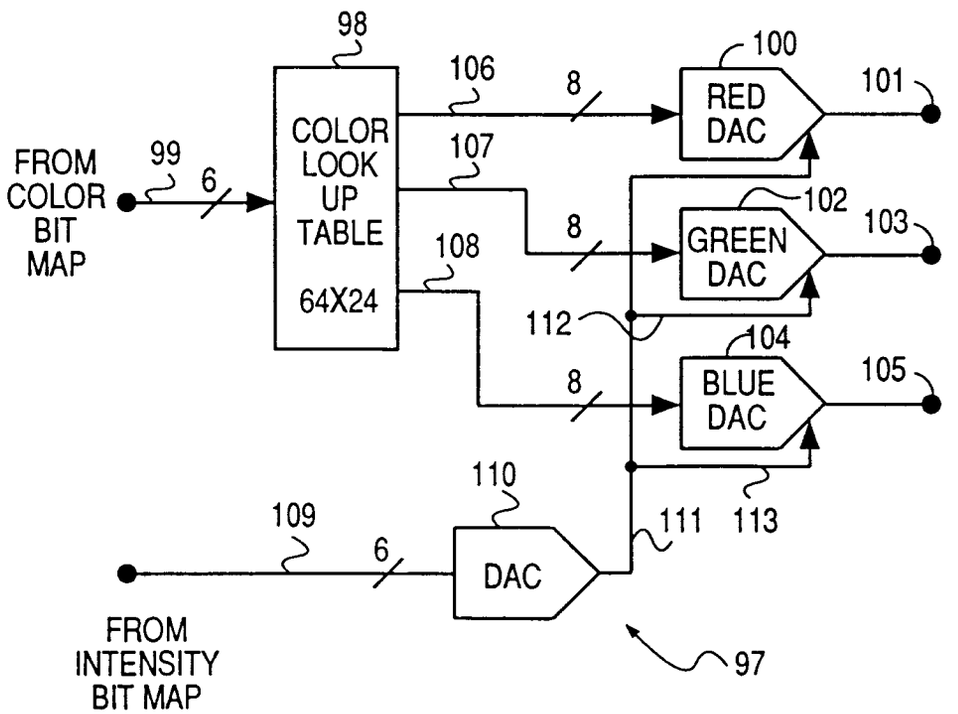

98
FROM COLOR BIT MAP
99
6
COLOR LOOK UP TABLE 64X24
106
8
100
RED DAC
101
107
8
102
GREEN DAC
103
108
112
8
104
BLUE DAC
105
110
109
6
DAC
111
113
FROM INTENSITY BIT MAP
97

FIG. 6

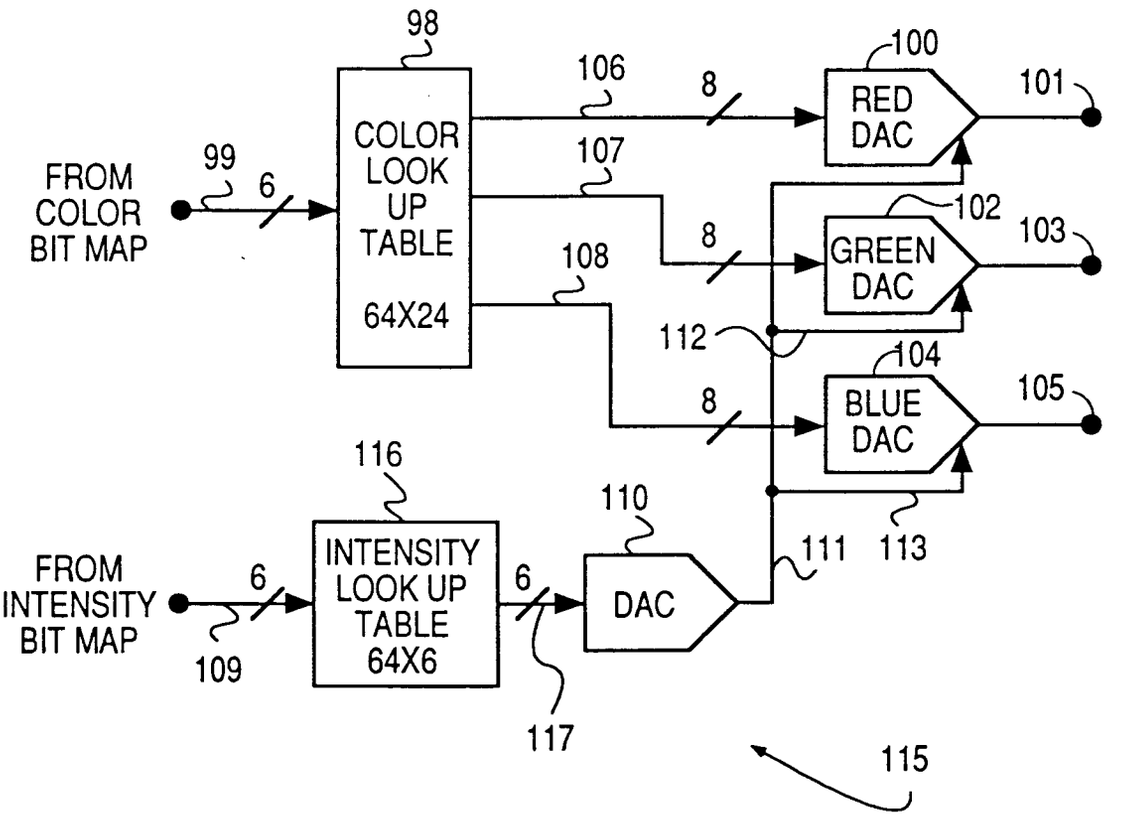

98
COLOR LOOK UP TABLE 64X24
FROM COLOR BIT MAP
99
6
106
107
108
8
8
8
100
RED DAC
101
102
GREEN DAC
103
104
BLUE DAC
105
112
116
INTENSITY LOOK UP TABLE 64X6
FROM INTENSITY BIT MAP
6
109
6
110
DAC
111
113
117
115

FIG. 7

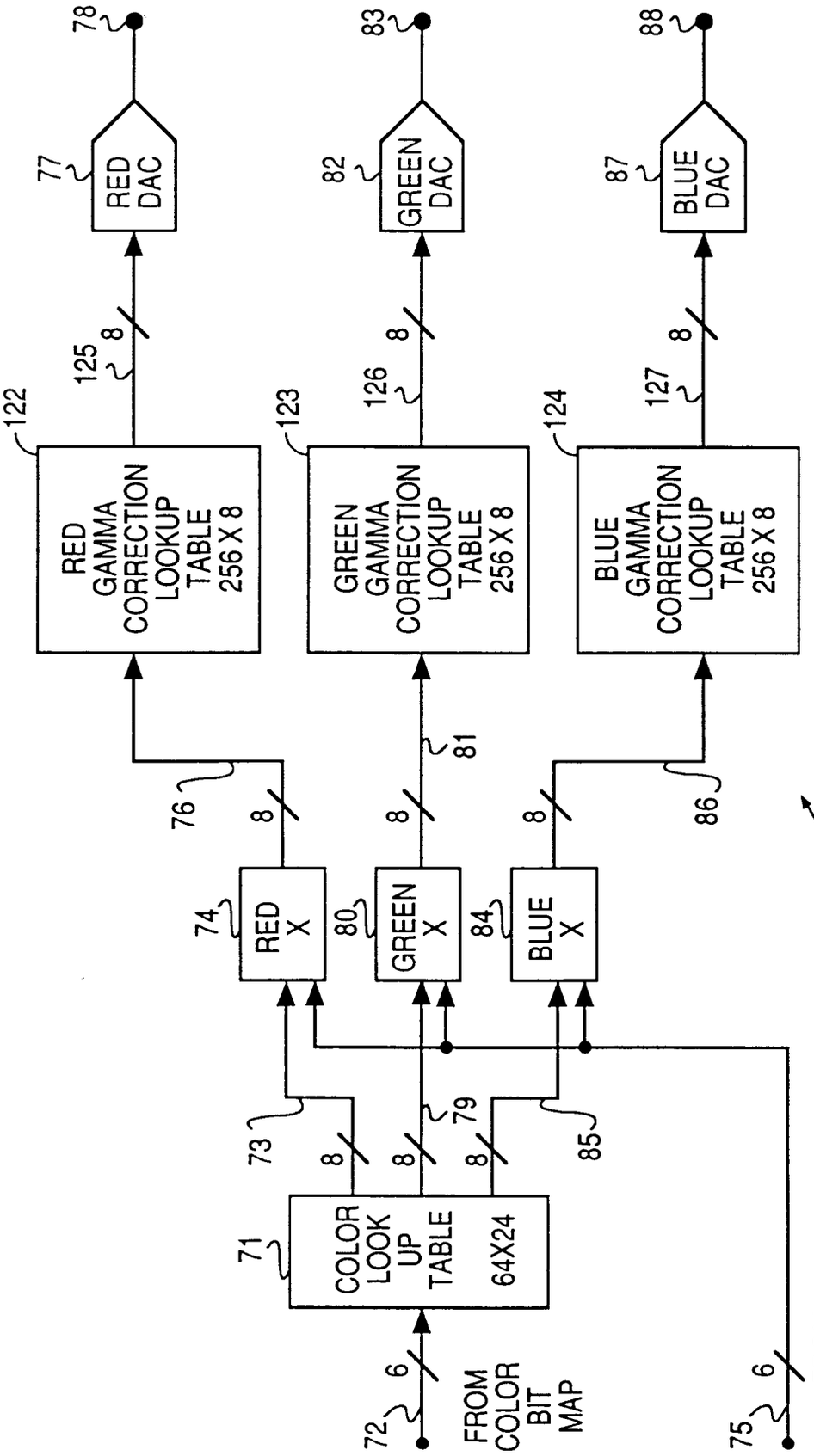

78
83
88
77
RED DAC
82
GREEN DAC
87
BLUE DAC
125
8
126
8
127
8
122
RED GAMMA CORRECTION LOOKUP TABLE 256 X 8
123
GREEN GAMMA CORRECTION LOOKUP TABLE 256 X 8
124
BLUE GAMMA CORRECTION LOOKUP TABLE 256 X 8
76
8
81
8
86
8
74
RED X
80
GREEN X
84
BLUE X
121
73
8
79
8
85
8
71
COLOR LOOK UP TABLE 64X24
72
6
FROM COLOR BIT MAP
75
6
FROM INTENSITY BIT MAP

FIG. 8

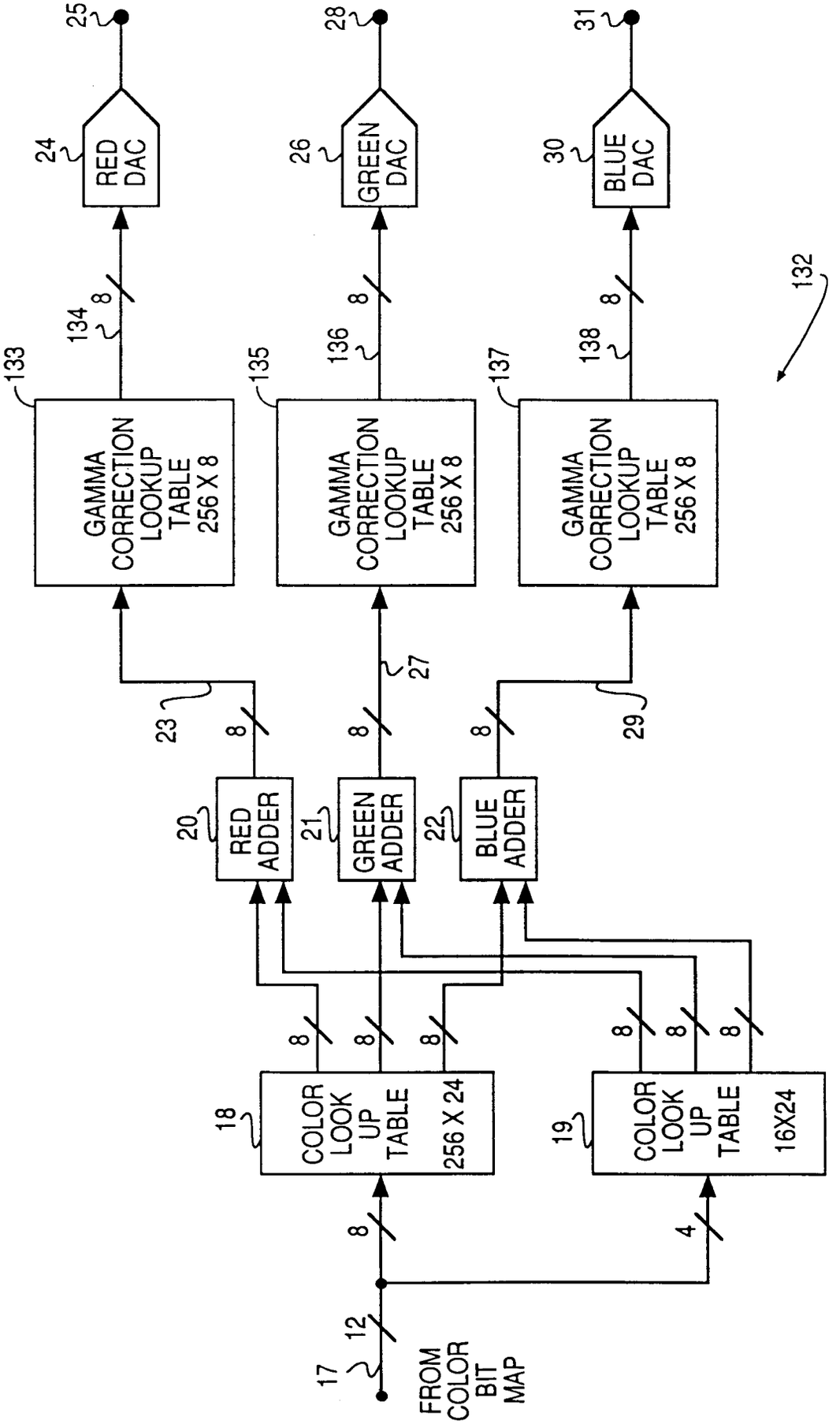

FROM COLOR BIT MAP
17
12
8
4
COLOR LOOK UP TABLE 256 X 24
18
COLOR LOOK UP TABLE 16X24
19
RED ADDER
20
GREEN ADDER
21
BLUE ADDER
22
23
27
29
GAMMA CORRECTION LOOKUP TABLE 256 X 8
133
GAMMA CORRECTION LOOKUP TABLE 256 X 8
135
GAMMA CORRECTION LOOKUP TABLE 256 X 8
137
134
136
138
RED DAC
24
GREEN DAC
26
BLUE DAC
30
25
28
31
132

FIG. 9

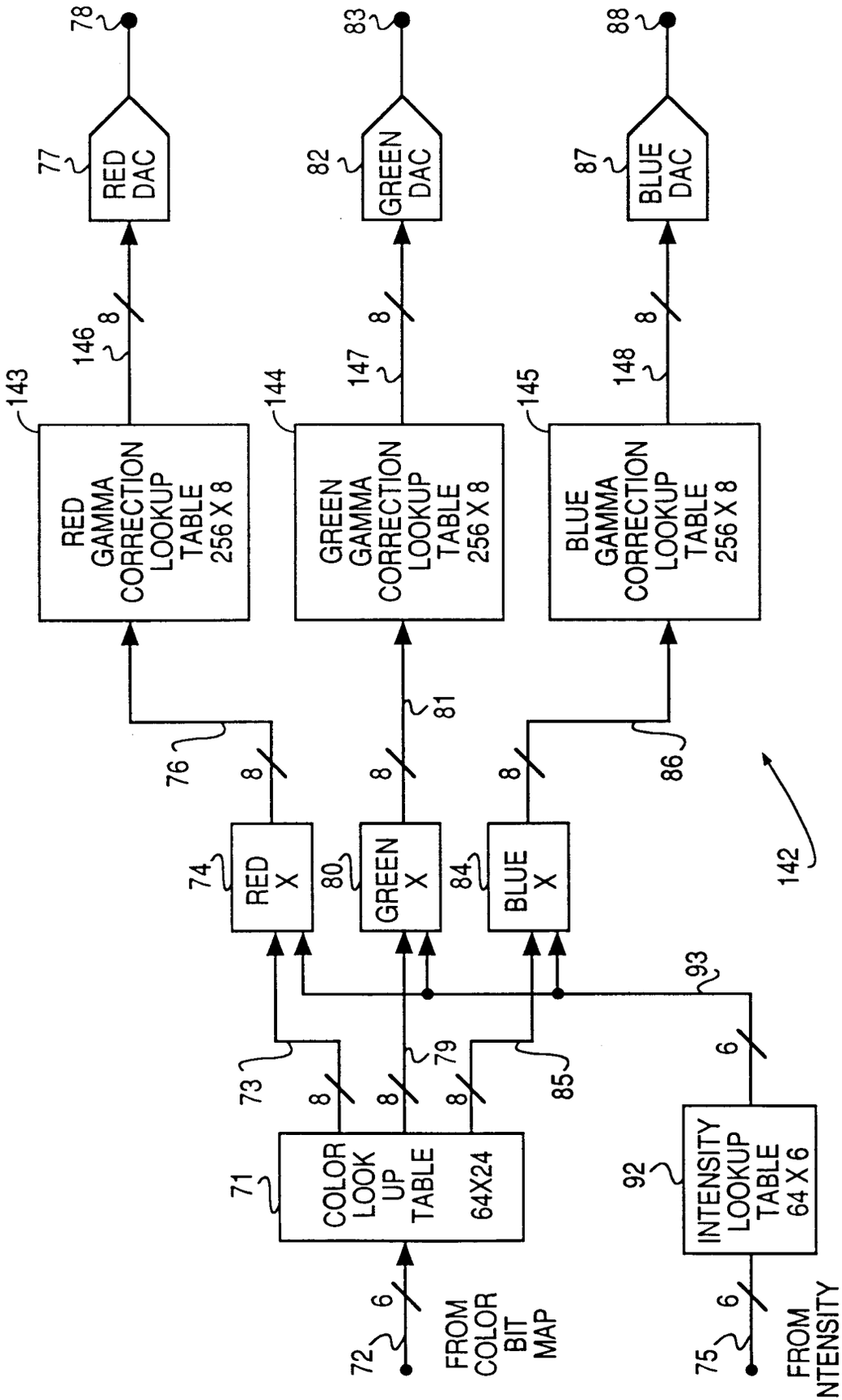

78
83
88
77
RED DAC
82
GREEN DAC
87
BLUE DAC
146
8
147
8
148
8
143
144
145
RED GAMMA CORRECTION LOOKUP TABLE 256 X 8
GREEN GAMMA CORRECTION LOOKUP TABLE 256 X 8
BLUE GAMMA CORRECTION LOOKUP TABLE 256 X 8
76
8
81
8
86
8
74
RED X
80
GREEN X
84
BLUE X
142
93
73
8
79
8
85
8
6
71
COLOR LOOK UP TABLE 64X24
92
INTENSITY LOOKUP TABLE 64 X 6
72
6
FROM COLOR BIT MAP
75
6
FROM INTENSITY BIT MAP

FIG. 10