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Clock with clock adjusting data memory.

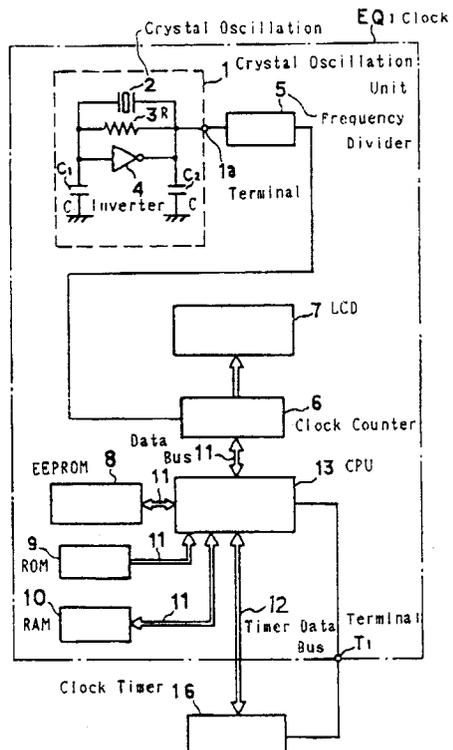
(Constitution) An oscillation circuit (1) has its frequency error stored as clock adjusting data in a memory such as EEPROM (8) or the like during a manufacture process by using a clock timer. The clock adjusting data stored in the memory (8) are adjusted in the adjusting sequence of the clock adjusting program, which is executed for a period of 12 hours.

The fast/slow adjustments are automatically accomplished to a correct time for the constant period by the clock adjusting data adjusted in the adjusting sequence.

(Effects)

It is possible to reduce the number of parts, improve the flexibility for design, standardize the clock circuit, eliminate the fast/slow adjusting member, and simplify the fast/slow adjustments.

FIG. 1



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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 253 227 (EM MICROELECTRONIC-MARIN SA) * page 2, line 1 - page 3, line 4; figure 2 *	1,2	G04G3/02
A	GB-A-2 091 511 (CITIZEN WATCH CO LTD)	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G04G
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	21 December 1993	Exelmans, U	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			