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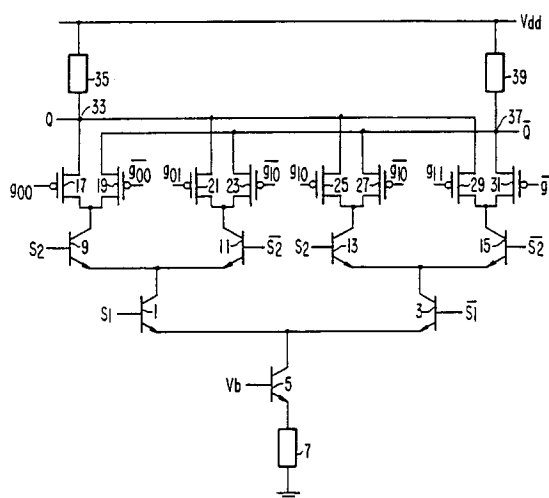
(11) Publication number:

0 511 711 A3

(12)

EUROPEAN PATENT APPLICATION(21) Application number: **92201158.0**(51) Int. Cl.⁶: **H03K 19/173, H03K 19/20,
H03K 19/094, H03K 19/0948**(22) Date of filing: **24.04.92**(30) Priority: **01.05.91 US 695036**(43) Date of publication of application:
04.11.92 Bulletin 92/45(84) Designated Contracting States:
DE FR GB IT(88) Date of deferred publication of the search report:
15.03.95 Bulletin 95/11(71) Applicant: **Philips Electronics N.V.**
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INTERNATIONAAL OCTROOIBUREAU B.V.,
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NL-5656 AA Eindhoven (NL)(54) **Programmable combinational logic circuit.**

(57) A programmable logic circuit for deriving any selected combinational logic function of a plurality of input logic signals, a particular logic function being established by programming signals supplied to the logic circuit. The circuit is a branching tree structure of successive gating levels, each gating level receiving a respective input logic signal and including one or more pairs of logic switches, each such gating switch being a bipolar transistor or a CMOS pair. Each pair of gating switches in a given gating level is coupled to one of the gating switches in the preceding gating level. A programming level following the highest gating level includes respective pairs of logic switches for the respective programming signals, each such pair driving one of the gating switches in the highest gating level. The logic circuit can serve as a prototype which can be programmed and reprogrammed during debugging of a programmable logic device (PLD) in which it is included. All combinational logic functions (AND, OR, XOR, etc.) can be established by appropriate logic values of the programming signals.

**FIG.1****EP 0 511 711 A3**



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Application Number
EP 92 20 1158

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	RADIO FERNSEHEN ELEKTRONIK, vol.26, no.1, January 1977 pages 10 - 24 M. AUER ET AL.: 'Komplexe ECL-Schaltkreise' * page 24, left-hand column; figure 22b *	1	H03K19/173 H03K19/20 H03K19/094 H03K19/0948
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A		4,6	
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A	--- PATENT ABSTRACTS OF JAPAN vol. 9, no. 266 (E-352) (1989) 23 October 1985 & JP-A-60 113 525 (SHARP K. K.) 20 June 1985 * abstract *	5	TECHNICAL FIELDS SEARCHED (Int.Cl.5)
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A	--- GB-A-2 146 863 (FERRANTI PLC) * figure 2 *	1,4,6	
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The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 5 January 1995	Examiner Arendt, M
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	



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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.24, no.5, October 1989, NEW YORK, US pages 1265 - 1270 M. INO ET AL.: '30-ps 7.5-GHz GaAs MESFET Macrocell Array' * figure 2 *	1,4,6	
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The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 5 January 1995	Examiner Arendt, M
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			