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(54) Image information control apparatus and display device.

(57) An image information control apparatus includes :

a. first means for generating and outputting an image information transfer timing signal for controlling a transfer timing of image information ;

b. second means for thinning the image information transfer timing signal transferred from the first means in accordance with an environmental temperature and outputting a thinned image information transfer timing signal ;

c. third means for controlling a voltage waveform upon reception of the image information transfer timing signal ; and

d. fourth means for controlling the third means so that the voltage waveform is kept constant during a period of at least two continuous image information transfer timing signals output from the second means.

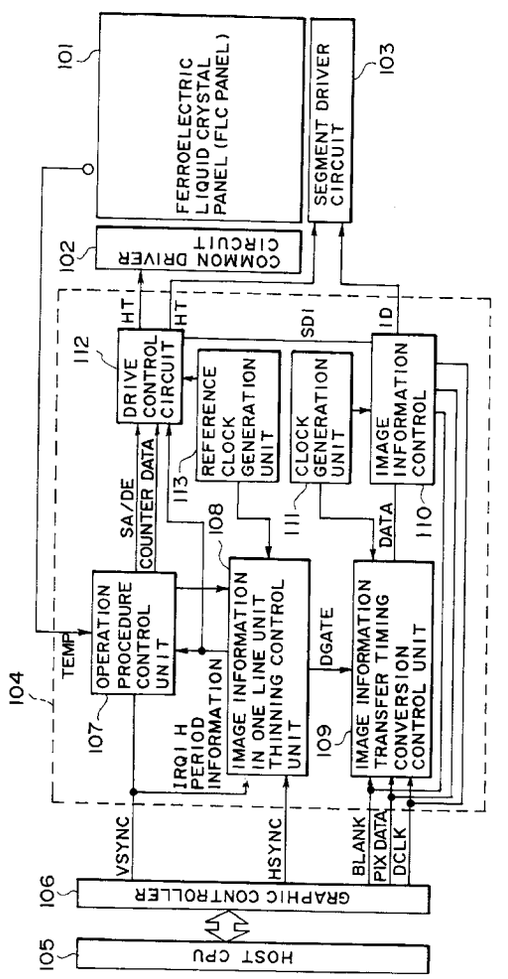


FIG. 1

EP 0 519 743 A2

The present invention relates to an image information control apparatus in a display system and particularly a display system using a ferroelectric liquid crystal having a memory property.

A recent liquid crystal display system used in a personal computer (PC) or a workstation (WS) has a larger screen size and a higher resolution and is required to have compatibility with an existing PC or WS.

In, e.g., recently popular IBM PC/AT machines, IBM CGA (Color Graphics Array), IBM EGA (Enhanced Graphics Array), IBM VGA (Video Graphics Array), and IBM 8514/A image adapter specifications are available as popular display modes used in the display system. These adapter specifications have different resolutions and different number of colors to be displayed.

For example, a CRT (Cathode Ray Tube) display system is known as a system capable of selectively setting the above display modes. Examples of the CRT display system are "Multisync II., "Multisync 3D", "Multisync 4D", and "Multisync 5D" available from NEC CORP. In a liquid display system for realizing a laptop PC or WS, it is difficult to cause one display system to selectively set different display modes.

In particular, a display system using a ferroelectric liquid crystal having a memory property suitable for a large screen size and a high resolution performs scan at a low frame frequency (5 to 20 Hz) so as to display information with a high resolution, as described in U.S.P. 5,058,994. This driving at the low frame frequency is achieved in synchronism with communication of image information.

At this time, when the display mode is changed, a synchronization relationship between driving at the low frame frequency and communication of image information is changed to pose a problem.

In a display system using a ferroelectric liquid crystal, the drive frequency is changed in accordance with a change in environmental temperature to compensate for temperature dependency for threshold characteristics inherent to the ferroelectric liquid crystal, and a period required to write in one-line information is changed accordingly. In order to synchronize driving at the low frame frequency and communication of image information, the end of write access of one-line information is signaled by an HSYNC signal (horizontal sync signal) to a graphic controller for managing transfer and communication of image information (information written in a VRAM under the control of a host CPU) when write access of one-line information is completed. Upon reception of the information representing the end of write access of one-line information, the graphic controller transfers one-line image information to the display system.

In order to employ the above communication system (called an external synchronization system), image information management software called a BIOS (Basic Input Output System) having a graphic controller therein must be changed.

This change may result in a loss of compatibility with CRT application software. For example, a palette (i.e., an element having a function of converting image information to color information) present in the graphic controller is accessed during a vertical blanking period of the CRT and changes color information in accordance with a CPU instruction. For this reason, when palette access is performed in accordance with the external synchronization system, color conversion timing errors occur because the vertical blanking period (every frame period) depends on the frame period of the ferroelectric liquid crystal panel, as compared with the case in which information is displayed in the CRT display system. This indicates that the color conversion speed becomes different from that in the CRT display system when application software for frequently performing screen color conversion is executed. As a result, compatibility with the CRT display system is lost in this application software. Some application software programs count the number of frames and then execute the next operations. In this case, a time difference occurs until the next operation is performed due to the same reason as described above. The processing speed in this case becomes different from that of the CRT display system, and the compatibility is therefore lost.

In a display system utilizing a ferroelectric liquid crystal, since interlaced scan is performed, the output procedures of image information from the VRAM are determined. In particular, the output procedures must be changed in accordance with a change in drive temperature, and information associated with this change is signaled to the graphic controller. Upon reception of this information, the graphic controller must interrupt VRAM access for a predetermined period of time so as to change the procedures for accessing the VRAM. This also makes it difficult to establish compatibility with the CRT display system.

On the other hand, since a ferroelectric liquid crystal has temperature characteristics, the drive waveform width (time required to perform write access) 1H or drive voltage must be controlled in accordance with the environmental temperature. In particular, control of 1H requires a special implementation due to the following reason. Although the period for transferring one-line image information is fixed-in the CRT display system, the one-line image information write time (period for receiving image information) of the ferroelectric liquid crystal is changed in accordance with a change in environmental temperature and is delayed to twice to eight times the transfer period of the CRT display system (e.g., VGA).

In order to solve this problem, there is proposed a method of defining 1H as an integer multiple of the image information transfer period of the CRT display system and thinning image information every 1H

scan. In another method described in EP 414960A1 to Miyamoto et al, temperature characteristics within the defined 1H are compensated by a drive voltage.

In the above system, however, since 1H is defined by the CRT display system, the 1H time change width in accordance with the environmental temperature is increased with an increase in 1H scan period of the CRT display system. During this period, when temperature compensation is performed by only the drive voltage, the drive voltage amplitude value becomes too high. This indicates that the breakdown voltage of a driver circuit for driving the ferroelectric liquid crystal must be increased, thus posing another problem. Fig. 5 shows 1H and the drive voltage as a function of the environmental temperature.

In addition, the drive voltage must be abruptly changed at a point where the 1H is changed in accordance with the environmental temperature. A voltage source for abruptly changing the drive voltage requires a long period of time to obtain a predetermined voltage value because the ferroelectric liquid crystal has a large capacitance. As a result, write access is not started until the drive voltage reaches a rated value.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a liquid crystal display system having improved compatibility with a CRT display system.

In particular, it is the principal object of the present invention to provide a temperature compensation system using a drive waveform against a change in environmental temperature.

According to the present invention, there is provided an image information control apparatus comprising:

a. first means for generating and outputting an image information transfer timing signal for controlling a transfer timing of image information;

b. second means for thinning the image information transfer timing signal transferred from the first means in accordance with an environmental temperature and outputting a thinned image information transfer timing signal;

c. third means for controlling a voltage waveform upon reception of the image information transfer timing signal; and

d. fourth means for controlling the third means so that the voltage waveform is kept constant during a period of at least two continuous image information transfer timing signals output from the second means.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a drive unit according to the present invention;

Fig. 2 is a flow chart showing a flow used in the present invention;

Fig. 3 is a block diagram of an operation procedure control unit used in the present invention;

Fig. 4 is a timing chart of the operation procedure control unit used in the present invention;

Fig. 5 is a graph showing a conventional temperature compensation relationship of 1H and the drive voltage as a function of the environmental temperature;

Fig. 6 is a graph showing a temperature compensation relationship of 1H and the drive voltage as a function of the environmental temperature according to the present invention;

Fig. 7 is a block diagram of a drive control circuit for performing temperature compensation, used in the present invention; and

Fig. 8 is a timing chart of the drive control circuit used in the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram showing a display system according to the present invention. The display system includes a ferroelectric liquid crystal (FLC) panel 101, a common (scan line) driver circuit 102, a segment (information line) driver circuit 103, a control circuit 104, a host CPU (Central Processing Unit) 105 of, e.g., an IBM PC/AT machine, a graphic controller 106, an operation procedure control unit 107, an image information in one line unit thinning control unit 108, an image information transfer timing conversion control unit 109, an image information control unit 110, a transfer clock generation unit 111, a drive control unit (for controlling a write in timing for one line of the FLC panel 101) 112, a reference clock generation unit 113, and a thermo-sensor 114.

The common driver circuit 102 designates a scan address to access an arbitrary line represented by the scan address. The segment driver circuit 103 accesses an information signal corresponding to image information to a predetermined line. The graphic controller 106 comprises a VGA controller serving as a display control section of the host CPU 105. The operation procedure control unit 107 controls operation procedures of the control circuit 104. The control unit 108 thins image information from the graphic controller 106 in units of lines. The image information transfer timing conversion control unit 109 converts image information transferred from the graphic controller 106 to a transfer speed and a timing which are suitable for the segment driver circuit 103. The image information control unit 110 converts image information into pieces of image information ID_1, ID_2,... transferrable every predetermined period. The transfer clock generation unit 111 generates a clock signal for the segment driver circuit 103. The drive control circuit

112 outputs a control signal for forming a drive waveform suitable for the common driver circuit 102 and the segment driver circuit 103. The reference clock generation unit 113 generates a reference clock for detecting the period of an HSYNC signal (horizontal sync signal) and generating a reference signal for a drive waveform period. The thermo-sensor 114 detects the environmental temperature of the FLC panel 101.

Functions of signal lines arranged between the control circuit 104 and the graphic controller 106 will be described below. Signals on these signal lines are output from a VGA as a standard graphic controller.

(1) VSYNC (vertical sync signal): This signal is a sync signal for determining a one-frame timing.

The VSYNC period is 1/70 or 1/60 sec for VGA.

(2) HSYNC (horizontal sync signal): This signal is a sync signal for determining a one-line timing.

The HSYNC period is 31.8 μsec for VGA.

(3) BLANK (blanking signal): When the signal level of the BLANK signal is set at "H", image information is carried on PIX DATA. When the BLANK signal is set at "L" level, boarder image information is carried.

(4) PIX DATA (image information signal): This signal is an image information signal on a signal line, obtained when information written by the host CPU 105 in a VRAM (image information storage memory) in the graphic controller 106 is read out.

(5) DCLK (dot clock signal): This signal is a timing signal for determining a one-dot timing of the PIX DATA.

(Basic Operation)

Fig. 2 is a flow chart showing the basic operation of the control circuit 104. Fig. 3 is a block diagram of the image information in one line unit thinning control unit 108 used in the present invention, and Fig. 4 is a timing chart of the control unit 108.

The basic operation in Fig. 2 will be described in detail below with reference to Figs. 1, 3, and 4. Numbers in circles in Figs. 2 and 4 represent the same operation periods. Assume that the graphic controller 106 outputs the above signals at the same timings and procedures as in the CRT display system in accordance with VRAM management software called a BIOS present in the graphic controller 106 under the control of the host CPU 105 for generating image information.

① When power is supplied, the control circuit 104 causes an H-SYNC period detection unit 301 shown in Fig. 3 to compare a reference clock from the reference clock generation unit 113 with an HSYNC signal and detect the number of reference clocks counted within the period of the HSYNC signal, thereby detecting the. period of the HSYNC signal. The detection information as horizontal sync information is supplied to the operation procedure control unit 107.

② The thermo-sensor 114 senses environmental temperature information of the FLC panel 101, and Temp information as temperature information is supplied to the operation procedure control unit 107.

③ A write period (1H = one horizontal scan period) and a drive voltage V which are required for writing one-line information of the FLC panel 101 is determined from the Temp information obtained in the period ② . The method of determining these values will be described in detail later. The image information is thinned in units of lines on the basis of the determined 1H. The number of lines to be interleaved in one vertical scan period is determined in accordance with the number of thinned lines. A thinned value N-1 corresponds to the number of lines interleaved in one vertical scanning period. When the thinned value N-1 is 2, interlaced scan is performed such that the first, fourth, seventh,..., (3F-2)th scan lines are scanned for the first field scan in the order named, the second, fifth, eighth,..., (3F-1)th scan lines are scanned for the second field scan in the order named, and the third, sixth, ninth,... 3Fth scan lines (F = 1, 2, 3,... integer) are scanned for the third field scan in the order named.

In the present invention, the first to third field scan cycles need not be determined in the order named. For example, a random interlacing system may be employed such that the second field scan may be the first field scan, and the first field may be the second field scan. This scan system is disclosed in U.S.P. 5,058,994. Such a multiinterlaced scan system may be incorporated in the present invention.

④ When the 1H, the drive voltage, and the thinned value are calculated, the operation procedure control unit 107 waits until a VSYNC signal output from the graphic controller 106 becomes active.

⑤ When an active VSYNC signal is detected, the operation procedure control unit 107 performs comparison of the HSYNC signal period detected in the period ① to detect the HSYNC signal period to check again if the HSYNC signal period is changed. This detection is performed because the HSYNC signal period in the graphic controller 106 may be changed by the host CPU 105. If any change is detected, the flow returns to the step corresponding to the period ② , and the procedure for changing the 1H and the drive voltage is repeated. This operation is performed every time the VSYNC signal is active.

⑥ The operation procedure control unit 107 sets, in an input line register 302, initial input line infor-

mation m representing an image information output timing (this information representing a specific HSYNC signal at a timing at which image information is transmitted after the VSYNC signal becomes active) determined between the operation procedure control unit 107 and the graphic controller 106. Meanwhile, an HSYNC counter 303 is reset by the VSYNC signal and is counted up every time the HSYNC signal is input.

A count value from the HSYNC counter 303 is always input to a comparator 304 and compared with the value of the input line register 302. When these values coincide with each other, the comparator 304 outputs an "H"-level signal (DGATE signal) until the next HSYNC signal falls.

The DGATE signal is input to an interrupt signal generation unit 305. The interrupt signal generation unit 305 generates an interrupt signal, i.e., an IRQ1 signal to be input to the control unit 107 and the drive control circuit 112 at the leading edge of the DGATE signal.

⑦ When the operation procedure control unit 107 detects the IRQ1 signal, it can detect that one-line image information set in the input line register 302 has been transferred. Next necessary input line information is set in the input line register 302. The count value of this information is a value obtained such that a value N obtained by adding the thinned value N-1 to one is added to a previous value ILD (= m) of the input line register 302. Fig. 4 shows the timing chart for the thinned value N-1 = 2, and the count value set in the input line register 302 is given as ILD+3 (m+3, m+6, m+9,....)

On the other hand, the image information output to the PIX DATA signal line is temporarily input to the image information transfer timing conversion control unit 109.

⑧ The operation procedure control unit 107 sets, in the drive control circuit 112, initial scan address latch data SA to be written in the FLC panel 101. The operation procedure control unit 107 outputs a drive enable signal DE for driving the common driver circuit 102 to the segment driver circuit 103. When the drive enable signal DE is set at "H" level, an SDI signal (i.e., a trigger signal for transferring image information to the segment driver circuit 103) and a panel 1H timing signal HT (i.e., a signal for determining the 1H period of the FLC panel 101) output from the drive control circuit 112 are set active.

⑨ The operation procedure control unit 107 receives the control unit interrupt signal IRQ1 serving as a transfer detection signal for image information corresponding to the count value (ILD+3: m+3, m+6, m+9,...) of the input line register 302. when reception of this signal is detected, the operation procedure control unit 107 sets the corresponding image information in the input line register 302 and transfers it to the drive control circuit 112. When reception of the IRQ1 signal is detected by the operation procedure control unit 107, the control unit 107 sets scan address data (SA+N) in the input line register 302 and transfers it to the drive control circuit 112.

The drive control circuit 112 sets the scan address latch data SA set in the period ⑧ in the common driver circuit 102 in response to the IRQ1 signal. At the same time, the drive control circuit 112 generates the panel 1H timing signal HT and supplies it to both the common driver circuit 102 and the segment driver circuit 103. By this operation, the common driver circuit 102 performs deletion of the addressed scan line. Data write access corresponding to the addressed scan line is performed on the basis of the image information transferred to the segment driver circuit 103 during the next panel 1H period.

During this period, the SDI signal is output from the drive control circuit 112, and at the same time the image information DATA input at a timing in the period ⑦ from the image information transfer timing conversion control unit 109 is output to the segment driver circuit 103 through the image information control unit 110 at a speed suitable for the transfer speed of the common driver circuit 102 and the segment driver circuit 103. Fig. 4 shows timings at which 2,560-dot (one pixel is constituted by four dots to perform area gradation) image information ID is transferred to the segment driver circuit 103 at a period of 100 nsec in accordance with 8-bit parallel transfer. When the panel 1H has a speed lower than that, the segment driver circuit 103 waits at the end of transfer during the difference time.

⑩ The operation procedure control unit 107 determines whether one field (one frame when viewed from the graphic controller 106) for the FLC panel 101 is completed. For example, the number of scan lines transferred from the graphic controller 106 is counted. If this count value exceeds a value obtained by adding n to the current input data ILD, one field is determined to be completed. In this case, the flow returns to the step corresponding to the period ④ to wait for reception of a VSYNC signal and start inputting the next field data. However, if the count value is smaller than the sum, the flow returns to the step corresponding to the period ⑨, and the subsequent operations are repeated.

⑪ The operation procedure control section 107 determines whether the end of field

in the period ⑩ is repeated N times. If so, the FLC panel 101 has received one-frame image information. However, if the end of field is repeated by the number of times smaller than N, processing during the period ④ is performed, and the subsequent operations are repeated. At this time, the initial input line data m is incremented by one to receive the next field data. If one of the numerical values from 1 to N is selected at random without incrementing the line data by one, random interlacing can be performed.

⑫ In the processing during the period ⑪, when write access of one frame is completed, the control circuit 104 determines whether a temperature compensation timing for the FLC panel 101 is set. This timing is determined with reference to the number of frames.

(Determination of 1H and Drive Voltage)

A method of controlling to maintain the drive voltage constant to perform temperature compensation as a characteristic feature of the present invention will be described below.

The 1H is determined in accordance with the environmental temperature to be an 1H period optimal for the FLC panel 101 (basic operation ②). At this time, the drive voltage (maximum value of the common-segment drive waveform) is given as a fixed value.

The thinned value N-1 upon thinning of the image information in units of lines is determined by the following equation, and this calculation is performed in the operation procedure control unit 107 (basic operation ③):

1H/HSYNC Signal Period = n

Integer Obtained by Rounding Decimal Part of n = N

By this calculation, the image information and the SYNC signal period are thinned, and the resultant values are respectively input to the segment driver circuit 103 and the drive control circuit 112. The thinning is performed by the thinning control unit 108.

When an optimal 1H value for the FLC panel 101 is selected in accordance with the environmental temperature, and image information is received at a period as an integer multiple of the HSYNC period, a time interval is formed until next driving is started at the end of 1H period.

This time interval is changed from 0 to a maximum of the SYNC signal period in accordance with a change in environmental temperature. During this time interval, the terminal potentials of the segment and common electrodes of the FLC panel 101 are controlled to be zero. Then, even if any time interval is formed, the image information will not be changed. When the 1H period is shortened with an increase in environmental temperature, the time for fixing the terminal potentials to be zero is prolonged. With this control, a waveform to be driven in synchronism with reception of the image information can be output even if the environmental temperature is changed and hence the 1H period is changed. Fig. 6 shows the relationship between 1H, the constant voltage time and the drive voltage as a function of the environmental temperature.

The above method of controlling the terminal potential of the FLC panel 101 to zero will be described below.

Fig. 7 is a block diagram showing part of the drive control circuit 112, and Fig. 8 is a timing chart thereof. A description will be made with reference to Figs. 7 and 8.

The IRQ1 signal has the same timing as that obtained when the HSYNC signal is thinned by the number of lines calculated by the 1H and the HSYNC signal. For this reason, image information is input at the period of this IRQ signal, and driving is started at this period.

As shown in Fig. 7, the operation procedure control unit 107 sets a count value in a programmable counter in accordance with information from the thermo-sensor 114. The programmable counter starts counting the reference clocks when the IRQ1 signal goes to "L" level. When the counter counts a predetermined value under the control of the operation procedure control unit 107, the counter outputs a ripple carry signal (RCO). The counter is reset again and outputs the RCO signal at a predetermined period. The RCO signal is used to generate a TIMR signal through a toggle F-F (Fig. 8). The TIMR signal is input to the drive waveform control signal generation circuit, so that the drive control signal is switched at every leading edge of the TIMR signal.

The drive control signal generation circuit is reset every time the IRQ1 signal goes to "L" level. The same drive control signal is repeatedly output.

On the other hand, the timing generation circuit sets a DACT signal to "H" level at the leading edge of the TIMR signal after the IRQ1 signal goes to "L" level. Thereafter, the timing generation circuit counts the leading edges of the TIMR signal. If the IRQ1 signal does not go to "L" level during counting of a predetermined count, the DACT signal is reset to "L" level. Fig. 8 shows a case in which the count value is 5.

The DACT signal is input to the drive waveform control change circuit. During the "L" level of this signal, a signal from the drive waveform control signal generation circuit is forcibly changed to a given value (i.e., a value for nullifying the terminal potential of the FLC panel 101) and is output to the segment and common driver circuits. This part is the important charac-

teristic feature of the present invention.

The 1H period has the same duration as the "H" level duration of the DACT signal. This duration has a value obtained by multiplying 4 (in this embodiment) with the period of the TIMR signal. When the TIMR signal period is controlled (i.e, the counter value of the programmable counter is controlled) by the operation procedure control unit in accordance with a change in environmental temperature, the 1H period can be changed in accordance with the change in environmental temperature. Since the difference between the IRQ1 signal period and the 1H period corresponds to the "L" level duration of the DACT signal, the drive waveform control signal is forcibly changed so that the terminal potential of the panel becomes zero. As a result, the FLC panel can be maintained in a state wherein the information has been written during this duration.

Outputs SWFD0 and SWFD1 and outputs CWFD0 and CWFD1 from the drive waveform control signal generation circuit are waveform control signals for the segment and common driver circuits, respectively. Values in Fig. 8 represent hexadecimal values of 2-bit signals as the signals SWFD0, SWFD1, CWFD0, and CWFD1, respectively.

The timing generation circuit resets a CSCLKCLR signal at the trailing edge of the DACT signal and sets it to "H" level again upon a lapse of the same pulse width (i.e., the period A in Fig. 8) as that of the TIMR signal. A CSCLK signal is generated from the CSCLKCLR signal and an inverted signal of the TIMR signal. The HT signal goes to "L" level at the leading edge of the first TIMR signal after the IRQ1 signal goes to "L" level. The HT signal is set to "H" level again at the leading edge of the next TIMR signal.

The segment and common driver circuits can be controlled in accordance with the above signals, i.e., SWFD0, SWFD1, CWFD0, CWFD1, CSCLK, and HT signals.

Drive waveform output timings of the driver circuit will be briefly described. The output waveform of the driver circuit is started at the leading edge of the CSCLK signal when the HT signal goes to "L" level. At this time, the level of the drive waveform is determined by the values of the SWFD0, SWFD1, CWFD0, and CWFD1 signals at the leading edge of the CSCLK signal. Thereafter, the drive waveforms of the segment and common electrodes are determined in accordance with the values of the SWFD0, SWFD1, CWFD0, and CWFD1 signals at the leading edge of the CSCLK signal.

As described above, a CRT display system output signal output from a graphic controller is received, and appropriate image information is transferred to the FLC panel 101. The terminal potential of the FLC panel 101 is forcibly set to zero (constant potential) in accordance with a change in environmental temperature, thereby performing temperature compensation without changing the drive voltage.

This indicates that driver circuit breakdown problems depending on the HSYNC signal period and write errors caused by the delay of the drive voltage upon a change in 1H can be solved.

Claims

1. An image information control apparatus comprising:
   a. first means for generating and outputting an image information transfer timing signal for controlling a transfer timing of image information;
   b. second means for thinning the image information transfer timing signal transferred from said first means in accordance with an environmental temperature and outputting a thinned image information transfer timing signal;
   c. third means for controlling a voltage waveform upon reception of the image information transfer timing signal; and
   d. fourth means for controlling said third means so that the voltage waveform is kept constant during a period of at least two continuous image information transfer timing signals output from said second means.

2. An apparatus according to claim 1, wherein said fourth means comprises means for maintaining the voltage waveform constant so that a terminal voltage difference of matrix electrodes is set to zero.

3. A display device comprising:
   a. first means for generating and outputting an image information transfer timing signal for controlling a transfer timing of image information;
   b. second means for thinning the image information transfer timing signal transferred from said first means in accordance with an environmental temperature and outputting a thinned image information transfer timing signal;
   c. third means for controlling a voltage waveform upon reception of the image information transfer timing signal;
   d. fourth means for controlling said third means so that the voltage waveform is kept constant during a period of at least two continuous image information transfer timing signals output from said second means; and
   e. fifth means for controlling display means to start one horizontal scan of matrix electrodes upon reception of the image information transfer timing signal.

4. A device according to claim 3, wherein said display means comprises a ferroelectric liquid crystal display panel.

5. A method of displaying data, comprising the steps of generating a timing signal for controlling image data transfer; thinning said timing signal by an amount dependent upon a measure of environmental temperature; and controlling a horizontal scan in response to said thinned timing signal.

6. A method according to claim 5, further comprising the steps of controlling a voltage waveform in response to said thinned timing signal, wherein said waveform is maintained substantially constant for at least two periods of said thinned timing signal.

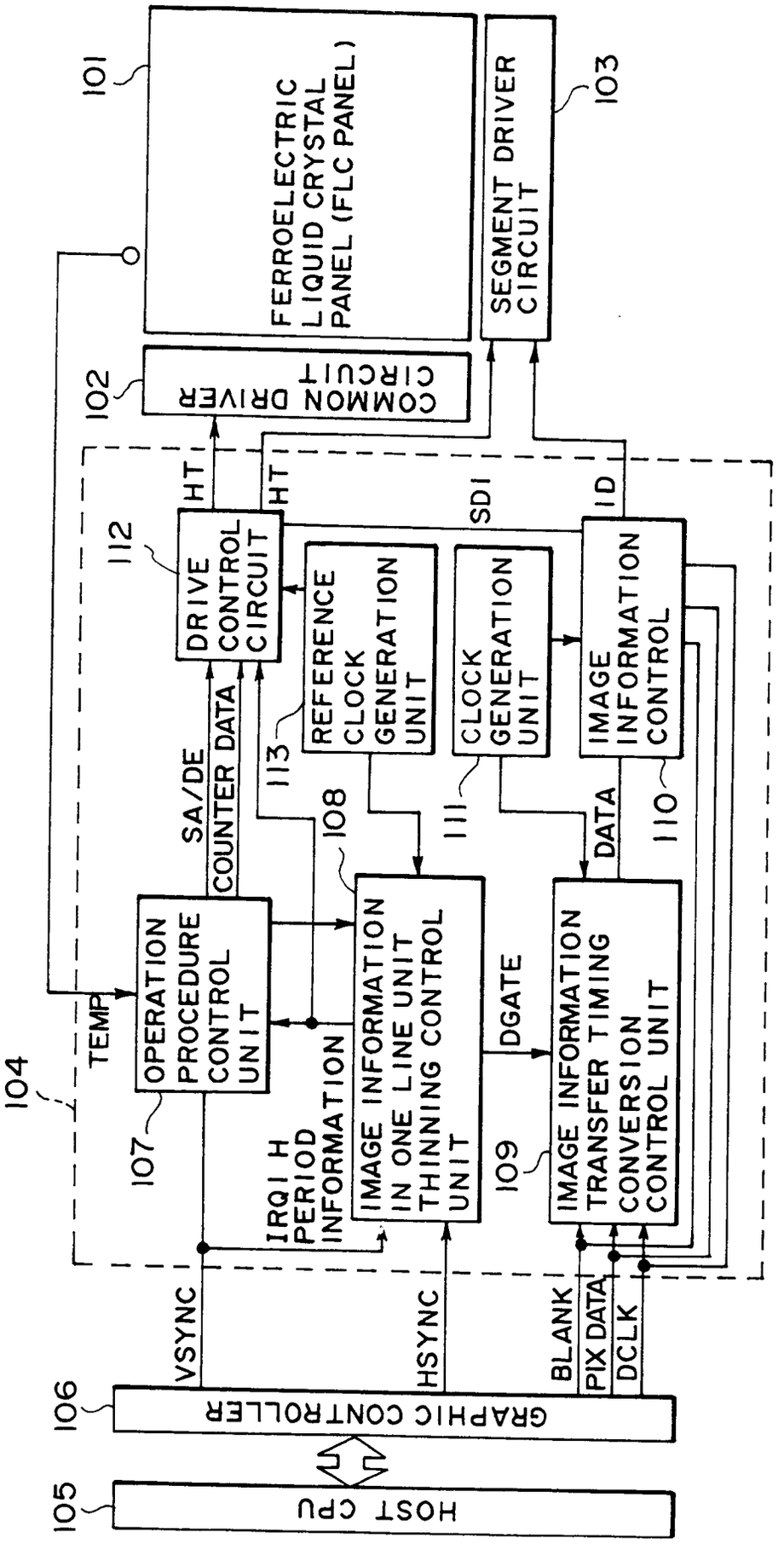

101
FERROELECTRIC LIQUID CRYSTAL PANEL (FLC PANEL)
103
SEGMENT DRIVER CIRCUIT
102
COMMON DRIVER CIRCUIT
HT
HT
SDI
ID
112
DRIVE CONTROL CIRCUIT
REFERENCE CLOCK GENERATION UNIT
CLOCK GENERATION UNIT
IMAGE INFORMATION CONTROL
113
111
110
SA/DE
COUNTER DATA
108
DATA
TEMP
OPERATION PROCEDURE CONTROL UNIT
IMAGE INFORMATION IN ONE LINE UNIT THINNING CONTROL UNIT
DGATE
IMAGE INFORMATION TRANSFER TIMING CONVERSION CONTROL UNIT
104
107
IRQ1 H PERIOD INFORMATION
109
VSYNC
HSYNC
BLANK
PIX DATA
DCLK
106
GRAPHIC CONTROLLER
105
HOST CPU

FIG. 1

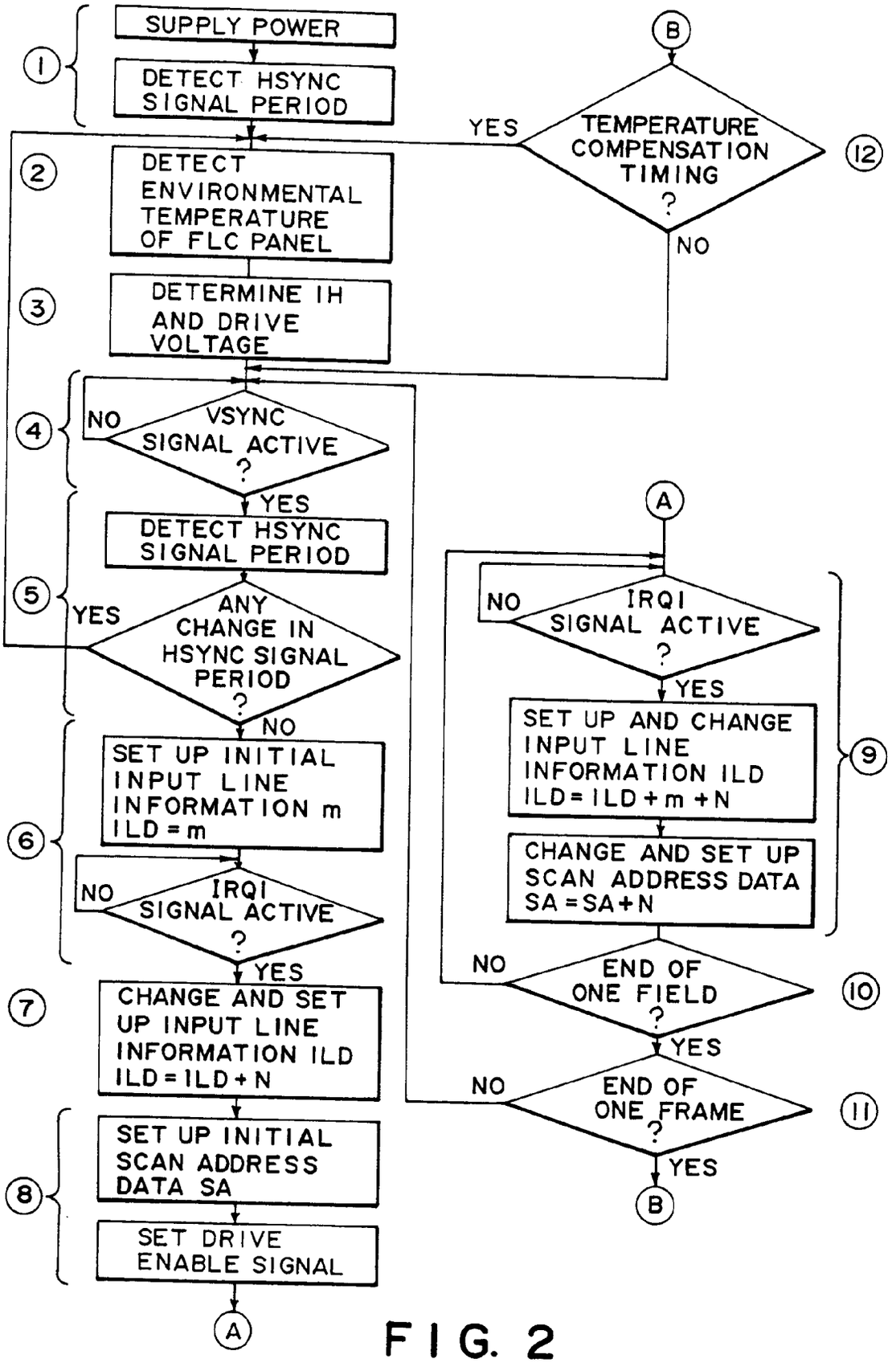

SUPPLY POWER
DETECT HSYNC SIGNAL PERIOD
DETECT ENVIRONMENTAL TEMPERATURE OF FLC PANEL
DETERMINE IH AND DRIVE VOLTAGE
VSYNC SIGNAL ACTIVE ?
NO
YES
DETECT HSYNC SIGNAL PERIOD
ANY CHANGE IN HSYNC SIGNAL PERIOD ?
YES
NO
SET UP INITIAL INPUT LINE INFORMATION m ILD = m
IRQI SIGNAL ACTIVE ?
NO
YES
CHANGE AND SET UP INPUT LINE INFORMATION ILD ILD = ILD + N
SET UP INITIAL SCAN ADDRESS DATA SA
SET DRIVE ENABLE SIGNAL
A
B
TEMPERATURE COMPENSATION TIMING ?
YES
NO
IRQI SIGNAL ACTIVE ?
NO
YES
SET UP AND CHANGE INPUT LINE INFORMATION ILD ILD = ILD + m + N
CHANGE AND SET UP SCAN ADDRESS DATA SA = SA + N
END OF ONE FIELD ?
NO
YES
END OF ONE FRAME ?
NO
YES
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 2

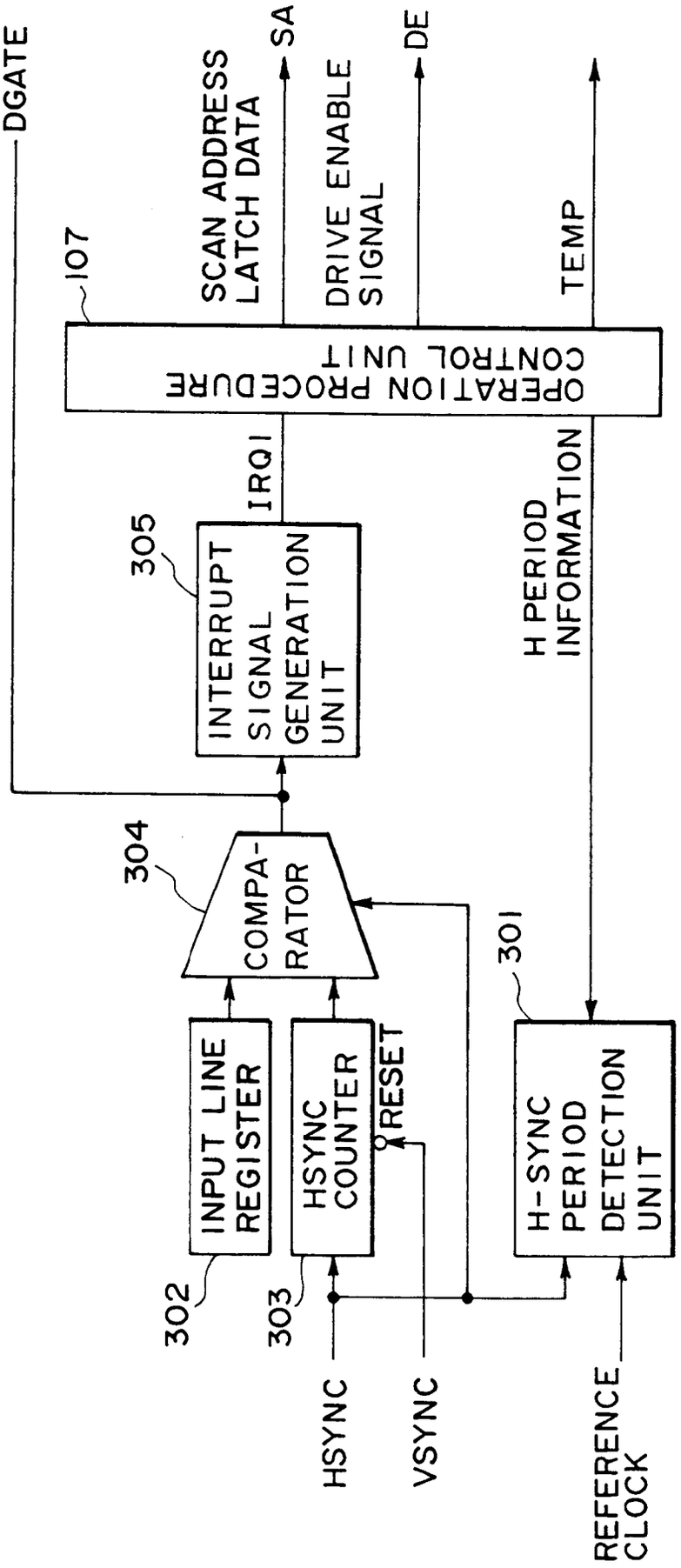

DGATE
107
SCAN ADDRESS LATCH DATA
SA
DRIVE ENABLE SIGNAL
DE
TEMP
OPERATION PROCEDURE CONTROL UNIT
IRQ1
H PERIOD INFORMATION
305
INTERRUPT SIGNAL GENERATION UNIT
304
COMPA-RATOR
301
INPUT LINE REGISTER
HSYNC COUNTER
RESET
H-SYNC PERIOD DETECTION UNIT
302
303
HSYNC
VSYNC
REFERENCE CLOCK

FIG. 3

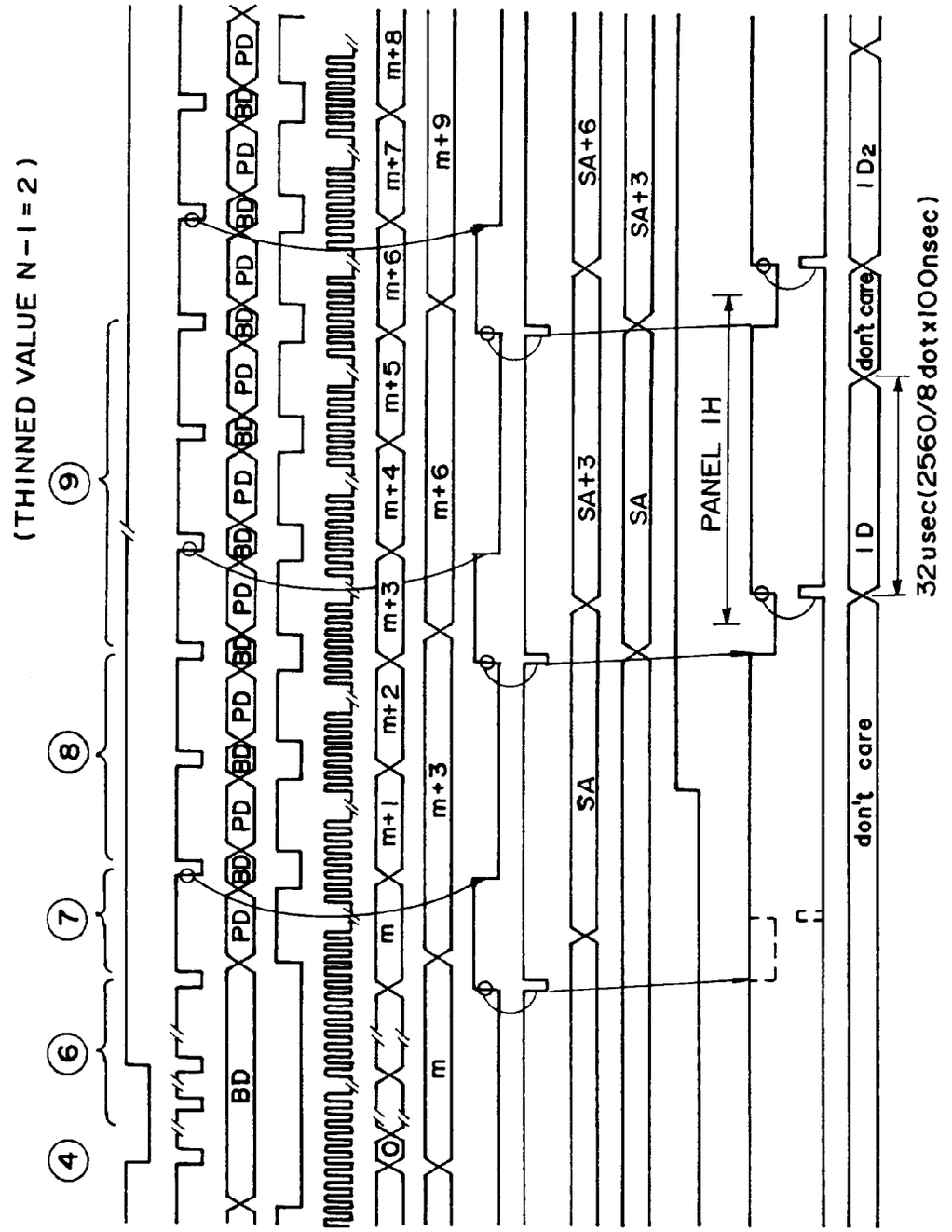

(THINNED VALUE N-1=2)
4
6
7
8
9
VSYNC
HSYNC
PIX DATA
HBLANK
DCLK
HSYNC COUNTER
INPUT LINE REGISTER
DGATE
IRQI
SCAN ADDRESS LATCH DATA
SCAN ADDRESS DATA
DRIVE ENABLE DE
PANEL IH TIMING SIGNAL HT
SDI
ID
BD
PD
0
m
m+1
m+2
m+3
m+4
m+5
m+6
m+7
m+8
m+9
SA
SA+3
SA+6
PANEL IH
n
don't care
ID
ID2
32usec(2560/8dot×100nsec)

FIG. 4

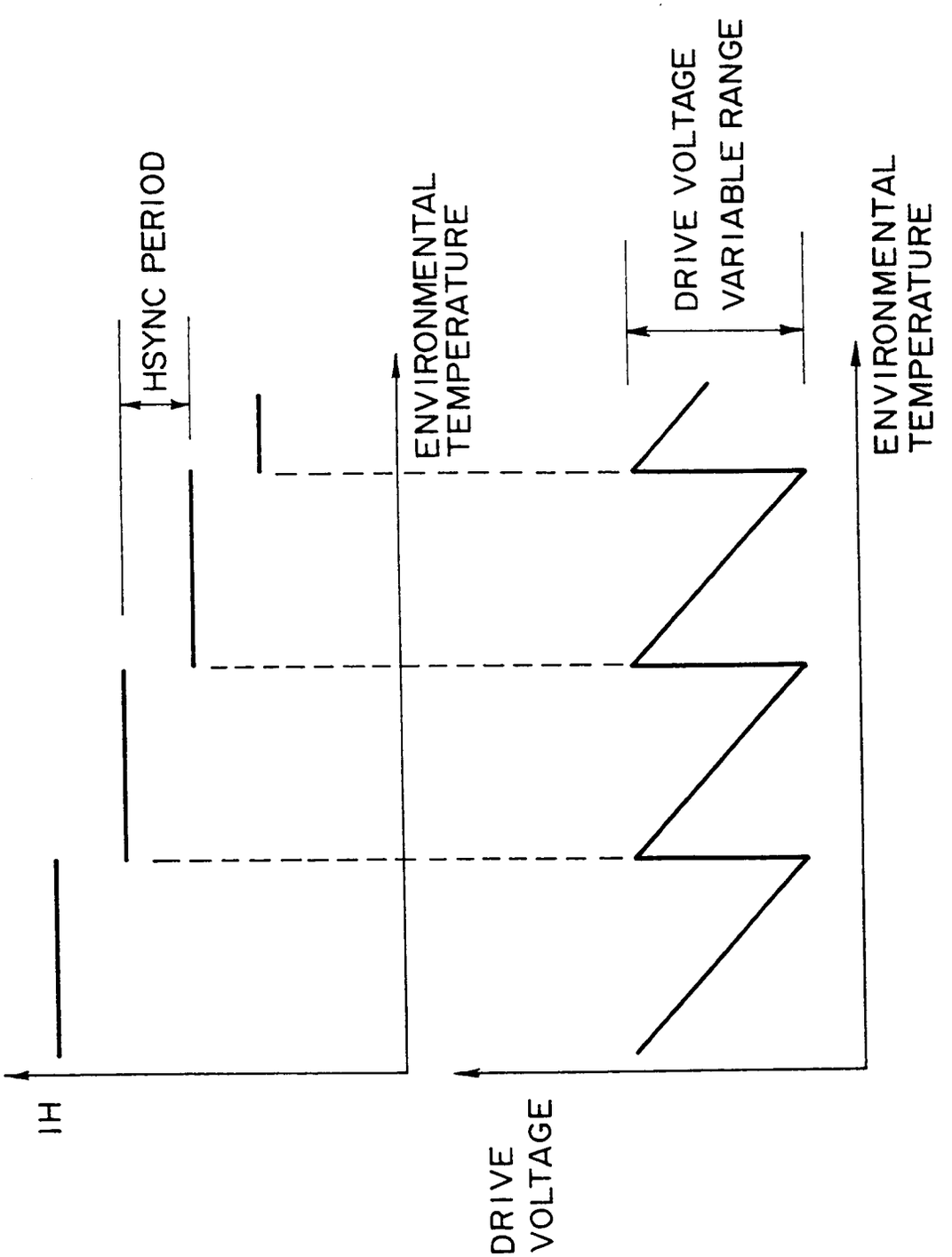

HSYNC PERIOD
ENVIRONMENTAL TEMPERATURE
DRIVE VOLTAGE VARIABLE RANGE
ENVIRONMENTAL TEMPERATURE
IH
DRIVE VOLTAGE

FIG. 5

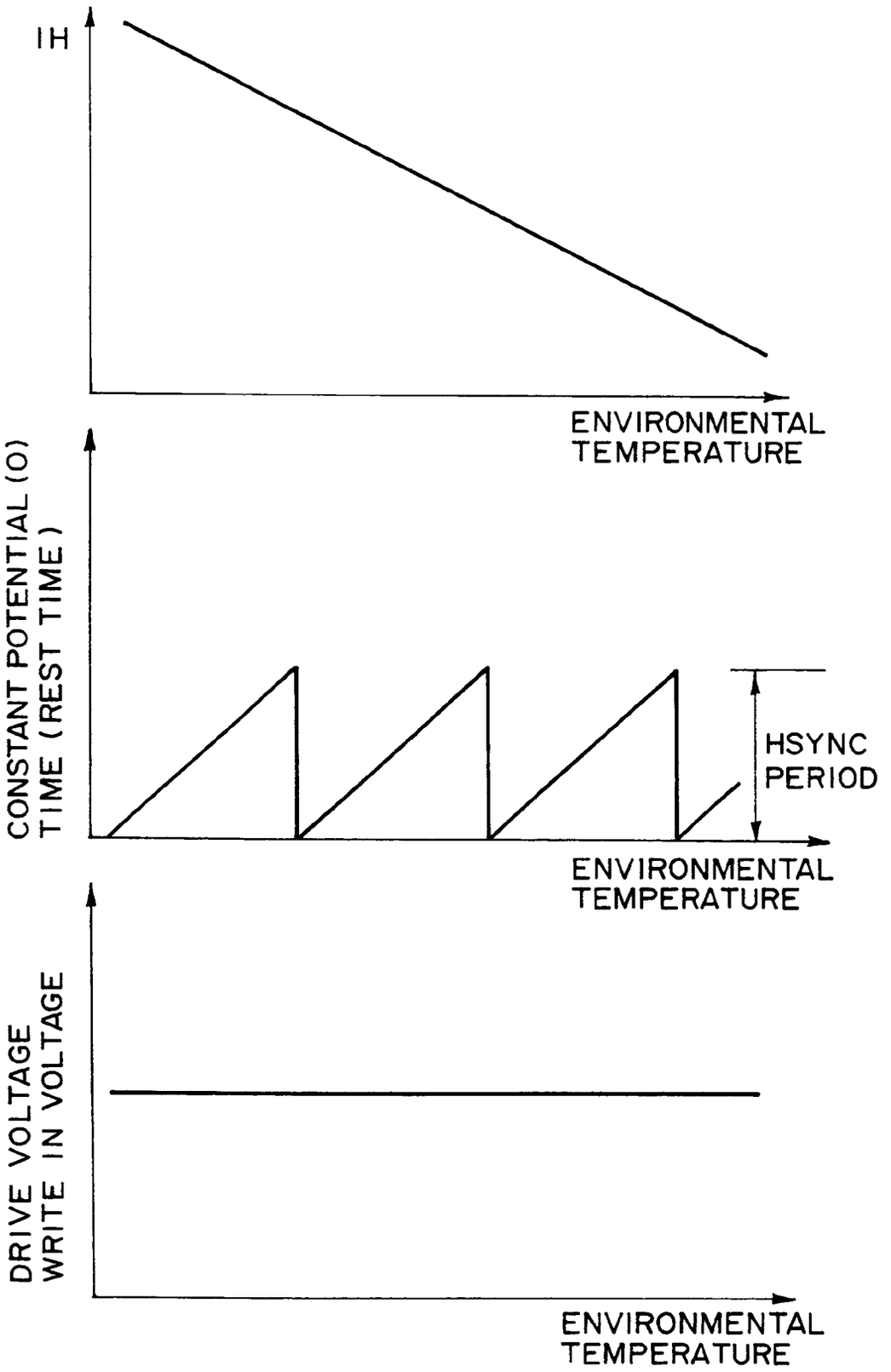

IH
ENVIRONMENTAL TEMPERATURE
CONSTANT POTENTIAL (O)
TIME (REST TIME)
HSYNC PERIOD
ENVIRONMENTAL TEMPERATURE
DRIVE VOLTAGE
WRITE IN VOLTAGE
ENVIRONMENTAL TEMPERATURE

FIG. 6

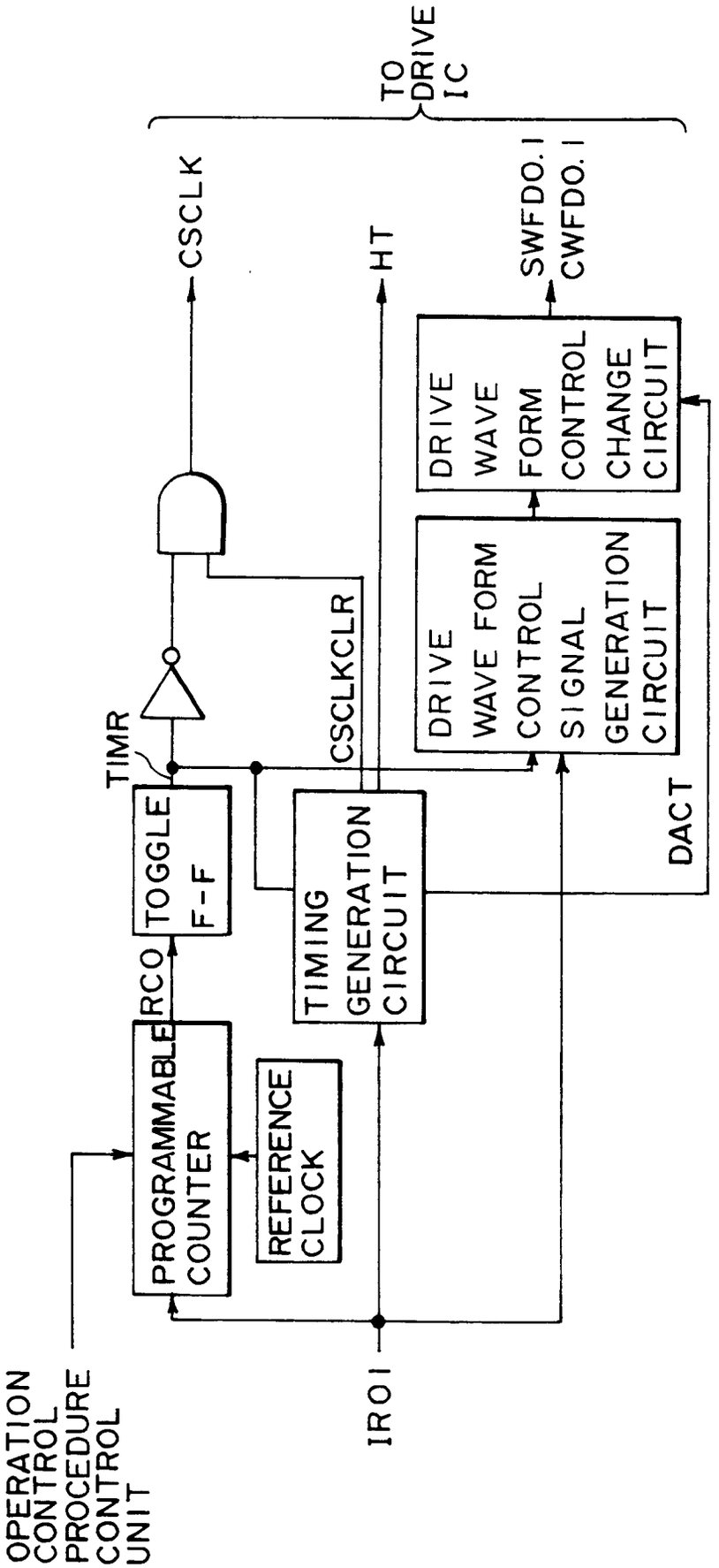
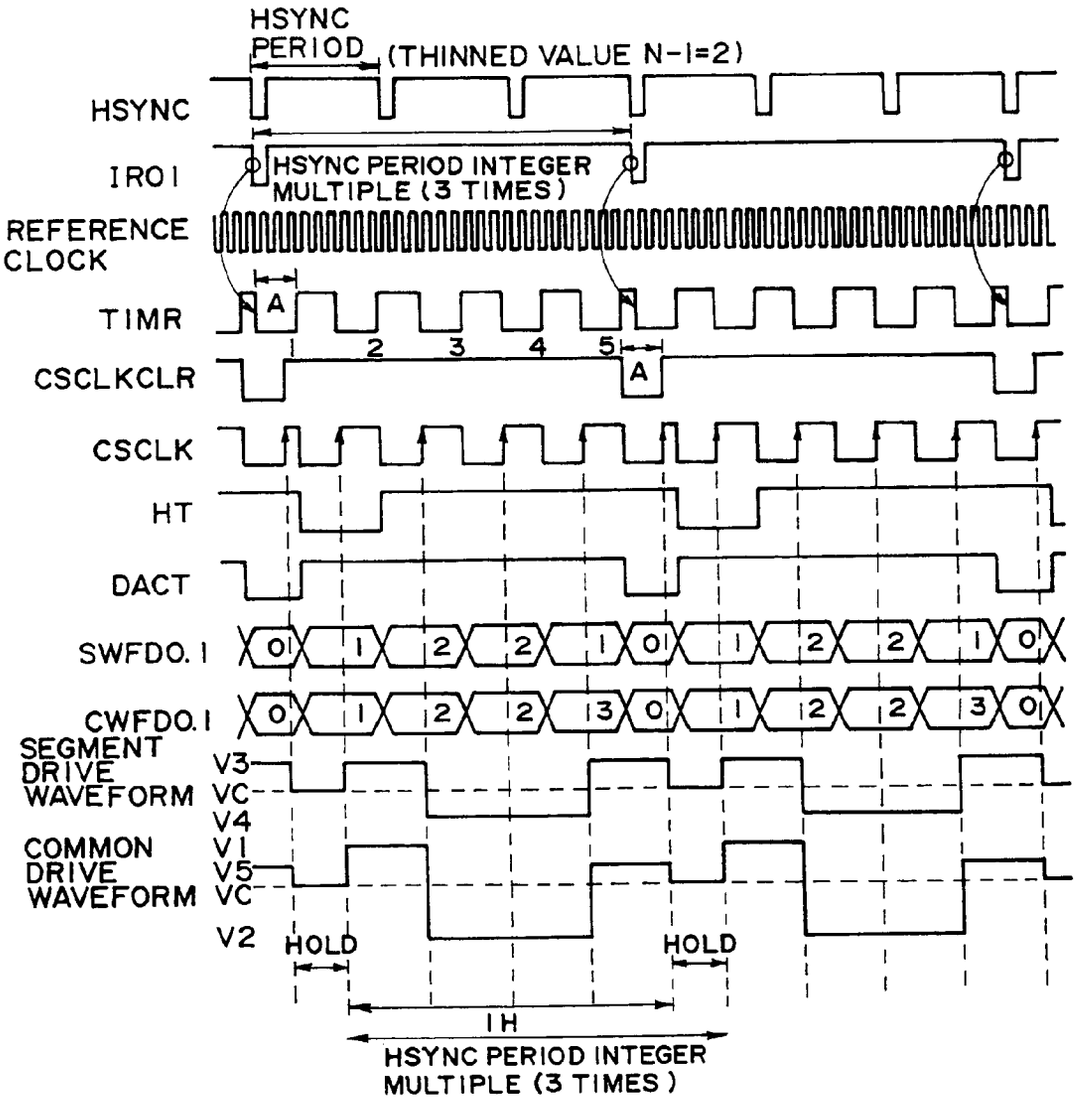

TO DRIVE IC
CSCLK
HT
SWFDO. I
CWFDO. I
DRIVE WAVE FORM CONTROL CHANGE CIRCUIT
DRIVE WAVE FORM CONTROL SIGNAL GENERATION CIRCUIT
TIMR
CSCLKCLR
TOGGLE F-F
TIMING GENERATION CIRCUIT
DACT
RCO
PROGRAMMABLE COUNTER
REFERENCE CLOCK
OPERATION CONTROL PROCEDURE CONTROL UNIT
IROI

FIG. 7



DRIVER CIRCUIT OUTPUT LEVEL TABLE

SWFDO.1	0	1	2	3
OUTPUT LEVEL	VC	V3	V4	-
CWFDO.1	0	1	2	3
OUTPUT LEVEL	VC	V1	V2	V5

FIG. 8