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(54) Boron implanted polysilicon resistor using an oxide screen.

(57) In a method for fabricating a polysilicon resistor structure, a layer of polysilicon (14) is formed over an insulation layer (11) on a substrate (10). The insulation layer may have windows through which the polysilicon may extend to contact the substrate. Selected regions of the polysilicon layer are implanted to form conductive regions, for interconnections, buses, and the like, and the polysilicon layer is patterned to remove portions of the polysilicon layer to create a desired resistor network pattern. A layer of undoped oxide (25) is formed overall, to fully encapsulate the top and sides of the layer of polysilicon. The thickness of the undoped oxide is selected to enable a dopant implantation energy to be determined, which will result in dopant being implanted through the undoped oxide, as a screen, with a peak concentration of dopant located at a central depth in the layer of polysilicon. Thereafter, a layer of BPSG (43) is formed over the oxide and reflowed to produce a planarized structure.

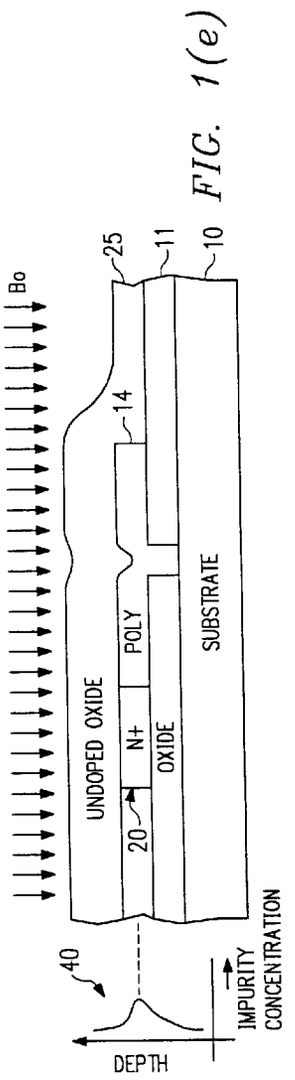

FIG. 1(e)

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This invention relates to improvements in semiconductor processes, and more particularly to improvements in methods for fabricating resistors in polysilicon layers.

It is desirable, in the manufacture of resistor-load SRAMs for example, to produce very high-valued polycrystalline silicon (polysilicon) resistors, for instance, with resistances as high as 1 to 10 teraohms (one teraohm $\equiv 1T\Omega \equiv 10^{12}\Omega$). It is usually preferable for the resistor bodies, or "channels", to be lightly-doped with boron in order to enhance the reverse diode formed by the junction of each channel area with its heavily-doped contact area.

Typically, the polysilicon layer in which the resistor is formed is between 500Å and 1000Å thick, to achieve high resistance. It is desirable, in the channel doping, to implant the boron so that the peak of the (approximately Gaussian) profile lies at or near the center of the polysilicon film in which the resistor is formed. This guarantees that, after nominal annealing, the resulting profile is most nearly uniform through the film, and is repeatable in concentration. It also prevents the existence of a significant amount of the distribution running deep into the underlying layers.

One problem that exists is that commercial ion implantation equipment is not easily operated at beam energies below 25 keV. At such low beam energies, the projected range for boron is about 825Å. On the other hand, it is preferable to operate with a minimum of 30keV beam current, where the projected range would be about 1000Å. However, in both instances, the peak of the implanted boron distribution is well beyond the center of the film thickness.

Another problem is that when boron is directly implanted into the poly film, it is done so with the resistor channel exposed. However, ion implantation usually entails relatively high particle contamination of wafers, and high-value resistors are extremely vulnerable to such contamination. Even small levels of contamination can dramatically change the resistivity of polysilicon, especially when the polysilicon is lightly doped, and, as a consequence, such direct implantation is not an ideal solution.

In light of the above, it is, therefore, an object of the invention to provide an improved method for fabricating a resistor in a polysilicon layer in which the doping profile is approximately Gaussian, with the highest concentration of dopant in the center of the polysilicon layer.

It is another object of the invention to provide a method of the type described, which is not as vulnerable to contamination as previous techniques

It is still another object of the invention to provide a method of the type described in which the doping concentration distribution is more readily repeatable.

It is yet another object of the invention to provide a method of the type described, which can use standard, readily available semiconductor fabrication or ion implantation equipment.

It is still a further object of the invention to provide a method of the type described, which adds no extra steps or complexity to standard integrated circuit fabrications processes.

These and other objects, features and advantages of the invention will become apparent to those skilled in the art from the following detailed description, when read in conjunction with the accompanying drawings and appended claims.

In accordance with a broad aspect of the invention a method for fabricating resistors in a polysilicon film or layer is presented. The method includes the step of providing a screen of undoped deposited oxide over the polysilicon film prior to the dopant implantation. The oxide then enables dopant implantation energies to be chosen within the recommended operating range of commercially available equipment and ideal processing parameters so that the distribution peak is near the center of the polysilicon film, and shields the polysilicon surface from contamination.

More particularly, a method is presented for fabricating a polysilicon resistor structure in which a layer of polysilicon is formed over an insulation layer on a substrate. The insulation layer may have windows through which the polysilicon may extend to contact the substrate. Selected regions of the polysilicon layer are implanted to form conductive regions, for interconnections, buses, and the like, and the polysilicon layer is patterned and selectively removed to create a desired resistor network pattern. A layer of undoped oxide is formed overall to fully encapsulate the top and sides of the polysilicon network pattern. The thickness of the undoped oxide is selected to enable a dopant implantation energy to be determined that will result in dopant being implanted through the undoped oxide, as a screen, with a peak concentration of dopant located at a central depth in the layer of polysilicon. Thereafter, a layer of BPSG is formed over the oxide and reflowed to produce a planarized structure.

The invention is illustrated in the accompanying drawing, in which:

Figures 1(a) - 1(f) are cross-sectional views of an integrated circuit device in various stages of its manufacture, in accordance with the method of a preferred embodiment of the invention.

In the various figures of the drawing, the sizes and dimensions of the parts has been exaggerated or distorted for clarity of illustration and ease of description. Also, in the various figures, like reference numerals are used to denote like or similar parts.

The steps for fabricating a resistor in a polysilicon layer, in accordance with a preferred embodiment of the invention are illustrated in Figures 1(a) - 1(f), cross-sectional views of an integrated circuit device in various stages of its manufacture. Such resistors can

be used, for example, in many integrated circuit devices, one excellent example of use being 1 - 4 megabit, 4T2R SRAM devices. It should be noted that the process steps and structures herein described do not necessarily form a complete process flow for manufacturing integrated circuits. It is anticipated that the present invention may be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. Moreover, although the invention is illustrated with various parts and layers of certain conductivity types and of certain dopants of specified doping concentrations, those skilled in the art will recognize that other, perhaps even opposite, conductivity types, and other dopants and different doping concentrations might be used to equal advantage.

Thus, in accordance with one embodiment of the invention, as shown in Figure 1(a), a substrate 10 is provided, on which a layer of insulation, such as oxide layer 11 is formed, for example, by known techniques, such as by thermal oxidation, or other known method. The substrate 10 can be silicon or polysilicon to which, in the embodiment illustrated, contact is to be made, for example. The oxide layer 11 is masked and etched to form a window or via 12 through which contact can be made to the underlying substrate 10. A layer 14 of polysilicon, in which a resistor will be subsequently formed, in accordance with a preferred embodiment of the invention, will be formed. The polysilicon layer 14 can be formed, for instance by CVD or other process, over the oxide layer 11 to extend into the window 12 to contact the underlying substrate 10. The thickness of the polysilicon layer 14 can be the same as that presently employed, for example, in the range of between about 500Å and 1000Å.

As shown in Figure 1(b), a layer of photoresist 16 is formed over the polysilicon film 14. The photoresist layer 16 is masked, exposed, and selectively removed, in accordance with known techniques, to form a window 18 overlying the portions 20 of the polysilicon layer 14 that will be implanted to form conductive regions, such as for example interconnects, buses, wiring, a V_{cc} rail, and so on. Thus, for example, phosphorus or arsenic can be implanted to produce highly doped N+ regions in the exposed portions 20 of the polysilicon layer 14. The photoresist layer 16 is then stripped.

Next, as shown in Figure 1(c), a new layer 22 of photoresist is formed over the structure, including the highly doped region 20. The photoresist layer 22 is then masked, exposed, and etched to the level of the oxide layer 11 to remove the exposed photoresist material and the portions of the polysilicon layer 14 lying beneath the exposed photoresist regions to create from the remaining portions of the polysilicon layer 14 the desired resistor network. In the resistor network, typically the body of the resistors that will ultimately be formed will be on the order of about 2μm to 4μm long by about 1μm wide. The photoresist layer 22 is then stripped.

Following the removal of the unwanted regions of the polysilicon layer 14, as shown in Figure 1(d), a layer 25 of undoped oxide is deposited overall, for example by a known TEOS reduction process. The thickness of the layer 25 can be, for example, in the range of between about 1200Å to 1500Å, or other suitable thickness to accomplish the desired distribution of dopant implanted to form the resistor in the underlying polysilicon layer 14. That is, the thickness of the oxide layer 25 is selected to enable the dopant implantation energies to be chosen so that the dopant concentration distribution peak is near the center of the polysilicon film 14. The thickness of the oxide layer 25 can be determined by known techniques, such as by LSS computer modeling techniques or by other known process modeling simulation techniques to achieve the desired dopant concentration distribution. The oxide layer 25 also serves to shield the surface of the polysilicon layer 14 from contamination.

Moreover, since the oxide layer 25 is deposited after the resistor pattern is etched, the layer 14 of polysilicon is completely encapsulated by the oxide. Furthermore, since all other operations pertaining to resistor formation are complete at that point, the screen provided by the oxide layer 25 can remain permanently, thus avoiding the detrimental effects on the resistors that might attend if the oxide layer 25 were to be removed. The screen provided by the oxide layer 25, in fact, can comprise the undoped oxide underlayer that is needed for subsequent BPSG planarizing films, with the dopant implantation energy adjusted to accommodate the thickness requirements of the sub-BPSG oxide. Preferably, the oxide layer 25 is deposited after the resistor network is formed, since otherwise, resistor degradation might result.

As shown in Figure 1(e), a dopant, such as boron, is implanted through the oxide layer 25 into the polysilicon layer 14. In accordance with the invention, the dopant is implanted so that the peak concentration of dopant is maximum at approximately the center of the polysilicon layer 14, as shown by the graph 40 of impurity concentration vs. depth adjacent the drawing in Figure 1(e). The depth scale of the graph 40 is approximately the same as the stylized cross-section of the portion of the integrated circuit shown, to emphasize the Gaussian distribution of dopant from the surface of the device in the direction of the substrate. It has been found, for example, that with a layer of undoped oxide having a thickness of between about 1100Å and 1500Å, for example about 1220Å, and with an implantation energy of between about 40keV and 60keV, for example, between about 45keV and 55keV, boron can be implanted, for example, in doses of between about (1×10^{12} cm^{-2} to 1×10^{13} cm^{-2}) to produce the

doping profile generally shown by the graph 40.

As mentioned, when the boron doped region is formed with a resistor body dimensions of between about 2 to 4μm long by 1μm wide, in the polysilicon films of thickness between about 500Å to 1000Å thick, it has been found that a final resistance value of between about 0.1 to 10.0 TΩ can be achieved. Also, as mentioned, other dopants, such as arsenic, antimony, phosphorus, or the like can be used in place of the boron implant dopant described.

To complete the device, next, as shown in Figure 1(f), a layer of boro-phoso-silicate glass (BPSG) 43 can be formed, and reflowed over the surface of the structure. After the glass layer 43 is reflowed, it should be noted that since the flattest part of the approximately Gaussian profile of the implanted resistor dopant was at the peak in about the center of the depth of the polysilicon film 14 prior to reflowing the BPSG, a high-level of repeatability to the average concentration is achievable. Moreover, because of the centrally located flat part of the implant, and because of the small amount of implanted dopant extending beyond the bottom of the polysilicon film 14, after subsequent high temperature annealing, a nearly constant concentration of dopant is created from the top to the bottom of the polysilicon layer 14.

Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

Claims

1. A method for fabricating a polysilicon resistor structure, comprising:
   forming a layer of undoped oxide over a layer of polysilicon;
   implanting a dopant through said layer of undoped oxide into said layer of polysilicon with an energy to produce a peak concentration of said dopant at approximately a center depth of said layer of polysilicon to form a resistor structure in said layer of polysilicon.

2. The method of claim 1 further comprising the step of producing highly doped regions at selected locations in said polysilicon layer.

3. The method of claim 2 wherein said step of producing highly doped regions comprises implanting N+ producing impurities into said selected locations of said layer of polysilicon.

4. The method of claim 1 further comprising patterning said layer of polysilicon prior to said step of forming said layer of undoped oxide to form a desired resistor network pattern, whereby said undoped oxide is formed to surround the top and sides of said layer of polysilicon.

5. A method for fabricating a polysilicon resistor structure, comprising:
   providing a substrate;
   forming a layer of insulation on said substrate;
   forming a window in said layer of insulation extending to said substrate;
   forming a layer of polysilicon on said layer of insulation extending into said window to contact said substrate;
   forming a first mask over said layer of polysilicon to provide a window to expose implantation regions of said layer of polysilicon layer;
   implanting said exposed implantation regions to form conductive regions in said layer of polysilicon;
   stripping said first mask;
   forming a second mask over said polysilicon layer;
   removing, according to said second mask, portions of said polysilicon layer to create a desired resistor network pattern;
   removing said second mask;
   forming a layer of undoped oxide overall;
   implanting a dopant through said layer of undoped oxide into said layer of polysilicon with an energy to produce a peak concentration of said dopant at approximately a center of said layer of polysilicon to form a resistor structure in said layer of polysilicon;
   providing a layer of boro-phoso-silicate glass overall;
   and heating said layer of boro-phoso-silicate glass to cause said layer of boro-phoso-silicate glass to reflow and planarize.

6. The method of claim 5, wherein said step of forming a layer of insulation comprises forming a layer of oxide.

7. The method of claim 6 wherein said step of forming a layer of oxide comprises thermally growing oxide on said substrate.

8. The method of claim 5 wherein said step of forming a layer of polysilicon comprises depositing said polysilicon by a CVD process.

9. The method of claim 5 wherein said window of said masking layer defines routes for conductive paths in said polysilicon layer.

10. The method of claim 5 wherein said step of producing highly doped regions in said polysilicon layer comprises implanting N+ producing impurities into said polysilicon layer.

11. The method of claim 10 comprising the step of selecting said dopant from the group consisting of phosphorus and arsenic.

12. The method of claim 4 or 5, wherein said step of forming said desired resistor network pattern comprises the steps of forming said polysilicon layer to have resistor body patterns of between about 2 to 4μm long and about 1μm wide.

13. The method of claim 1 to 5 wherein said step of forming said layer of undoped oxide overall is accomplished by a TEOS reduction process.

14. The method of claim 1 or 5 wherein said step of forming said layer of undoped oxide overall is accomplished by forming an undoped oxide layer of thickness of between about 1200Å to 1500Å.

15. The method of claim 14 further comprising selecting the thickness of said undoped oxide layer so that the dopant concentration distribution peak of an implanted impurity in said layer of polysilicon can be controlled to be near the center of said layer of polysilicon.

16. The method of claim 14 further comprising completely encapsulating said polysilicon layer with said layer of undoped oxide.

17. The method of claim 1 or 5 further comprising the step of allowing said layer of undoped glass to remain permanently on said polysilicon layer.

18. The method of claim 17 further comprising the step of permitting said layer of undoped glass to serve as a sub-BPSG oxide.

19. The method of claim 1 or 5 wherein said step of implanting dopant through said layer of undoped oxide comprises implanting boron.

20. The method of claim 19 wherein said step of implanting boron comprises implanting boron with an implantation energy of between about 40keV and 60keV.

21. A method for implanting dopant into a polysilicon layer, comprising:

determining the thickness of an insulation layer through which said dopant can be implanted, and determining an implantation energy by which said dopant can be implanted, in order to locate a center of dopant concentration at a central depth in said polysilicon layer;

forming a insulation layer of said determined thickness on said polysilicon layer;

implanting said dopant through said insulation layer into said layer of polysilicon with said determined implantation energy.

22. The method of claim 21 wherein said step of forming an insulation layer comprises forming a layer of undoped oxide.

23. The method of claim 22 wherein, for a polysilicon layer of thickness between about 500Å and 1000Å, and for a dopant of boron, said step of determining the thickness of said insulation layer comprises determining a thickness for undoped oxide between about 1200Å to 1500Å, and said step of determining an implantation energy comprises determining an implantation between about 40keV and 60keV.

24. The method of claim 20 or 23 wherein said step of implanting dopant comprises implanting boron in doses of between about 1×10^{12} cm^{-2} to 1×10^{13} cm^{-2}.

25. The method of claim 1, 5 or 21 wherein said step of implanting dopant comprises implanting dopant from the group consisting of boron, antimony, and arsenic.

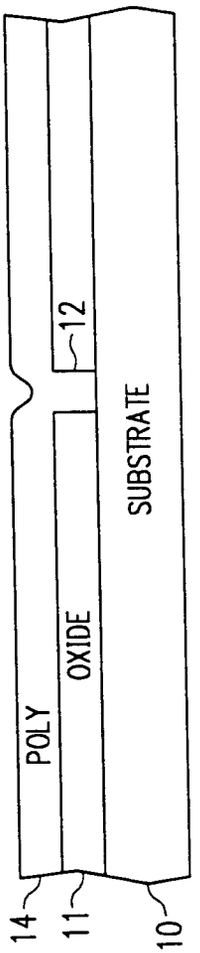

FIG. 1(a)

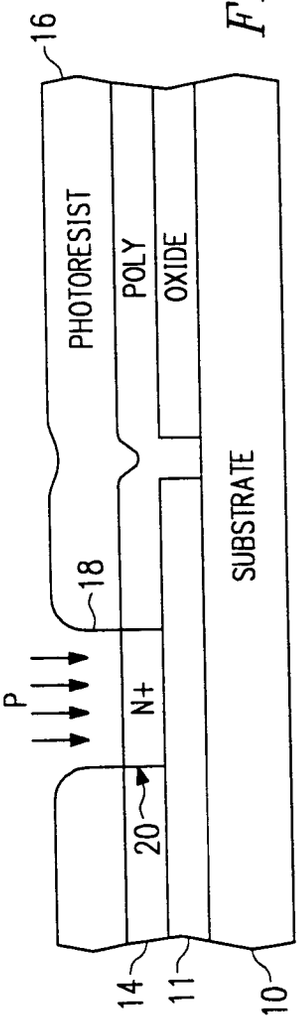

FIG. 1(b)

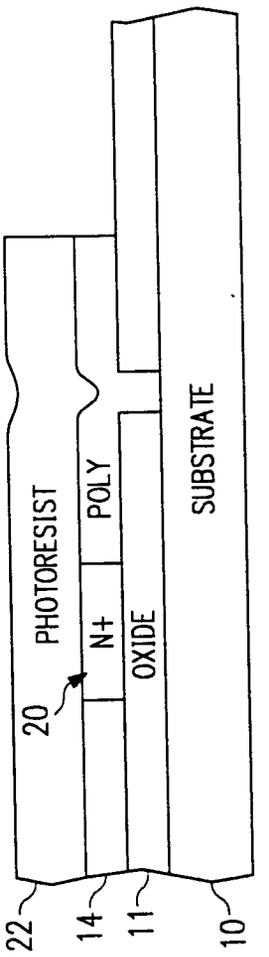

FIG. 1(c)

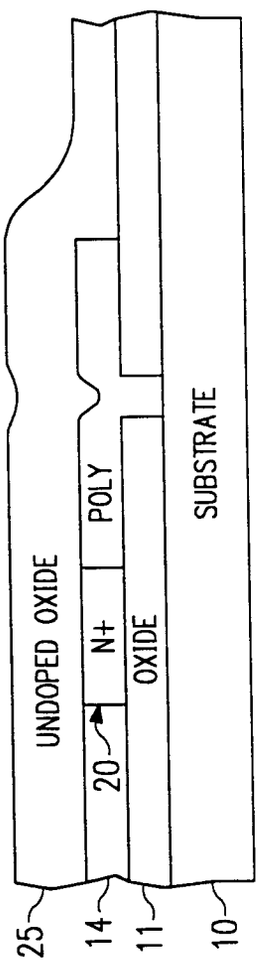

FIG. 1(d)

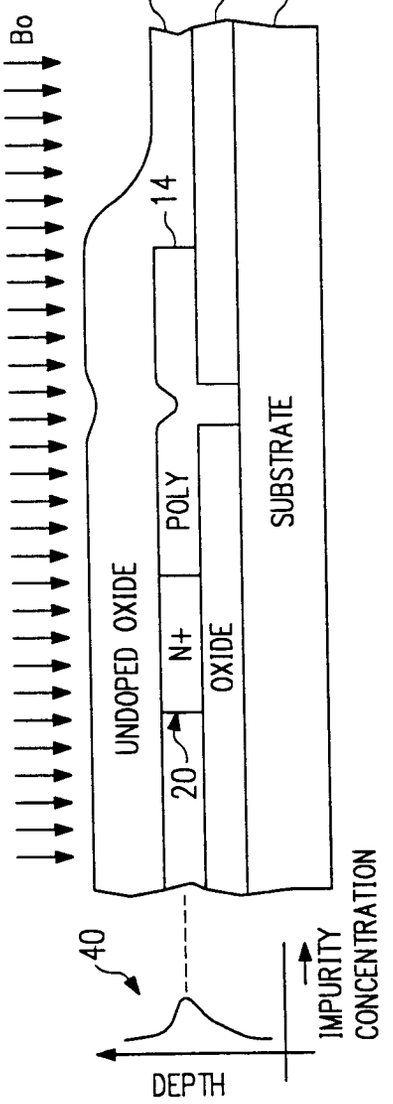

FIG. 1(e)

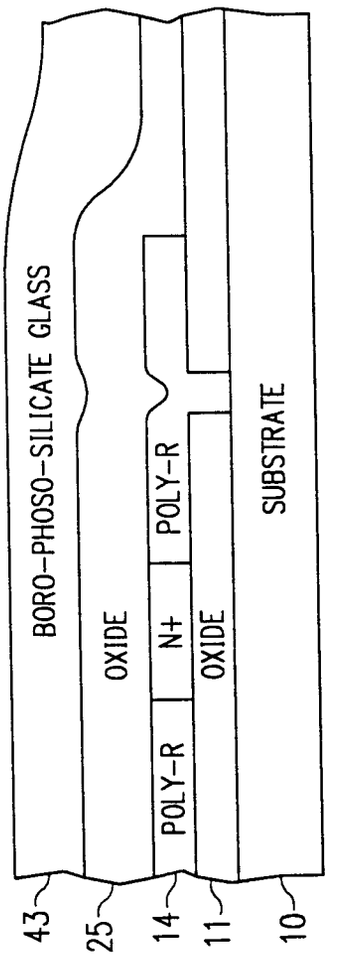

FIG. 1(f)

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EUROPEAN SEARCH REPORT

Application Number

EP 92 30 5958

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	GB-A-2 110 470 (HUGHES AIRCRAFT COMPANY) * page 2, line 44 - line 84; figure 2 *	1-4,17, 21,22,25	H01L21/3205 H01L21/3215
Y		5,6,9-11	
Y	US-A-4 828 629 (SHUJI IKEDA ET AL.) * column 9, line 46 - column 10, line 61; figures 11,12 *	5,6,9-11	
X	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 24, no. 1A, June 1981, NEW YORK US pages 74 - 75; J.M.LEAS ET AL.: 'Polysilicon resistor process' * the whole document *	1,21,22	
A		5-8	
A	EP-A-0 145 926 (INTERNATIONAL BUSINESS MACHINES CORP.) * column 10, line 26 - column 13, line 31; figures 4,5 *	1-25	
A	GB-A-2 207 809 (SAMSUNG SEMICONDUCTOR & TELECOMMUNICATIONS) 8 February 1989 * page 4, line 21 - page 6, line 15; figures 2A-2E *	1-25	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	05 OCTOBER 1992	LE MINH I.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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