



EUROPEAN PATENT APPLICATION

⑤¹ Int. Cl.⁵: **H03K 17/22**

②② Date of filing: 27.08.92

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⑤4 Zero-consumption power-on reset circuit.

⑤7 A power-on reset circuit utilizes capacitive couplings and does not establish any static current path between the supply rails. The circuit has a null static consumption and may be advantageously integrated

in CMOS micrologics. Moreover the circuit is insensitive to rebounds on the supply rails and to internal and external noise.

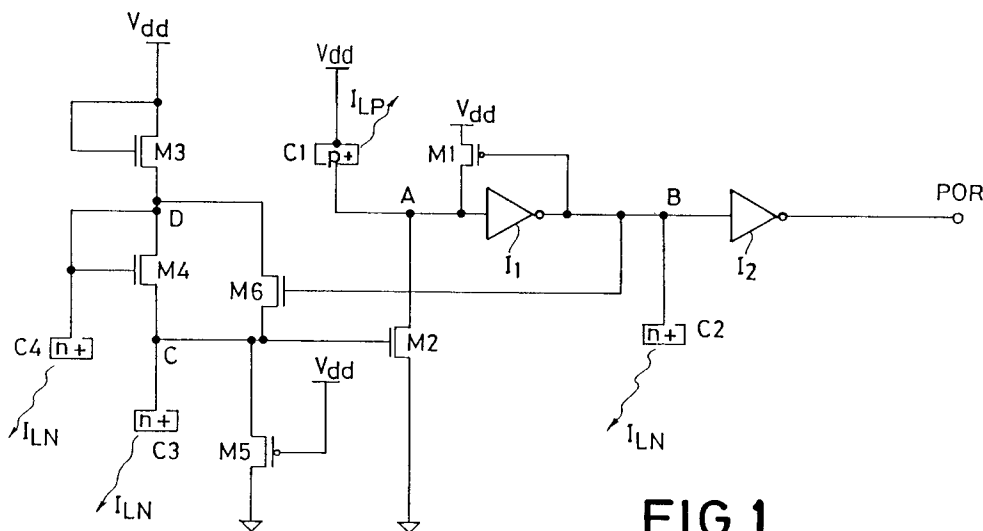


FIG. 1

BACKGROUND OF THE INVENTION

In integrated circuits and particularly in micrologics, there is often the necessity of integrating specific circuits capable of ensuring the resetting of all the functional structures of the integrated device to a certain state whenever power is switched on, independently of the manner in which the supply voltage raises from ground potential to the nominal supply voltage, in order to prevent the occurrence of unlicit or un contemplated configurations, which may cause malfunctioning and sometime latching of the whole device.

So-called power-on reset circuits, commonly referred to by the acronym POR, preside to this function. These circuits are capable of generating a resetting pulse of predetermined characteristics upon switching on the integrated circuit.

Generally, these POR circuits have an architecture which implies static current paths between the supply nodes and, though these power dissipating static current paths may normally have a relatively high impedance, the persistence of a nonnegligible static power consumption may not be compatible with design specifications of CMOS integrated devices, which typically have a null static consumption.

Moreover these POR circuits may become themselves a cause of malfunctioning if accidentally stimulated by internal or external transient events, e.g. noise induced by the switching of output buffers and the like.

OBJECTIVE AND SUMMARY OF THE INVENTION

A main objective of the present invention is to provide a power-on reset circuit (POR) having a null static power consumption and which is particularly insensitive to improper stimuli.

These objectives and other advantages are achieved by the circuit object of the present invention which is characterized by having a null static power consumption and an outstanding immunity to noise. Essentially the circuit comprises a first and a second inverter, connected in cascade, the output of the second inverter representing the output of the reset circuit. The interconnection node between the two inverters is capacitively coupled to ground potential while the input node of the first inverter is capacitively coupled to the supply voltage. A first switch, driven by the potential actually present on said interconnection node between the two inverters, is functionally connected between the input node of the first inverter and the supply rail and a second switch is functionally connected between the input node of the first inverter and ground. This second switch has a control terminal to which a driving signal which is tapped from a biasing line

connected to the supply rail and comprising at least two forward biased junctions in series with each other and capacitively coupled to ground potential, is fed. The node of the biasing line capacitively coupled to ground may be functionally connected to a control terminal of the second switch for determining a state of conduction or of interdiction.

The two forward biased and series-connected junctions of the biasing line may be realized by means of two diodes functionally connected in series and the connection node between the two series-connected diodes may also be capacitively coupled to ground potential.

Moreover, a discharge switch, controlled by the supply rail voltage may be connected between said node of capacitive coupling to ground of the biasing line and ground in order to quickly reset to ground potential the node controlling said second switch upon switching-off of the power supply to the integrated circuit.

A third switch may be connected between said intermediate node of the biasing line and a control terminal of the second switch and be driven by the signal present on the connection node between the two inverters, thus implementing, at the instant the first inverter triggers, a feedback which accelerates the discharge of the voltage present on the input node of the first inverter toward ground potential through the second switch, by increasing the potential present on said control node of the second switch toward the potential of the intermediate connection node of the biasing line, i.e. by eliminating the effect of the threshold of the second diode of the biasing line.

BRIEF DESCRIPTION OF THE DRAWINGS

The different aspects and advantage will become more evident through the following description of a preferred embodiment and reference to the annexed drawings, wherein:

Figure 1 is a circuit diagram of a power-on reset circuit of the invention;

Figure 2 is a diagram showing the operating voltage characteristics relative to the significant nodes of the circuit of Fig. 1.

DESCRIPTION OF THE BEST MODE

With reference to Fig. 1, the circuit of the invention readily integratable in a CMOS device comprises two inverters I1 and I2 connected in cascade. The circuit delivers a desired reset signal upon the switching on of the power to the integrated circuit through an output node POR. The input node A of the first inverter I1 is capacitively coupled to the supply node V_{dd} of the circuit

through an integrated capacitor C1, which may be formed by a P-type diffusion formed in a N-well region electrically connected to the supply rail V_{dd} . The intermediate connection node B between the two inverters is capacitively coupled to ground by means of an integrated capacitor C2, which may be realized by an N-type diffusion formed in a P-type of the integrated circuit substrate which is electrically connected to ground potential. A first switch M1, which may be realized by means of a P-channel MOS transistor, is driven by the signal present on the node B and is functionally connected between the input node A of the first inverter I1 and the supply rail V_{dd} . A second switch M2 which may be realized by means of an N-channel MOS transistor, is functionally connected between the input node A of the first inverter I1 and ground and is driven by a driving signal which is derived from a node C of capacitive coupling to ground of a biasing line connected to the supply rail, and which comprises at least two diodes or two forward biased junctions in series with each other, which may be implemented by means of two diode-configured N-channel MOS transistors M3 and M4. Both the node C and the intermediate node D of the biasing line are capacitively coupled to the ground potential of the circuit through respective integrated capacitors C3 and C4. Also these integrated capacitors C3 and C4 may be realized by means of N-type diffusions formed in a P-type substrate of the integrated circuit, connected to ground potential.

Moreover, a third switch may optionally and most preferably be connected between the C node of the biasing line, notably from where the signal driving the M2 switch is derived, for discharging the voltage present on the C node upon the switching off of the power; i.e. when the supply voltage drops below the potential of the C node. In the example shown in Fig. 1, such a switch is constituted by the P-channel transistor M5 whose control terminal is connected to the supply rail of the circuit.

Optionally the circuit may also advantageously be provided with a feedback loop constituted by a fifth switch M6 functionally connected between the D and C nodes of the biasing line and which is driven by the signal present on the B node between the two inverters. As shown, this fifth switch may be constituted by an N-channel MOS transistor.

The operation of the circuit, as may be followed by observing the diagrams of Fig. 2, is as follows.

Before the power-on instant, all the circuit nodes are at ground potential and all the devices are in an "OFF" state.

Upon switching on power, the nodes D, C and B initially continue to be maintained at ground potential because of their strong capacitive coupling with the substrate; the persistence of the ground potential on said nodes being eventually favored also by the natural current leakage toward ground, schematically depicted in Fig. 1 by the arrows I_{LN} , which is normally present in an N-type junction formed in a P-type substrate connected to ground.

On the contrary, the node A follows the rise of the supply voltage because of the strong capacitive coupling of this node with the supply rail (V_{DD}), also this voltage rise following behaviour is favored by the natural current leakage toward the supply rail, schematically indicated in Fig. 1 by the arrow I_{LP} , which is intrinsically present through a P-type junction formed in an N-well region connected to V_{DD} , and subsequently also by the establishment of an active current path toward the supply rail through the P-channel transistor M1.

After such a first brief capacitance charging phase, the further rise of the supply voltage toward the design value, begins to be followed also by the nodes D and C of the biasing line, each at a certain "distance" from the actual supply voltage due to the threshold voltages of the diode-connected transistors M3 and M4.

When the potential of the C node rises beyond the threshold voltage of an integrated N-channel transistor, through the N-channel transistor M2 a discharge path toward ground of the potential present on the input node A of the first inverter I1 is created. The rise of the C node potential causes, upon the switching on of the M2 transistor, a progressive drop of the potential of the input node A of the first inverter I1 from the level which had previously reached through the capacitive coupling provided by the capacitor C1 during said first charging phase and subsequently through the active path provided by the M1 transistor. When the dropping potential on the A node reaches the triggering level of the inverter I1, the latter triggers thus bringing its output node potential, i.e. the node B of the circuit, to the full value of the supply voltage, which determines the ending of the resetting pulse POR, which had been provided until that moment by the circuit through its output terminal.

The POR pulse, which from the power-on instant had followed the actual voltage rise of the supply rail V_{DD} , switches to ground potential, thus terminating its action on the circuits integrated in the semiconductor device.

Simultaneously, the triggering up to the supply voltage of the potential on the B node of the circuit, by further activating the transistor M2, suddenly increases the potential level reached by the C node of the biasing line, thus enhancing the conditions

which had lead to the new configuration (i.e. to the termination of the POR pulse).

This feedback action which is exerted through the node B on the M6 transistor, by substantially eliminating the effect on the potential reached by the C node due to the threshold of the M4 transistor, practically introduces an hysteresis which confers to the circuit an outstanding immunity against possible "rebounds" on the supply rail and/or internal noise. This effectively prevents the occurrence of spurious POR pulses which could otherwise take place as a consequence of an accidental drop of potential on the C node below the threshold level of the M2 transistor and produce an undesired spurious POR signal through the output terminal of the circuit.

The triggering level of the POR signal may be easily preestablished at the design stage by a relative dimensioning of the M1 and M2 transistors.

The M5 transistor permits to quickly discharge the C node and therefore also the D node of the biasing line, when the supply voltage drops below the level reached by the C node. This accelerates resetting after switching-off the integrated circuit. In practice, the transistor M5 may also be substituted by a diode, e.g. a P/N-well junction with the P-junction connected to the C node and the N-well connected to the supply rail. The action performed would be identical to that exerted by the transistor M5.

Of course the N and P diffusions which are used for realizing the capacitors C1, C2, C3 and C4 should have an area sufficiently large for establishing a strong capacitive coupling and cause relatively high leakage currents in order to optimize the operating conditions of the circuit.

Claims

1. A power-on reset circuit having a null static consumption, capable of generating through an output a resetting signal which upon powering the integrated circuit follows the rise of the supply voltage up to the design value and thereafter stably switches to ground potential, characterized by comprising cascade-connected first and second inverters, the output of the second inverter constituting the output of the power-on reset circuit, the connection node between the two inverters being capacitively coupled to ground and the input of the first inverter being capacitively coupled to the supply rail;
a first switch driven by the signal present on said connection node between the inverters, functionally connected between said input node of the first inverter and the supply rail;
a second switch functionally connected be-

tween said input node of the first inverter and ground and having a control terminal;

a biasing line connected to the supply rail and capacitively coupled to ground which comprises at least two series-connected forward biased junctions, the node of capacitive coupling to ground of the line being functionally connected to said control terminal of said second switch.

2. A circuit as defined in claim 1, wherein said two forward biased junctions in series are constituted by two diodes functionally connected in series, the connection node between the two diodes in series being capacitively coupled to ground.
3. A circuit as defined in claim 1, wherein a third switch driven by the supply voltage is functionally connected between said node of capacitive coupling to ground of said biasing line and ground.
4. A circuit as defined in claim 1, wherein a fourth switch is connected between a connection node between said two forward biased junctions and said control terminal of said second switch and is driven by the signal present on the connection node between said inverters, thus implementing upon the triggering of said first inverter, a feedback action capable of enhancing the discharge of the voltage present on the input node of the first inverter toward ground potential through said second switch and thus raising the potential on the control terminal of said second switch toward the potential of said connection node between said two junctions of the biasing line.
5. A circuit as defined in claim 1, wherein said integrated circuit has a P-type substrate connected to ground and said capacitive couplings to ground are established by means of integrated capacitors of an N-diffusion/P-substrate type and said capacitive coupling with the supply rail is realized by means of an integrated capacitor of a P-diffusion/N-well type wherein said N-well region is connected to the supply rail.
6. A circuit as defined in claim 5, wherein said second switch is an N-channel MOS transistor, said junctions connected in series of said biasing line are constituted by two diode-connected N-channel MOS transistors and said first switch is a P-channel MOS transistor.

7. A circuit as defined in claim 3, wherein said discharge switch which is controlled by the supply voltage is a P-channel MOS transistor capable of conducting when the supply voltage drops below the potential of said node of capacitive coupling to ground of said biasing line. 5

8. A circuit as defined in claim 4, wherein said fourth switch is an N-channel MOS transistor. 10

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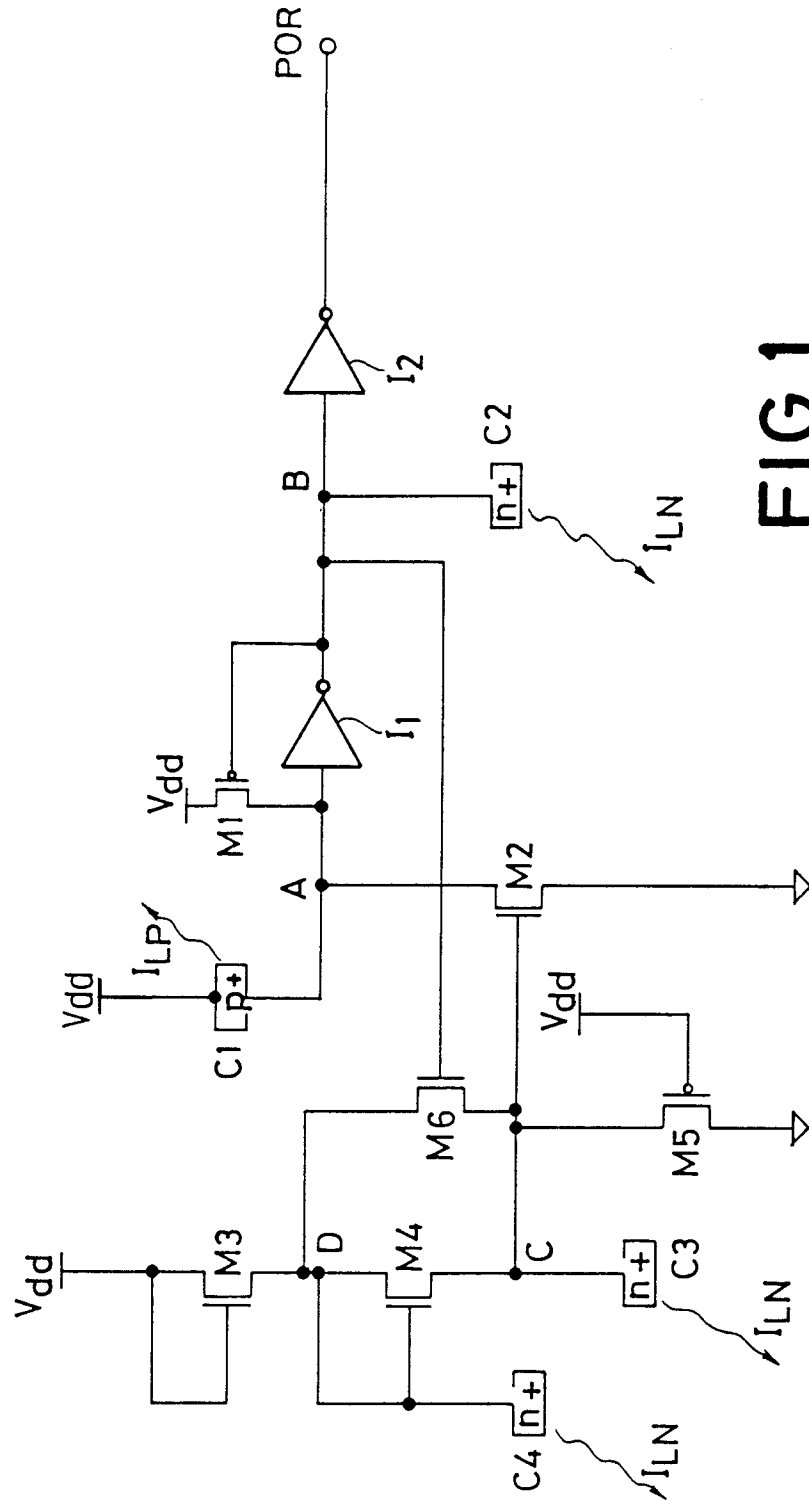


FIG. 1

