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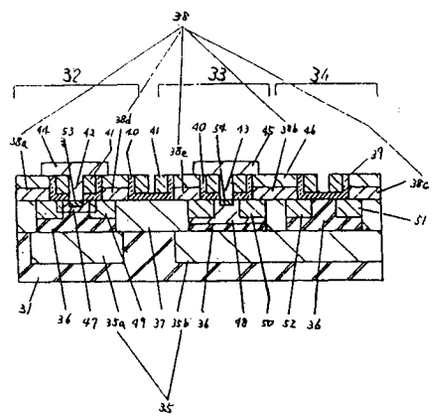
(54) **Semiconductor integrated circuit device and method of fabricating the same.**

(57) A superhigh speed vertical transistor having an ultra thin base, a vertical NPN transistor having a reverse direction structure for composing an IIL, and a lateral PNP transistor similarly composing an IIL to be an injector are formed on a P-type silicon substrate 1 by self-aligned and integrated. The emitter leading-out part opening of the superhigh speed vertical NPN transistor and the collector leading-out part opening of the vertical NPN transistor having a reverse direction structure are self-aligned to the base leading-out electrode. In the epitaxial layer, the P-type intrinsic base layer of superhigh speed vertical NPN transistor is formed by impurity diffusion from the emitter leading-out electrode formed of polysilicon film, and the P-type base layer of the vertical NPN transistor having a reverse direction structure is formed by ion implantation. By thus forming the superhigh speed vertical NPN transistor having a reverse direction structure in self-aligned process, the superhigh speed vertical NPN transistor of self-aligned type and IIL device may be integrated on a same chip. Besides, by forming the intrinsic base layer of the vertical NPN transistor having a reverse direction structure deeper in junction than the base layer formed by impurity diffusion from the polysilicon emitter electrode for the superhigh speed NPN transistor of self-aligned type, the low concentration epitaxial layer part beneath the intrinsic base layer for composing the emitter of the vertical NPN transistor having a reverse direction structure may be made smaller, thereby avoiding lowering of the current gain of the vertical NPN transistor having a reverse direction structure and lowering of high speed operation of IIL device accompanying accumulation of minority carrier.

Fig. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 92 30 8118

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 193 934 (TOKYO SHIBAURA ELECTRIC CO) 10 September 1986 * page 13, line 6 - page 17, line 26; figures 7A-9 *	1,2	H01L27/02 H01L21/82
A	* page 19, line 7-11 *	3,4	
A	DE-A-39 15 634 (TOSHIBA KAWASAKI KK) 30 November 1989 * column 7, line 10 - column 9, line 32; figures 1,2A-2H *	5-8,11	
A	EP-A-0 250 869 (TOKYO SHIBAURA ELECTRIC CO) 7 January 1988	5	
A	PATENT ABSTRACTS OF JAPAN vol. 015 no. 139 (E-1053) ,9 April 1991 & JP-A-03 019278 (MATSUSHITA ELECTRON CORP) 28 January 1991, * abstract *	10	
A	INTERNATIONAL ELECTRON DEVICES MEETING, 3 December 1979 WASHINGTON, D.C., USA, pages 328-331, KOICHI KANZAKI ET AL. 'A New Super High Speed ECL Compatible I2L Technology' * page 328, "Device structure/process * * figures 1-3 *	1,5	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 September 1995	Fransen, L

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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