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(54) Digital oscillator and color subcarrier demodulation circuit.

(57) A digital oscillator including an integrator (32, 33) for cumulatively integrating a specified signal and a controller (34-37) responsive to a control signal for maintaining the output frequency of the integrator (32, 33) within a limit corresponding to the amplitude of the control signal.

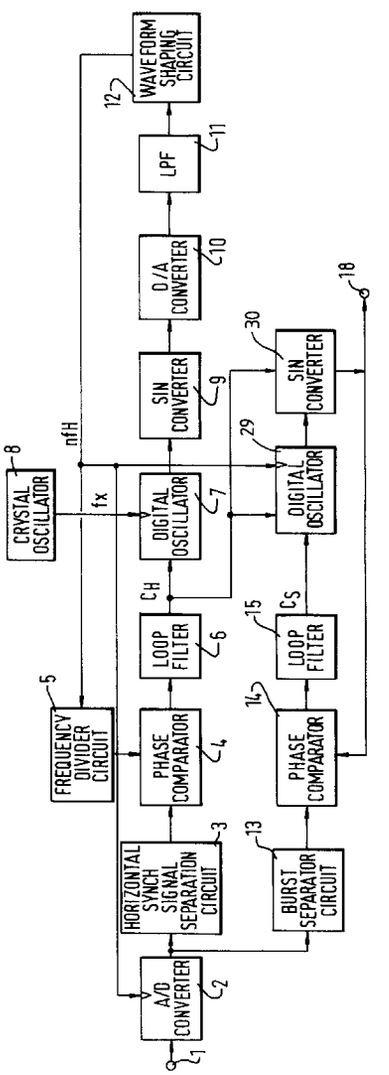

FIG. 5

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The present invention relates to a digital oscillator and a color subcarrier demodulation circuit having the digital oscillator, which are suitable for VTRs and television receivers.

Recently, television receivers which use digital signal processing systems have been developed. A specialized reproduction function which uses digital memories such as still picture reproduction can be simply achieved by constructing a television receiver with a digital signal processing system.

Among the types of digital television receivers, there are those which adopt a clock fH phase-synchronized with the horizontal synchronization signal and those which adopt a clock fsc phase-synchronized with the burst signal, which is a reference for the color subcarrier, as the system clock. When a clock fsc phase-synchronized with the burst signal is used, in the case of color demodulation, the B-Y and R-Y color difference signals can be simply demodulated by latching the color component at a timing synchronized to the clock. Thus, a simple construction of the color demodulation circuit is achieved.

However, in the case of a VCR (Video Tape Recorder), in image signals which contain jitter, the color subcarrier frequency and the horizontal synchronization signal frequency diverge from an interleaved relationship. That is to say, in this case, if clock fsc is adopted, the sampling point of the horizontal synchronization signal is not constant, and the horizontal output pulse is bound to have jitter. For this reason, there is a disadvantage in that the number of digital data in one horizontal period or one vertical period will not be constant.

Therefore, this type of case requires the adoption of the clock fH type system. However, in the NTSC and PAL systems, a color subcarrier is required in order to execute synchronized demodulation of the AM-modulated signals. For this reason, the design is such that a clock phase-synchronized with the color subcarrier is demodulated by the clock fH.

FIGURE 1 is a block diagram showing a prior art color subcarrier demodulation circuit which generates clock fH and, at the same time, demodulates the color subcarrier using this clock fH.

The analog video signal input through input terminal 1 is supplied to A/D converter 2. A/D converter 2 samples the input analog video signal at clock with frequency nfH (hereafter, clock nfH) from waveform shaping circuit 12 (described below), and converts it to a digital signal. The digitized video signal is supplied to horizontal synchronization signal separation circuit 3. Horizontal synchronization signal separation circuit 3 separates the horizontal synchronization signal from the digital video signal and supplies it to phase comparator 4. At the same time, frequency divider circuit 5 divides clock nfH from waveform shaping circuit 12 by n and supplies a signal with frequency fH to phase comparator 4. Phase comparator 4 compares the phases of the two inputs and outputs a phase error signal to loop filter 6. The phase error signal is integrated by a specified time constant in loop filter 6 and is output as control signal CH for digital oscillator 7. A clock of frequency fx is also supplied from crystal oscillator 8 to digital oscillator 7.

FIGURE 2 is a circuit diagram showing a practical construction of digital oscillator 7, and FIGURE 3 is a waveform diagram to illustrate its operation.

Control signal CH is input from loop filter 6 to digital oscillator 7 via input terminal 21. m1 bit adder 22 adds the output of data flip-flop (hereafter, DFF) 23 and control signal CH and outputs this to DFF 23. DFF 23 supplies the output of adder 22 to adder 22 at a clock of frequency fx which is input via terminal 24. That is to say, control signal CH is cumulatively integrated at every clock cycle by adder 22 and DFF 23. As shown in FIGURE 3, a sampled saw-tooth wave with amplitude of two (2) powered by m1 sampled at a cycle of 1/fx appears at output terminal 25. Since the oscillation frequency f1 of this saw-tooth wave is regulated by the cycle of 1 sample being 1/fx, it can be expressed by the following Equation (1).

$$f1 = (CH/2^{m1}).fx \quad (1)$$

As shown by Equation (1), the output of digital oscillator 7 is proportional to control signal CH, the phase error signal from phase comparator 4. The output signal of digital oscillator 7 is converted from a saw-tooth wave to a sine-wave in sine-wave converter (hereafter referred to SIN converter) 9. It is then converted to an analog signal by D/A converter 10, and is supplied to low-pass filter (referred to as LPF, hereafter) 11. LPF 11 eliminates the feed-back component of the input analog signal, and then supplies it to waveform shaping circuit 12. Waveform shaping circuit 12 shapes the waveform of the output of LPF 11 to a binary digital signal. The output clock of waveform shaping circuit 12 is divided into 1/n by frequency divider circuit 5 and is fed back to phase comparator 4. That is to say, a phase-locked loop (PLL) is composed of phase comparator 4, loop filter 6, digital oscillator 7, SIN converter 9, D/A converter 10, LPF 11, waveform shaping circuit 12 and frequency divider circuit 5. A clock nfH of frequency n times is output from waveform shaping circuit 12 by phase-synchronization with the horizontal synchronization signal from horizontal synchronization signal separation circuit 3.

At the same time, the digital video signal from A/D converter 2 is also supplied to burst separator circuit 13. Burst separator circuit 13 extracts the burst signal which is the reference of the color subcarrier, and outputs this to phase comparator 14. Phase comparator 14 compares the phases of the extracted burst signal and the output signal of SIN converter 17 (described below), and supplies a phase error signal to loop filter 15. Loop

filter 15 integrates the phase error signal by a specified time constant, and outputs it as control signal CS for digital oscillator 16. Digital oscillator 16 has the same composition as digital oscillator 7, and cumulatively integrates control signal CS at every cycle of clock nfH from waveform shaping circuit 12. Therefore, the oscillation output of digital oscillator 16 becomes a saw-tooth wave in which the frequency is proportional to phase error signal CS.

The oscillation output of digital oscillator 16 is supplied to SIN converter 17 and converted into a sine wave. The output of SIN converter 17 is output to output terminal 18 and, at the same time, is fed back to phase comparator 14. Thus, a PLL is composed by phase comparator 14, loop filter 15, digital oscillator 16 and SIN converter 17. The burst signal from burst separator circuit 13, that is to say, a demodulated color subcarrier which is phase synchronized to the color subcarrier, is output at output terminal 18.

Digital oscillator 16 is operated by clock nfH from waveform shaping circuit 12, and its oscillating frequency fsc1 is expressed by the following Equation (2). Here, m2 is the number of integration bits of digital oscillator 16.

$$\begin{aligned} fsc1 &= (Cs/2^{m2}) \cdot (CH/2^{m1}) \cdot fx \\ &= (Cs \cdot CH/2^{m1+m2}) \cdot fx \end{aligned} \qquad \ldots (2)$$

As shown by this Equation (2), apart from the oscillation frequency of digital oscillator 16 being influenced by control signal CS from loop filter 15, it is also influenced by the output signal CH of loop filter 6. Therefore, there is a problem that, in the state in which the relationship between the horizontal synchronization frequency and the color subcarrier frequency rapidly fluctuates, as in VCR and the like, the oscillation frequency of digital oscillator 16 becomes unstable due to the fluctuation of control signal CH.

To take account of this point, a method of demodulating a color subcarrier corresponding to the rapid fluctuation of the horizontal synchronization signal has been disclosed in the specification of U.S. Patent 4,625,232. FIGURE 4 is a block diagram showing a prior art color subcarrier demodulation circuit to which this method has been applied.

The point in which FIGURE 4 differs from FIGURE 1 is that divider 19 has been added between loop filter 15 and digital oscillator 16. Divider 19 is designed to divide control signal CS from loop filter 15 by control signal CH from loop filter 6 and supply the division result to digital oscillator 16 as a control signal.

In this case, oscillation frequency fsc2 of digital oscillator 16 can be expressed by the following Equation (3).

$$\begin{aligned} fsc2 &= (Cs/CH \cdot 2^{m2}) \cdot nfx \\ &= (Cs/CH \cdot 2^{m2}) \cdot (CH/2^{m1}) \cdot fx \\ &= (Cs/2^{m1+m2}) \cdot fx \end{aligned} \qquad \ldots (3)$$

As shown in Equation (3), oscillation frequency fsc2 of digital oscillator 16 is not affected by control signal CH of loop filter 6. Thus, in FIGURE 4, the fluctuation of system clock nfH is compensated. Therefore, in the color subcarrier demodulation circuit in FIGURE 4, even if the relationship between the horizontal synchronization frequency and the color subcarrier frequency fluctuates rapidly, a stable demodulated color subcarrier can be demodulated.

However, in the composition of FIGURE 4, digital oscillator 16 is controlled by the same divider 19 output throughout 1 horizontal period. Therefore, the output phase error of digital oscillator 16 due to the error of the division result produced by the bit limits of divider 19 accumulates throughout one (1) horizontal period. For instance, in the case of the frequency nfH of the system clock being set at 910 times the horizontal synchronization frequency, the phase error also will be 910 times. For this reason, the operation accuracy of divider 19 is required to be sufficiently high. That is to say, it is necessary to increase the bit number of the control signal supplied to digital oscillator 16, and this leads to increasing the scale of the hardware.

In this way, in the prior art color subcarrier demodulation circuit described above, the output phase error of the digital oscillator based on the operation error of the divider accumulates throughout one (1) horizontal period. Therefore, there is a problem in that a high operation accuracy of the divider is required, and it is necessary to increase the scale of the hardware construction.

The present invention therefore seeks to provide a digital oscillator which has a simple circuit construction.

The present invention also seeks to provide a digital oscillator which can stably demodulate a color subcarrier.

A further object of the present invention is to provide a color subcarrier demodulation circuit having a digital oscillator.

A digital oscillator according to one aspect of the present invention has an integrator for cumulatively integrating a specified signal and a controller responsive to a control signal for maintaining the output frequency of the integrator within a limit corresponding to the amplitude of the control signal.

The color subcarrier demodulation circuit according to another aspect of the present invention has a horizontal synchronization signal separation circuit which separates the horizontal synchronization signal from the input television signal, a first phase comparator which outputs a first phase error signal based on the phase error by comparing the phases of the horizontal synchronization signal and the demodulated horizontal synchronization signal, a horizontal synchronization signal demodulation means which generates a clock which is phase-synchronized with the horizontal synchronization signal based on the first error signal, and feeds it back to the first phase comparator as the demodulated horizontal synchronization signal, a burst separator circuit which separates the burst signal from the input television signal, a second phase comparator which outputs a second phase error signal based on the phase error by comparing the phases of the burst signal and the demodulated color subcarrier, a digital oscillator having a control device which controls the limits of the integrated value from a cumulative integration device which outputs integrated values through cumulative integration of the second phase error signal based on the clock from the horizontal synchronization signal demodulation means, and a normalization circuit which normalizes the oscillation output of this digital oscillator using the first phase error signal, and feeds it back to the second phase comparator as the demodulated color subcarrier.

For a better understanding of the present invention and many of the attendant advantages thereof reference will be now be made by way of example to the accompanying drawings, wherein:

FIGURE 1 shows a block diagram of a prior art color subcarrier demodulation circuit;

FIGURE 2 shows a block diagram of the digital oscillator in FIGURE 1;

FIGURE 3 shows a waveform diagram of the oscillation output of a prior art digital oscillator;

FIGURE 4 shows a block diagram of a prior art color subcarrier demodulation circuit;

FIGURE 5 shows a block diagram of an embodiment of the digital oscillator and a color subcarrier demodulation circuit in which the oscillation is used;

FIGURE 6 shows a block diagram of a practical construction for digital oscillator 29 in FIGURE 5;

FIGURE 7 shows a block diagram of a practical construction for SIN converter 30 in FIGURE 5;

FIGURE 8 shows a waveform diagram of the oscillation output of digital oscillator 29; and

FIGURE 9 shows a block diagram of another example of the digital oscillator of the invention.

The present invention will be described in detail with reference to the FIGURES 5 through 9. Throughout the drawings, reference numerals or letters used in FIGURES 1 through 4 will be used to designate like or equivalent elements for simplicity of explanation.

Referring now to FIGURE 5, a first embodiment of the color subcarrier demodulation circuit having a digital oscillator according to the present invention will be described in detail.

An embodiment of this is described below with reference to the drawings. FIGURE 5 is a block diagram showing an embodiment of the digital oscillator and the color subcarrier demodulation circuit in which the oscillation is used. In FIGURE 5, components which are the same as in FIGURE 4 have been given the same symbols.

An analog video signal is input at input terminal 1. The construction of the component which generates clock nfH, which is phase-synchronized with the horizontal synchronization signal of this input analog video signal, is the same at that in FIGURE 4. That is to say, the input analog signal is supplied to A/D converter 2. A/D converter 2 samples the input analog video signal using a clock with frequency nfH from waveform shaping circuit 12, and supplies it to horizontal synchronization signal separation circuit 3 by converting it to a digital signal. horizontal synchronization signal separation circuit 3 separates the horizontal synchronization signal from the digital video signal and supplies it to phase comparator 4. At the same time, the output of waveform shaping circuit 12 is also input to frequency divider circuit 5. Frequency divider circuit 5 divides clock nfH from waveform shaping circuit 12 by n, and supplies signal of frequency fH to phase comparator 4.

Phase comparator 4 compares the phases of the two inputs, and outputs a phase error signal based on the phase error to loop filter 6. Loop filter 6 integrates the phase error signal using a specified time constant, and outputs the integrated output to digital oscillator 7 as control signal CH. A clock of frequency fx from crystal oscillator 8 is also supplied to digital oscillator 7. Digital oscillator 7 cumulatively integrates control signal CH from loop filter 6 using the clock cycle from crystal oscillator 8, and supplies a saw-tooth wave output of a frequency proportional to the phase error signal to SIN converter 9.

SIN converter 9 converts the input saw-tooth wave to a sine wave and supplies it to D/A converter 10. D/A converter 10 converts the input digital signal to an analog signal and supplies it to LPF 11. LPF 11 eliminates the feed-back component of the input analog signal, and supplies it to waveform shaping circuit 12. The design is that waveform shaping circuit 12 converts the output of LPF 11 to a binary digital signal and outputs it to A/D converter 2 and frequency divider 5. A PLL is composed by phase comparator 4, loop filter 6, digital oscillator 7, SIN converter 9, D/A converter 10, LPF 11, waveform shaping circuit 12 and frequency divider circuit 5.

At the same time, the digital video signal from A/D converter 2 is also supplied to burst separator circuit 13. Burst separator circuit 13 extracts the burst signal from the input video signal and outputs it to phase comparator 14. Phase comparator 14 compares the phases of the extracted burst signal and the output signal of SIN converter 30 (described below) and supplies a phase error signal based on the phase error between these two to loop filter 15. Loop filter 15 outputs control signal CS by integrating the phase error signal using a specified time constant. In this embodiment, the design is that this control signal CS is supplied to digital oscillator 29 concerned in an embodiment of this invention. The design is that control signal CH from loop filter 6 and clock nfH from waveform shaping circuit 12 are also input to digital oscillator 29.

FIGURE 6 is a block diagram showing a practical construction for digital oscillator 29 in FIGURE 5.

Control signal CS from loop filter 15 is supplied to adder 32 via input terminal 31. Adder 32 adds control signal CS and the output of selector circuit 34 (described below), and outputs this to DFF 33. DFF 33 latches the adder 32 output using clock nfH which is input via terminal 39, and outputs it to output terminal 35, selector circuit 34, subtractor 36 and comparator 37. At the same time, control signal CH from loop filter 6 is supplied to subtractor 36 and comparator 37 via input terminal 38. Subtractor 36 finds the difference between the output of DFF 33 and control signal CH, and outputs it to selector circuit 34. Comparator 37 compares the sizes of the output of DFF 33 and control signal CH, and outputs this comparison result to selector circuit 34. The design is that selector circuit 34 selects the output of subtractor 36 only in the case when the output of DFF 33 is shown to exceed control signal CH by the comparison result of comparator 37 and supplies it to adder 32. In other cases, it selects the output of DFF 33 and supplies that to adder 32.

In other words, adder 32 and DFF 33 cumulatively integrate control signal CS in the same way as in prior art until the output of DFF 33 exceeds control signal CH. The design is that, when the output of DFF33 exceeds control signal CH selector circuit 34 supplies only the output of subtractor 36, that is to say only the overflow amount by which the output of DFF 33 is in excess of that of adder 32 for addition to control signal CS.

The oscillation output which appears at output terminal 35 of digital oscillator 29 is supplied to SIN converter 30. Control signal CH from loop filter 6 is also input to SIN converter 30. The design is that SIN converter 30 converts the oscillation output of digital oscillator 29 to a sine wave after normalization through division by its amplitude CH, and outputs it to output terminal 18. At the same time it is fed back to phase comparator 14.

FIGURE 7 is a block diagram showing a practical construction of SIN converter 30 in FIGURE 5.

The oscillation output of digital oscillator 29 is supplied to divider 42 via input terminal 41. Control signal CH from loop filter 6 is also input to divider 42 via terminal 43. The design is that divider 42 divides the oscillation output of digital oscillator 29 by control signal CH, and outputs this division result as a ROM 44 address. The design of ROM 44 is to store the data for converting the saw-tooth wave to a sine wave, and to output the data stored at each address designated by divider 42 to output terminal 45.

The following is a description of the operation of an embodiment constructed in this way with reference to FIGURE 8. FIGURE 8 is a waveform diagram showing the oscillation output of digital oscillator 29.

The analog video signal input via input terminal 1 is converted to a digital signal by A/D converter 2 and supplied to horizontal synchronization signal separation circuit 3. Horizontal synchronization signal separator circuit 3 separates off the horizontal synchronization signal of the input video signal and outputs it to phase comparator 4. The obtaining of clock nfH, which is n times the frequency of, and phase-synchronized with, the separated horizontal synchronization signal by a PLL composed of phase comparator 4, loop filter 6, digital oscillator 7, SIN converter 9, D/A converter 10, LPF 11, waveform shaping circuit 12 and frequency divider circuit 5, is the same as in prior art.

In this embodiment, control signal CH from loop filter 6 and clock nfH are supplied to digital oscillator 29 and control signal CH is also supplied to SIN converter 30. Burst separator circuit 13 separates the burst signal form the output of A/D converter 2 and supplies it to phase comparator 14. In phase comparator 14, the separated burst signal is phase-compared with the output of SIN converter 30 and a phase error signal for both is supplied to loop filter 15. The phase error signal is integrated by loop filter 15 and then converted to control signal CS and supplied to digital oscillator 29.

Digital oscillator 29 cumulatively integrates control signal CS with a cycle of clock nfH. When the cumulatively integrated value exceeds control signal CH, cumulative integration of the excess amount continues as a fresh cumulative value. That is to say, as shown in FIGURE 8, a saw-tooth wave with amplitude CH and a

gradient determined by clock nfH and control signal CS, is output from digital oscillator 29. The oscillation frequency fsc3 of this saw-tooth wave can be expressed by the following Equation (4).

$$\begin{aligned} fsc3 &= (Cs/CH)\cdot nfx \\ &= (Cs/CH)\cdot(CH/2^{m1})\cdot fx \\ &= (Cs/2^{m1})\cdot fx \qquad \ldots (4) \end{aligned}$$

An oscillation output from digital oscillator 29 proportional to the phase error is input to SIN converter 30. Sin converter 30 first divides the oscillation output by control signal CH. As described above, the amplitude of the saw-tooth wave from digital oscillator 29 is CH, and fluctuates according to control signal CH. Thus, SIN converter 30 normalizes the saw-tooth wave by dividing it by CH. It outputs sine wave data from ROM 44 by making this normalized value a ROM 44 address. The output of SIN converter 30 is fed back to phase comparator 14. A demodulated color subcarrier which is phase-synchronized with the burst signal can be obtained at output terminal 18 by a PLL composed of phase comparator 14, loop filter 15, digital oscillator 29 and SIN converter 30.

As shown in Equation (4) above, the oscillation frequency of digital oscillator 29 is not subject to the influence of control signal CH. Therefore, even when the horizontal synchronization frequency changes rapidly, stable demodulation of the color subcarrier can be achieved without being influenced by this change. Moreover, in this embodiment, the control signal CH can be supplied to digital oscillator 29 without influencing the control signal CS from loop filter 15. For this reason, operation errors are not be accumulated, even if digital oscillator 29 executes cumulative integration. That is to say, the scale of the circuit can be made more compact, since there is no requirement to increase the number of bits.

In this way, in this embodiment, control signal CS from loop filter 15 is supplied to digital oscillator 29 as it stands. Therefore, in contrast to prior art, operation errors do not accumulate in the cumulative integration value of digital oscillator 29. Digital oscillator 29 cumulatively integrates control signal CS at every clock nfH and, at the same time, it regulates its integrated value by control signal CH from loop filter 6. The oscillation frequency is made proportional to CH by operating at clock nfH and is made proportional to CS/CH by regulating the upper limit at CH. That is to say, the influence of control signal CH is cancelled out, and the oscillation frequency becomes proportional to control signal CS. Therefore, a stable demodulated color subcarrier can be obtained.

Incidentally, as shown in FIGURE 9, an accumulator composed of adder 51, which executes the operation [modk.CH] for an arbitrary numerical CH and a regular integer k, and latch 52, which outputs to adder 51 by latching the output of adder 51, may be employed as the digital oscillator. In this case, the oscillation frequency is adjusted by suitably setting the [modk.CH] of adder 51.

When using this invention as described above, a stable demodulated color subcarrier can be obtained with a small-scale circuit.

As described above, the present invention can provide an extremely preferable digital oscillator and a color subcarrier demodulation circuit including the digital oscillator.

While there have been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed as the test mode contemplated for carrying out the present invention, but that the present invention includes all embodiments falling within the scope of the appended claims.

The foregoing description and the drawings are regarded by the applicant as including a variety of individually inventive concepts, some of which may lie partially or wholly outside the scope of some or all of the following claims. The fact that the applicant has chosen at the time of filing of the present application to restrict the claimed scope of protection in accordance with the following claims is not to be taken as a disclaimer or alternative inventive concepts that are included in the contents of the application and could be defined by claims differing in scope from the following claims, which different claims may be adopted subsequently during prosecution, for example for the purposes of a divisional application.

Claims

1. A digital oscillator comprising Integration means (32, 33) for cumulatively integrating a specified signal, CHARACTERIZED IN THAT the oscillator further includes:

control means (34-37) responsive to a control signal for maintaining the output frequency of the integration means (32, 33) within a limit corresponding to the amplitude of the control signal.

2. A color subcarrier demodulation circuit comprising:

a horizontal synchronization signal separation circuit (3) which separates the horizontal synchronization signal from the input television signal;

a first phase comparator (4) which outputs a first error signal based on the phase errors between the input horizontal synchronization signal and a demodulated horizontal synchronization signal;

a horizontal synchronization signal demodulation means which generates a clock, the clock being phase-synchronized with the horizontal synchronization signal based on the first error signal, the clock being input to the first phase comparator as the demodulated horizontal synchronization signal;

a burst separator circuit (13) which separates the burst signal from the input television signal; and

a second phase comparator (14) which outputs a second phase error signal based on the phase error between the burst signal and a demodulated color subcarrier, CHARACTERIZED IN THAT the color subcarrier demodulation circuit further comprises:

a digital oscillator (16) including integration means for cumulatively integration the second error signal and control means responsive to the clock for maintaining the output frequency of the integration means within a limit corresponding to amplitude of the first error signal; and

a normalization circuit (30) for normalizing the oscillation output of the digital oscillator in response to the first phase error signal, the oscillation output being input to the second phase comparator as the demodulated color subcarrier.

3. A digital oscillator comprising integration means (51,52) for cummulatively integrating a specified signal (Cs) CHARACTERIZED IN THAT the integration means comprises; an adder circuit (51) which executes the operation [modk.CH], where k is a regular integer, and CH is a control signal; and a triggered latch circuit connected to receive the output of the adder circuit and to feed its output as an input to the adder circuit.

4. A horizontal synchronization signal separation circuit which separates the horizontal synchronization signal from the input television signal comprising, a first phase comparator which outputs a first phase error signal based on the phase error by comparing the phases of the horizontal synchronization signal and the demodulated horizontal synchronization signal, a horizontal synchronization signal demodulation means which generates a clock which is phase-synchronized with the horizontal synchronization Signal based on the first error signal, and feeds it back to the first phase comparator as the demodulated horizontal synchronization signal, a burst separator circuit which separates the burst signal from the input television signal, a second phase comparator which outputs a second phase error signal based on the phase error by comparing the phases of the burst signal and the demodulated color subcarrier, a digital oscillator having a control device which controls the limits of the integrated value from a cumulative integration device which outputs integrated values through cumulative integration of the second phase error signal based on the clock from the horizontal synchronization signal demodulation means, and a normalization circuit which normalizes the oscillation output of this digital oscillator using the first phase error signal, and feeds if back to the second phase comparator as the demodulated color subcarrier.

FIG. 1

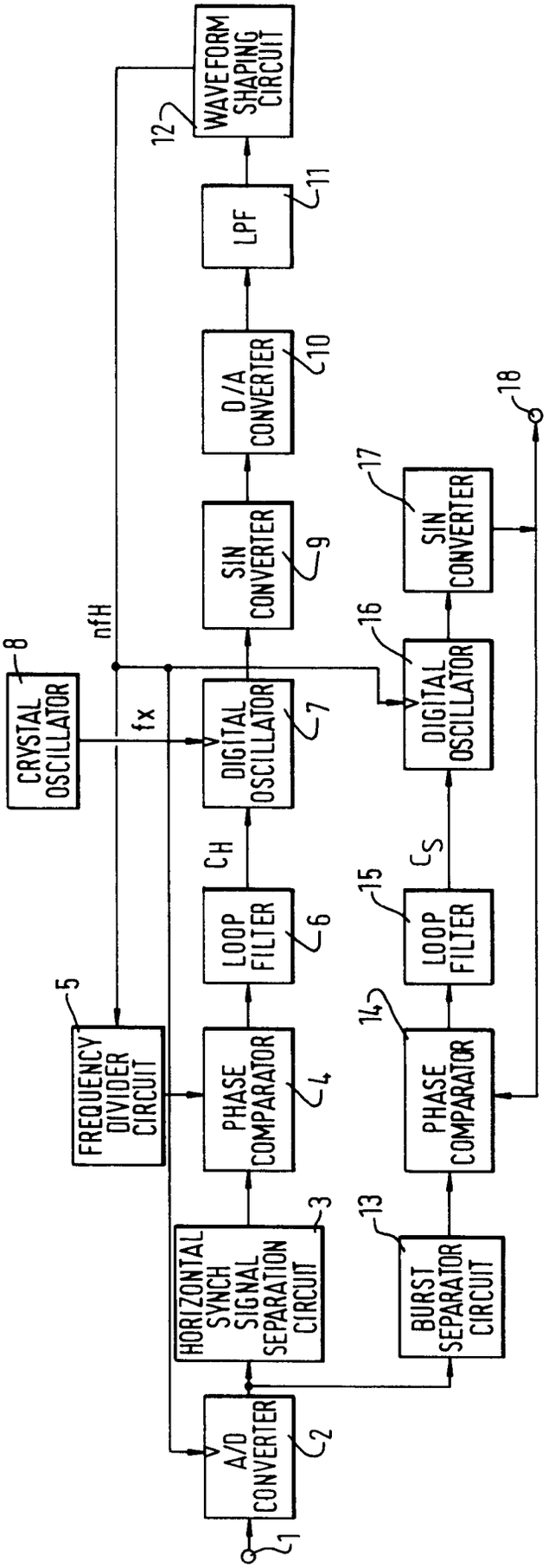
A/D CONVERTER
HORIZONTAL SYNCH SIGNAL SEPARATION CIRCUIT
BURST SEPARATOR CIRCUIT
PHASE COMPARATOR
PHASE COMPARATOR
FREQUENCY DIVIDER CIRCUIT
LOOP FILTER
LOOP FILTER
DIGITAL OSCILLATOR
DIGITAL OSCILLATOR
CRYSTAL OSCILLATOR
SIN CONVERTER
SIN CONVERTER
D/A CONVERTER
LPF
WAVEFORM SHAPING CIRCUIT
fx
nfH
CH
CS
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FIG.2

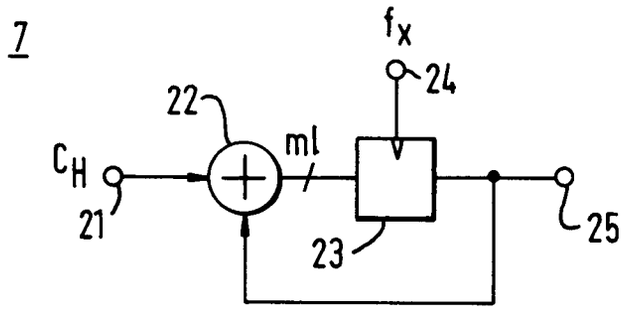


FIG.3

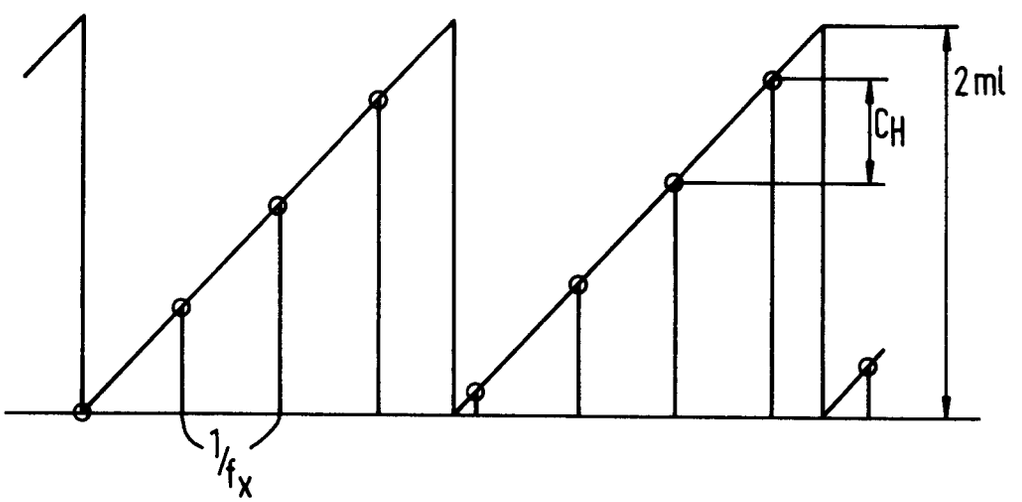
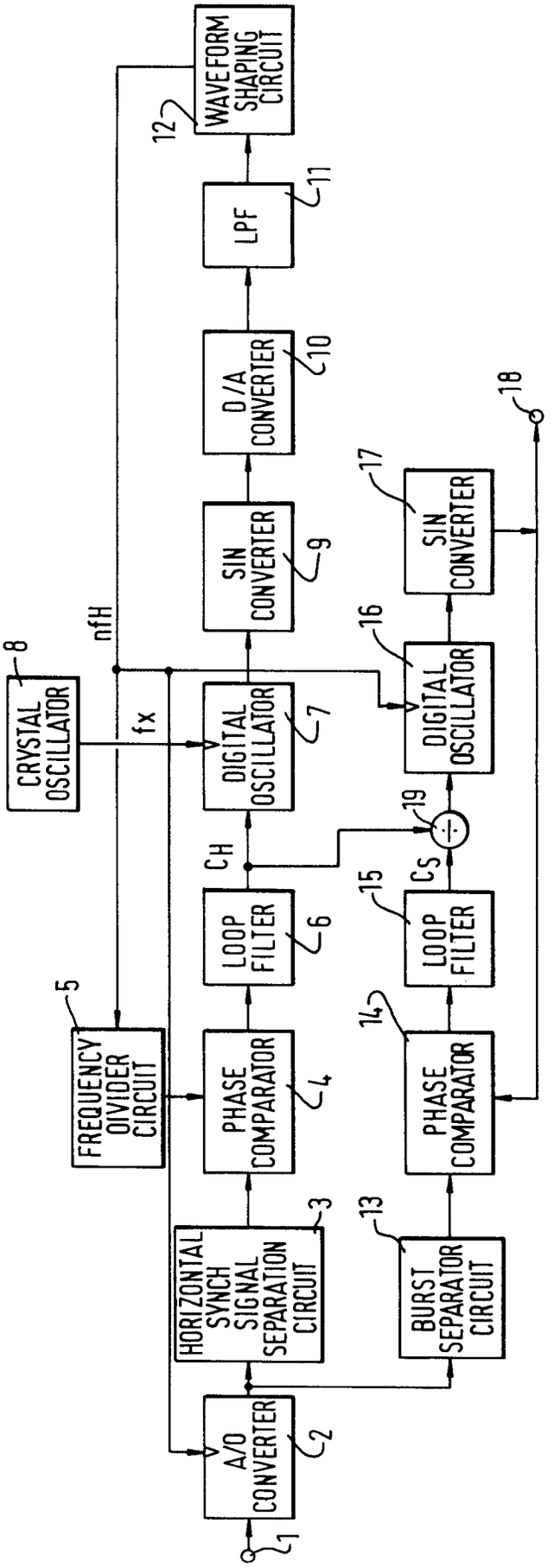


FIG. 4


1
A/D CONVERTER
2
HORIZONTAL SYNCH SIGNAL SEPARATION CIRCUIT
3
PHASE COMPARATOR
4
FREQUENCY DIVIDER CIRCUIT
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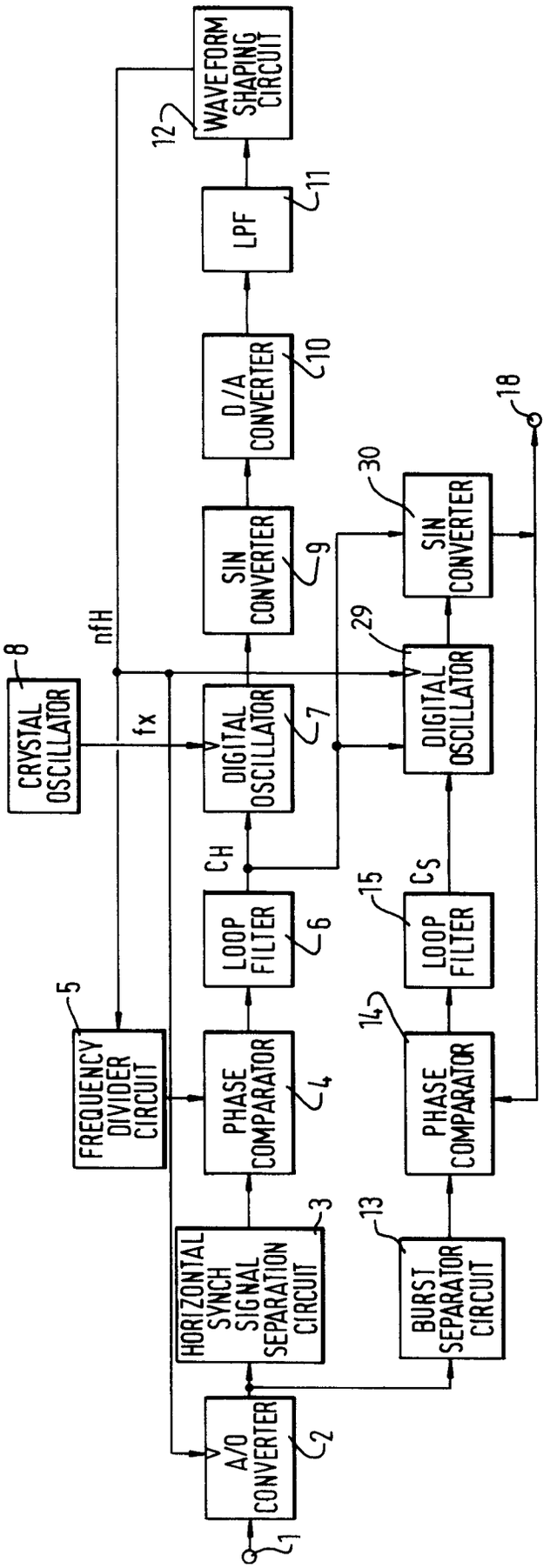
LOOP FILTER
6
DIGITAL OSCILLATOR
7
CRYSTAL OSCILLATOR
8
SIN CONVERTER
9
D/A CONVERTER
10
LPF
11
WAVEFORM SHAPING CIRCUIT
12
BURST SEPARATOR CIRCUIT
13
PHASE COMPARATOR
14
LOOP FILTER
15
DIGITAL OSCILLATOR
16
SIN CONVERTER
17
18
19
nfH
fx
CH
CS

FIG. 5


1
A/D CONVERTER
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HORIZONTAL SYNCH SIGNAL SEPARATION CIRCUIT
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PHASE COMPARATOR
4
FREQUENCY DIVIDER CIRCUIT
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LOOP FILTER
6
DIGITAL OSCILLATOR
7
CRYSTAL OSCILLATOR
8
SIN CONVERTER
9
D/A CONVERTER
10
LPF
11
WAVEFORM SHAPING CIRCUIT
12
BURST SEPARATOR CIRCUIT
13
PHASE COMPARATOR
14
LOOP FILTER
15
DIGITAL OSCILLATOR
29
SIN CONVERTER
30
18
nfH
fx
CH
CS

FIG. 6

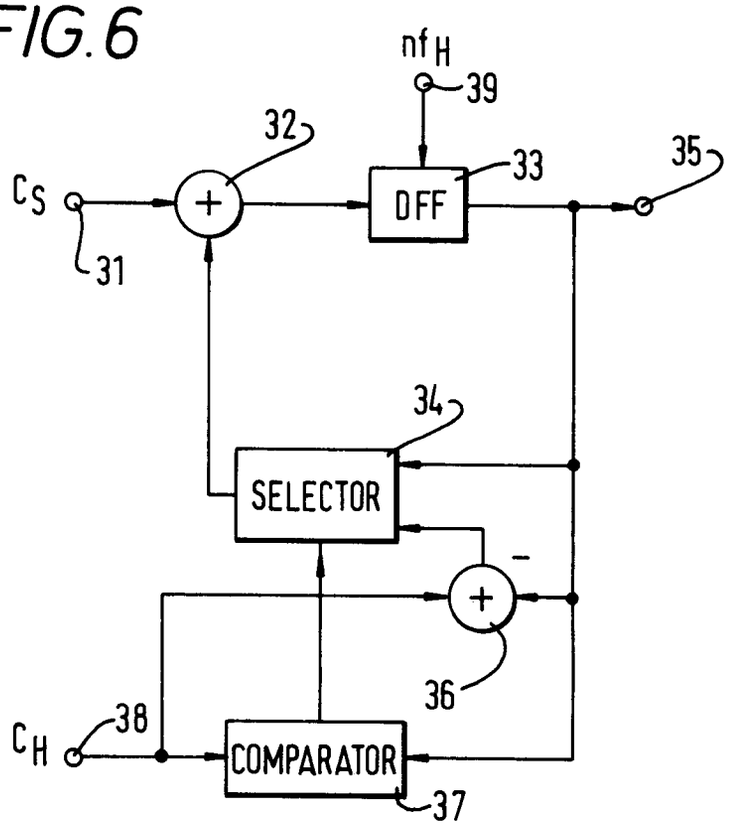
nf H
39
32
33
35
C S
31
DFF
34
SELECTOR
36
C H
38
COMPARATOR
37

FIG. 7

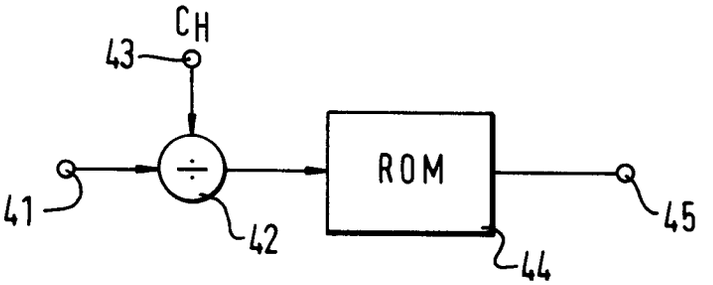
C H
43
41
42
ROM
44
45

FIG.8

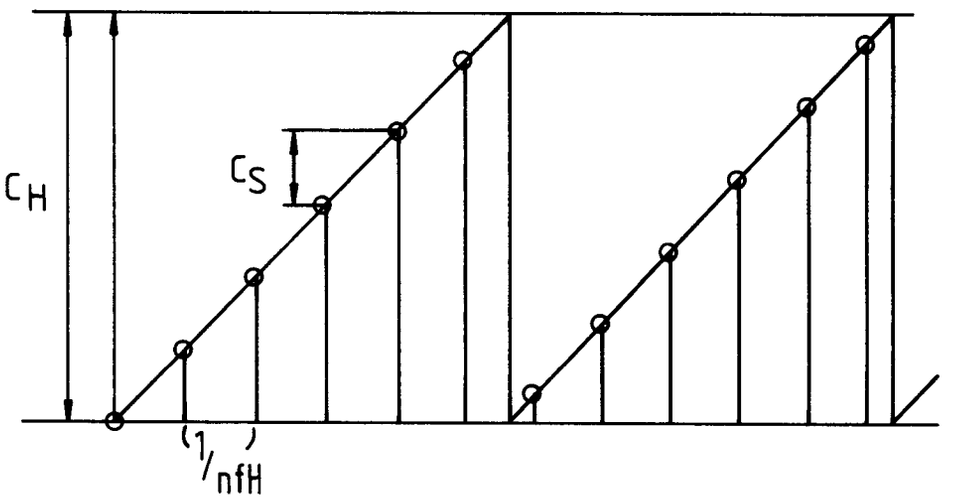

FIG.9