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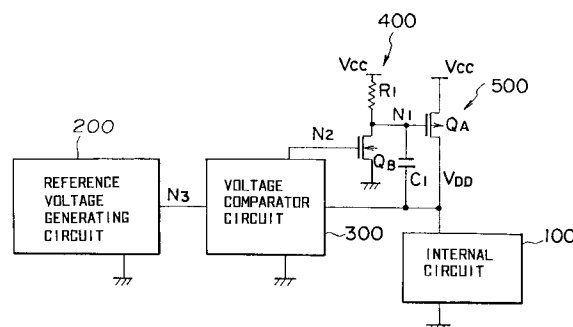
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SEMICONDUCTOR DEVICE AND BUILT-IN POWER CIRCUIT.

A power circuit to be preferably incorporated in a semiconductor device and for following noises due to the operation of an internal circuit serving as a load, which applies negative feedback to a variable resistance element (500) by a voltage comparator (300) and variable resistor driver (400) when the voltage V_{dd} applied to an internal circuit (100) due to the fluctuation of the supply voltage V_{cc} or operation of the internal circuit (100) fluctuates comparatively slowly. The circuit also quickly applies negative feedback to the variable resistance element (500) by a condenser (C1) for instantaneous fluctuation (noise) of the internal circuit applied voltage V_{dd} due to the operation of the internal circuit (100).

FIG. 1



FIELD OF THE INVENTION

The present invention pertains to a power circuit suitable for inclusion in a semiconductor apparatus, for example, in which circuit a follow-up characteristic with respect to noise caused by the operation of an internal load circuit is improved.

BACKGROUND ART

Recent demand for high integration and speed-up of electric circuits requires that a semiconductor apparatus is manufactured in a more and more refined manner. However, since the voltage used in a semiconductor apparatus does not vary in accordance with the scale of miniaturization, a problem of reliability inevitably surfaces because of the electric field concentration in a transistor of a very refined structure. Accordingly, a power supply by means of a so-called voltage drop circuit for supplying an externally applied voltage to an internal circuit after dropping the same voltage is desired in order to ensure reliability without changing the voltage used in a semiconductor apparatus.

Conventionally, a power circuit of this type comprises a variable resistance element, a reference voltage generating source, a comparator, and a resistance element driver, for the purpose of supplying a power supply voltage to an internal circuit.

A variable resistance element changes its value of resistance in response to a signal fed into its control input terminal inserted in the line which supplies power to an internal load circuit. A reference voltage generating source generates a reference voltage that serves as a reference for a voltage applied to the internal circuit. A comparator compares the reference voltage obtained from the reference voltage generating source with an applied voltage actually applied to the internal circuit. A resistance element driver drives the variable resistance element in accordance with an output signal from the comparator, thereby maintaining the applied voltage applied to the internal circuit at the same level on the basis of the variation of the value of resistance.

In such a power circuit, when a voltage V_{DD} (3V, normally) varies due to such causes as the variation of an externally supplied power supply voltage V_{CC} (5V, normally) or the operation of the internal circuit, a negative feedback is applied to the variable resistance element so as to cancel the variation, with the result that the applied voltage V_{DD} of the internal circuit is maintained at approximately the same level.

However, since it is impossible in such a conventional power circuit, to secure a large idling

current in the variable resistance element driver due to the requirement of power consumption reduction, there is a disadvantage in that a bad follow-up characteristic results with respect to an instantaneous variation (noise) of the internal circuit applied voltage V_{DD} , caused by the operation of the internal circuit, for example.

The present invention is designed to eliminate the above disadvantage, and the object thereof is to improve the follow-up characteristic of such a power circuit with respect to an instantaneous variation (noise) of the internal circuit applied voltage V_{DD} without increasing the idling current of the variable resistance driver.

DISCLOSURE OF THE INVENTION

The above object can be achieved by a configuration comprising: a variable resistance element whose resistance changes in response to a signal fed into its control input terminal inserted in the line which supplies power to an internal load circuit; a reference voltage generating source for generating a reference voltage that serves as a reference for an applied voltage applied to the internal circuit; a comparator for comparing the reference voltage obtained from the reference voltage generating source and the applied voltage applied to the internal circuit; a resistance element driver that drives the variable resistance element in accordance with the output signal of the comparator, thereby maintaining, in accordance with the variation of the resistance thereof, the applied voltage applied to the internal circuit at the same level; and a capacitor for negatively feeding back the applied voltage actually applied to the internal circuit to the control input terminal of the variable resistance element.

Accordingly, a follow-up characteristic of a power circuit of this type with respect to an instantaneous variation (noise) of the internal circuit applied voltage V_{DD} can be improved without increasing the idling current of the variable resistance element driver.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a diagram illustrating an embodiment of the present invention;

FIG.2 is a diagram illustrating examples of a reference voltage generating circuit, a voltage comparator circuit, and a variable resistance element driver of FIG.1;

FIG.3 is a diagram illustrating an example of an internal circuit of FIG.1;

FIG.4 is an illustration of waveforms showing variations of the states of each node, which variations are due to internal circuit noise;

FIG.5 is a schematic cross-sectional view of a p-channel MOSFET provided with a capacitor, which MOSFET is used in a semiconductor apparatus including the power circuit of the present invention;

FIG.6 is a diagram illustrating another embodiment of the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

FIG.1 is a diagram illustrating an embodiment of the present invention. Referring to FIG.1, a reference voltage generating circuit 200, which is a reference voltage generating source for generating a reference voltage N_3 that serves as a reference for a voltage applied to an internal load circuit 100 (embodied, for example, by an SRAM as mentioned in the following), is connected to a voltage comparator circuit 300 for comparing the reference voltage N_3 with an applied voltage V_{DD} (3V, normally) actually applied to the internal circuit 100.

The voltage comparator 300 is connected to a resistance element driver 400 for driving a variable resistance element Q_A (mentioned in the following) in accordance with an output signal N_2 of the comparator, thereby maintaining the applied voltage V_{DD} applied to the internal circuit 100 at the same level. As shown in the figure, this resistance element driver 400 comprises a resistance element R_1 and an n-channel MOSFET Q_B arranged in that order, when viewed from the external power supply voltage V_{CC} . The resistance element R_1 can be a p-channel MOSFET.

A variable resistance element 500 whose resistance varies in response to a signal fed to a control input terminal N_1 is inserted in a line supplying power to the internal circuit 100, which line leads from the external power supply voltage V_{CC} . This variable resistance element 500 comprises the p-channel MOSFET Q_A , as shown in the figure. A p-channel MOSFET is used in order to maintain the internal potential and the external potential of the internal circuit 100 at the same level.

A capacitor C_1 (100pF, for example) for negatively feeding back the applied voltage V_{DD} actually applied to the internal circuit 100 to the gate of the p-channel MOSFET Q_A , which gate embodies the control input terminal of the variable resistance element 500, is provided between the gate and the drain of the p-channel MOSFET Q_A .

In such a power circuit, when the voltage V_{DD} (3V, normally) applied to the internal circuit changes comparatively moderately due to such causes as the variation of the externally supplied power source voltage V_{CC} (5V, normally) or the operation of the internal circuit, a negative feedback is applied to the variable resistance element

500 (the p-channel MOSFET Q_A) via the voltage comparator 300 and the variable resistance element driver 400.

A rapid negative feedback is applied to the variable resistance element 500 (the p-channel MOSFET Q_A) via the capacitor C_1 in response to an instantaneous variation (noise) in the internal circuit applied voltage V_{DD} , which variation is due to the operation of the internal circuit 100, for example.

In this way, a follow-up characteristic with respect to an instantaneous variation (noise) in the applied voltage V_{DD} of the internal circuit 100 can be improved without increasing the idling current of the resistance element driver 400.

FIG.2 illustrates examples of the reference voltage generating circuit, the voltage comparator circuit, and the resistance element driver of FIG.1.

A p-channel MOSFET Q_{19} (Q_A), whose source terminal is connected to the external power source voltage V_{CC} and whose drain terminal is connected to the external circuit 100, is used as the variable resistance element 500, the gate terminal of the same MOSFET being supplied with a driving signal N_1 mentioned later.

The reference voltage generating source 200 is embodied by a constant-voltage circuit composed of an n-channel MOSFET series of three serially connected MOSFET's $Q_2 - Q_4$, the gates and the sources thereof being connected so as to manifest the function of a resistance element, and by a p-channel MOSFET Q_1 whose drain terminal is connected to an end of the n-channel MOSFET series $Q_2 - Q_4$, and whose gate terminal is connected to earth so as to manifest the function of a constant current source. The reference voltage N_3 is obtained at the point where the p-channel MOSFET Q_1 and the n-channel MOSFET series $Q_2 - Q_4$ are connected.

The voltage comparator 300 is embodied by a differential amplifier consisting of two pairs of p-channel MOSFET's of symmetric characteristics, namely (Q_5 and Q_{10}) and (Q_6 and Q_{11}) and of three pairs of n-channel MOSFET's of symmetric characteristics, namely (Q_7 and Q_{12}), (Q_8 and Q_{13}), and (Q_9 and Q_{14}). This configuration is of a so-called current mirror sense amplifier. This differential amplifier compares the reference voltage N_3 supplied to the gate terminals of the MOSFET Q_7 and the MOSFET Q_{13} , and the power source voltage V_{DD} supplied to the gate terminals of the MOSFET Q_8 and the MOSFET Q_{12} , the result of the comparison being output, as comparison result signals N_2 and N_2' , from the point where the MOSFET Q_5 and the MOSFET Q_7 are connected and from the point where the MOSFET Q_{10} and the MOSFET Q_{12} are connected.

The variable resistance element driver 400 is embodied by an amplifier circuit composed of a pair of n-channel MOSFET's (Q_{15} and Q_{17}) of symmetric characteristics and of a pair of n-channel MOSFET's (Q_{16} and Q_{18}) of symmetric characteristics. This amplifier amplifies the comparison result signal N_2 and N_2' supplied to the gate terminals of the MOSFET Q_{16} and the MOSFET Q_{18} , and supplies, as a driving signal N_1 , the amplified signal to the gate terminal of the MOSFET Q_{19} functioning as the variable resistance element 500.

One end of the capacitor C_1 , which is the essential part of the present invention, is connected to the point where the internal circuit 100 and the p-channel MOSFET Q_{19} functioning as the variable resistance element 500 are connected, i.e. the drain terminal of the p-channel MOSFET Q_{19} , and the other end of the capacitor C_1 is connected to the gate terminal of the p-channel MOSFET Q_{19} functioning as the variable resistance element 500.

Accordingly, when the applied voltage V_{DD} applied to the internal circuit 100 shows signs of rapidly increasing, the potential difference between the gate and the source of the p-channel MOSFET Q_{19} functioning as the variable resistance element 500 becomes small, and the source-drain resistance of the p-channel MOSFET Q_{19} increases so that the increase of the applied voltage V_{DD} applied to the internal circuit 100 is instantly checked. When the applied voltage V_{DD} applied to the internal circuit 100 shows signs of rapidly dropping, the gate-source potential difference of the p-channel MOSFET Q_{19} functioning as the variable resistance element 500 becomes great and the source-drain resistance of the p-channel MOSFET Q_{19} decreases so that the drop of the applied voltage V_{DD} applied to the internal circuit 100 is instantly checked.

FIG.3 illustrates an example of the internal circuit of FIG.1. The internal circuit 100 in FIG.3 is a basic circuit of an SRAM (static RAM).

In the figure, 110 represents an input buffer, 120 a decoder, 130 a cell array, 140 an amplifier, and 150 an output buffer.

The input buffer 110 is fed with inputs of address signals $A0 - A3$, a data D , a chip select signal CS and an enable signal WE , and consists of a row address buffer circuit 111, a column address buffer circuit 112, a data-in buffer circuit 113, a chip select buffer circuit 114, and a write enable buffer circuit 115.

The decoder 120 consists of a row decoder 121 and a column decoder 122, and selects a cell of the cell array 130 on the basis of an address signal.

The cell array 130 is where memory cells 131 (sixteen of them are shown in the figure) are arranged in the form of a matrix.

ranged in the form of a matrix.

The amplifier 140 consists of a write amplifier circuit 141 and two read sense amplifier circuits 142.

The output buffer 150 consists of a data-out buffer 151 for outputting the read data.

Circuit elements in the circuits described above constituting the internal circuit 100 in the form of an SRAM are driven by the power supply voltage V_{DD} .

FIG.4 is an illustration of waveforms showing variation of the states of each node, which variation is due to noise of the internal circuit. In FIG.4, (a) is a waveform illustration for the conventional circuit, (b) is a waveform illustration for the present invention, and the description is given below by comparing the two.

As is shown in FIG.4(a), in the conventional circuit, when the internal circuit applied voltage V_{DD} shows signs of a sharp drop, due to a rapid increase of power consumption in the internal circuit 100, at time t_1 accompanied by a rapid increase of the comparison result signal N_2 , the drop of the driving signal N_1 is more moderate than the increase of the comparison result signal N_2 , due to the delay in the operation of the variable resistance element driver 400. As a result, it takes a comparatively long time for the value of the internal circuit applied voltage V_{DD} to return to the original state.

Similarly, when the internal circuit applied voltage V_{DD} shows signs of a rapid increase due to a rapid drop of power consumption in the internal circuit 100, at time t_2 accompanied by a rapid drop of the comparison result signal N_2 , the increase of the driving signal N_1 is more moderate than the drop of the comparison result signal N_2 , due to the delay in the operation of the variable resistance element driver 400. As a result, it takes a comparatively long time for the value of the internal circuit applied voltage V_{DD} to return to the original state.

On the other hand, FIG.4 (b) shows that, in the circuit of this embodiment, when the internal circuit applied voltage V_{DD} shows signs of a rapid drop due to a rapid increase of power consumption of the internal circuit 100, at time t_1 , the accompanied increase of the comparison result signal N_2 is the same as that of the conventional circuit, but the driving signal N_1 shows an instantaneous drop at a greater rate than in the conventional circuit by virtue of the application of a rapid negative feedback effect of the capacitor C_1 . As a result, it takes a comparatively short time for the value of the internal circuit applied voltage V_{DD} to return to the original state.

Similarly, when the internal circuit applied voltage V_{DD} shows signs of a rapid increase due to a rapid drop of power consumption in the internal

circuit 100, at time t_2 , the accompanied drop of the comparison result signal N_2 is the same as that of the conventional circuit, but the driving signal N_1 shows an instantaneous increase at a greater speed than in the conventional circuit by virtue of a rapid negative feedback effect of the capacitor C_1 . As a result, it takes a comparatively short time for the value of the internal circuit applied voltage V_{DD} to return to the original state.

While it is possible to provide the p-channel MOSFET's Q_A and Q_{19} , and the capacitor C_1 separately and connect them afterwards, it is also possible to form them as one element as is shown in FIG.5.

FIG.5 is a schematic cross-sectional view of a p-channel MOSFET provided with a capacitor, which MOSFET is used in a semiconductor apparatus including a power circuit of the present invention.

The p-channel MOSFET's Q_A and Q_{19} shown in FIGS. 1 and 2 are fabricated such that a high-density source area 602 and a drain area 603 are formed on the face of an n-type silicon base 601 by means of ion implantation, for example.

When the gate electrode 604 is of a so-called poly-side gate, a polycrystalline silicon film 604a constituting the gate 604 is formed on the surface of a gate oxide film between the source area 602 and the drain area 603. A metal electrode film 604b is then formed on the polycrystalline silicon film 604a by deposition, for example.

The polycrystalline silicon film 604a should be formed such that it is in extensive contact with the drain area 603. The gate-drain electric capacitance is determined in correspondence with this contact area. The state of the circuit thus prepared becomes virtually the same as when the capacitor C_1 is connected between the gate and the drain.

The external power source voltage V_{CC} is applied to the source area 602, and the drain area 603 supplies the internal power source voltage V_{DD} in accordance with the driving signal N_1 input into the gate 604.

FIG.6 is a diagram illustrating another embodiment of the present invention. One notable configuration shown in FIG.6 is such that a resistance element R_2 is inserted in a signal line leading from the variable resistance element driver 400, while the other configurations remain the same as in FIG.2. This resistance element R_2 acts to absorb the noise superimposed on a feedback signal from the variable resistance element driver 400 so that the feedback effect of the capacitor C_1 is augmented.

POSSIBLE APPLICATION IN THE INDUSTRY

As has been described, a power circuit of the present invention is useful when it is intended that there should be a close follow-up on an instantaneous variation (noise) of the internal circuit applied voltage without increasing an idling current of the variable resistance element driver.

Claims

1. A power circuit comprising:
 - a variable resistance element (500) inserted in a power supplying line leading to a load, the value of resistance thereof varying in response to a signal (N_1) input into a control input terminal of the element;
 - a reference voltage generating source (200) for generating a reference voltage (N_3) that serves as a reference for an applied voltage applied to said load;
 - a comparator (300) for comparing the reference voltage (N_3) obtained from said reference voltage generating source (200) and the applied voltage (V_{DD}) applied to said load;
 - a resistance element driver (400) for driving, in accordance with an output signal (N_2) from said comparator (300), said variable resistance element (500) and maintaining, in accordance with the variation of the value of resistance thereof, the applied voltage (V_{DD}) applied to said load at the same level; and
 - a capacitor (C_1) for negatively feeding back the applied voltage (V_{DD}) applied to said load to the control input terminal of said variable resistance element (500).
2. A power circuit as claimed in Claim 1, wherein a resistance element (R_2) for augmenting the feedback effect of said capacitor (C_1) is provided on a signal line leading from said resistance element driver (400).
3. A power circuit as claimed in Claim 1 or Claim 2, wherein said load is a memory circuit and a power supply for supplying a normal operation voltage to said memory circuit is connected to said power supplying line.
4. A power circuit as claimed in any of Claims 1 to 3, wherein said comparator (300) is formed from a current mirror sense amplifier.
5. A power circuit as claimed in any of Claims 1 to 4, wherein said resistance element driver (400) consists of a resistance element (R_1) inserted between the power supply potential and the ground potential, and of an n-channel

transistor, said n-channel transistor being turned on and off in accordance with said output signal (N2),

said signal (N1) is extracted from a connect point where the resistance element (R1) and said n-channel transistor meet; and

all the element including said resistance element (R1) are formed as a MOS element.

6. A semiconductor apparatus including a power circuit as claimed in Claims 1 through 5 comprising:

a source area (602) and a drain area (603) formed on a base (601), the variable resistance element (500) of the power circuit as claimed in any of Claims 1 to 5 being formed on said base (601), and

a gate (604) provided between said source area (602) and said drain area (603) and formed in such a manner as to be in extensive contact with said drain area (603) so as to have an electric capacitance.

Amended claims

1. A power circuit comprising:

a variable resistance element (500) inserted in a power supplying line leading to a load, the value of resistance thereof varying in response to a signal (N₁) input into a control input terminal of the element;

a reference voltage generating source (200) for generating a reference voltage (N₃) that serves as a reference for an applied voltage applied to said load;

a comparator (300) for comparing the reference voltage (N₃) obtained from said reference voltage generating source (200) and the applied voltage (V_{DD}) applied to said load;

a resistance element driver (400) for driving, in accordance with an output signal (N₂) from said comparator (300), said variable resistance element (500) and maintaining, in accordance with the variation of the value of resistance thereof, the applied voltage (V_{DD}) applied to said load at the same level;

a capacitor (C₁) for negatively feeding back the applied voltage (V_{DD}) applied to said load to the control input terminal of said variable resistance element (500); and

a resistance element (R₂) for augmenting the feedback effect of said capacitor (C₁) is provided on a signal line leading from said resistance element driver (400).

3. A power circuit as claimed in Claim 1, wherein said load is a memory circuit and a power supply for supplying a normal operation voltage to said memory circuit is connected to

said power supplying line.

4. A power circuit as claimed in Claim 1 or Claim 3, wherein said comparator (300) is formed from a current mirror sense amplifier.

5. A power circuit as claimed in Claim 1, Claim 3, or Claim 4, wherein said resistance element driver (400) consists of a resistance element (R1) inserted between the power supply potential and the ground potential, and of an n-channel transistor, said n-channel transistor being turned on and off in accordance with said output signal (N2),

said signal (N1) is extracted from a connect point where the resistance element (R1) and said n-channel transistor meet; and

all the element including said resistance element (R1) are formed as a MOS element.

6. A semiconductor apparatus including a power circuit as claimed in any of Claim 1 and Claims 3 - 5 comprising:

a source area (602) and a drain area (603) formed on a base (601), the variable resistance element (500) of the power circuit as claimed in any of Claims 1 to 5 being formed on said base (601), and

a gate (604) provided between said source area (602) and said drain area (603) and formed in such a manner as to be in extensive contact with said drain area (603) so as to have an electric capacitance.

FIG. 1

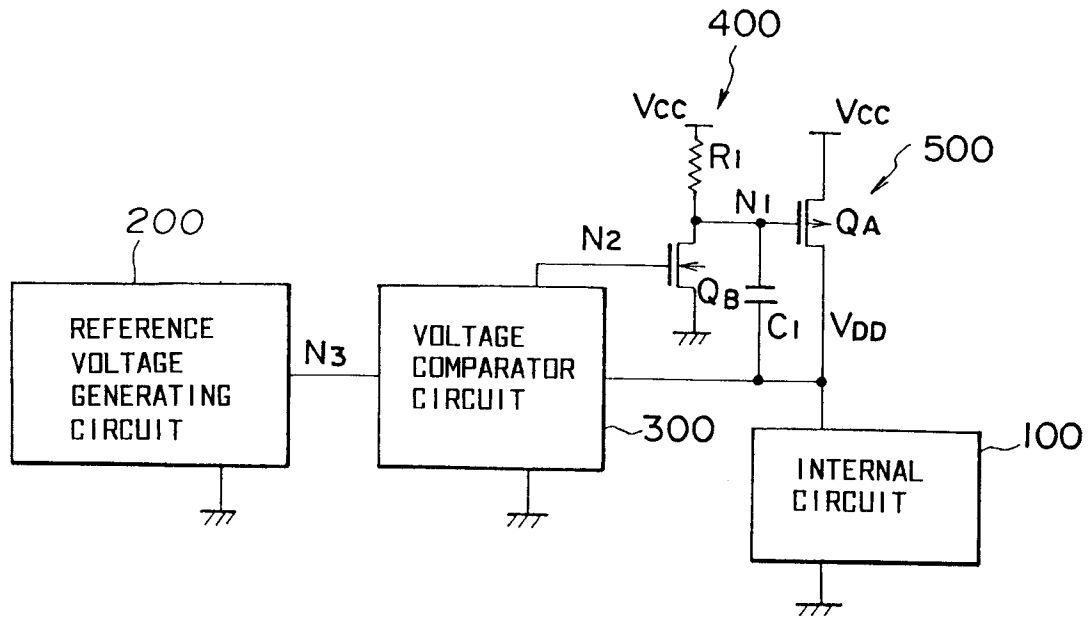


FIG. 2

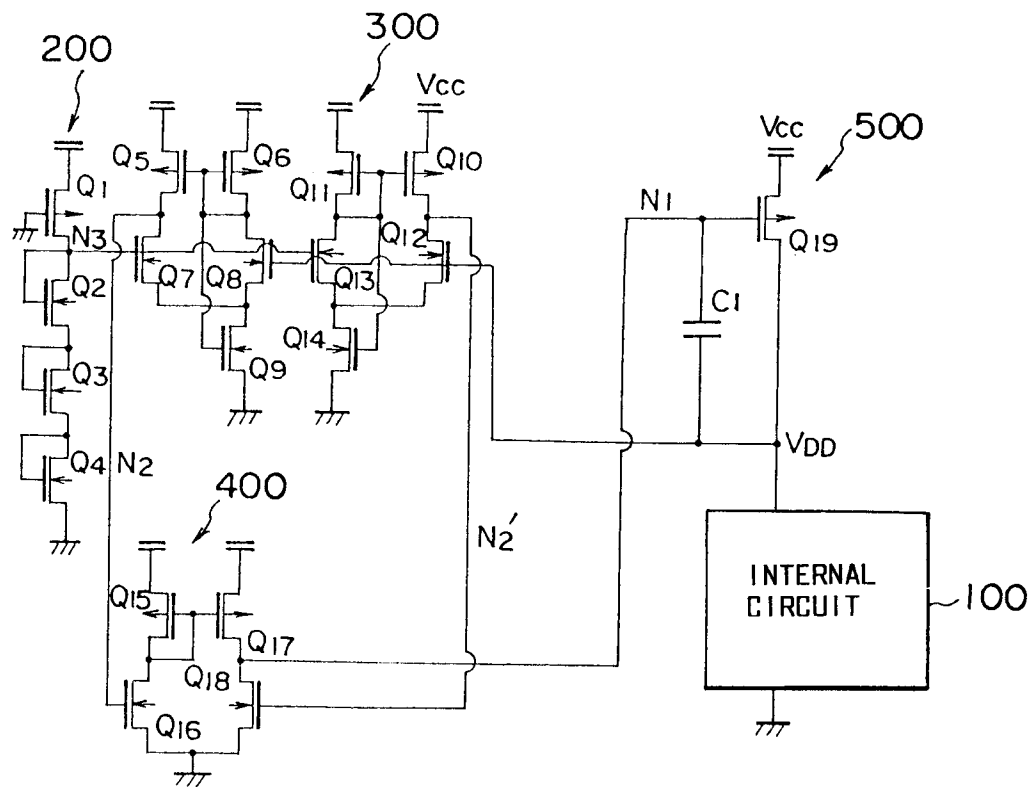


FIG. 3

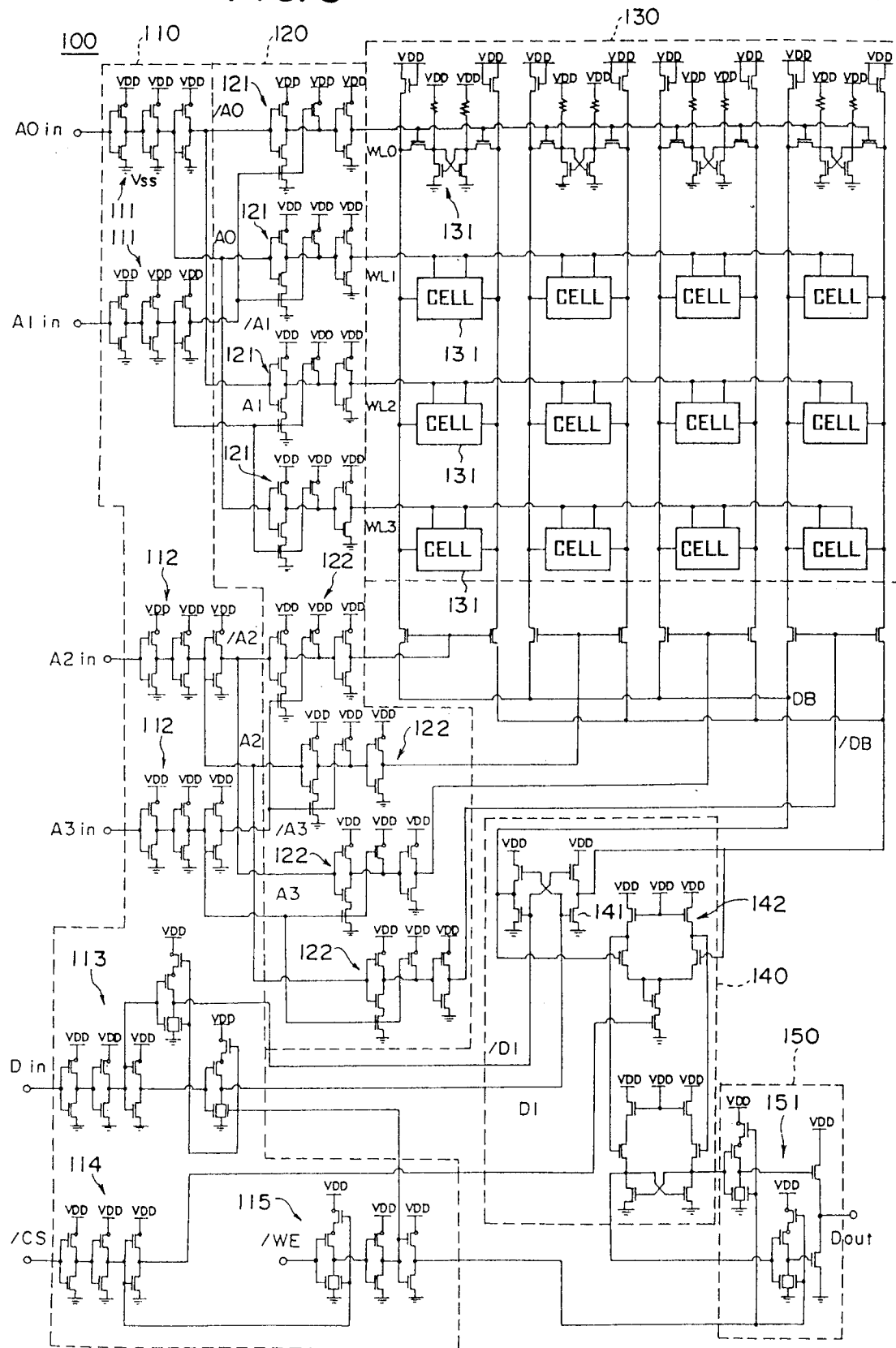


FIG. 4

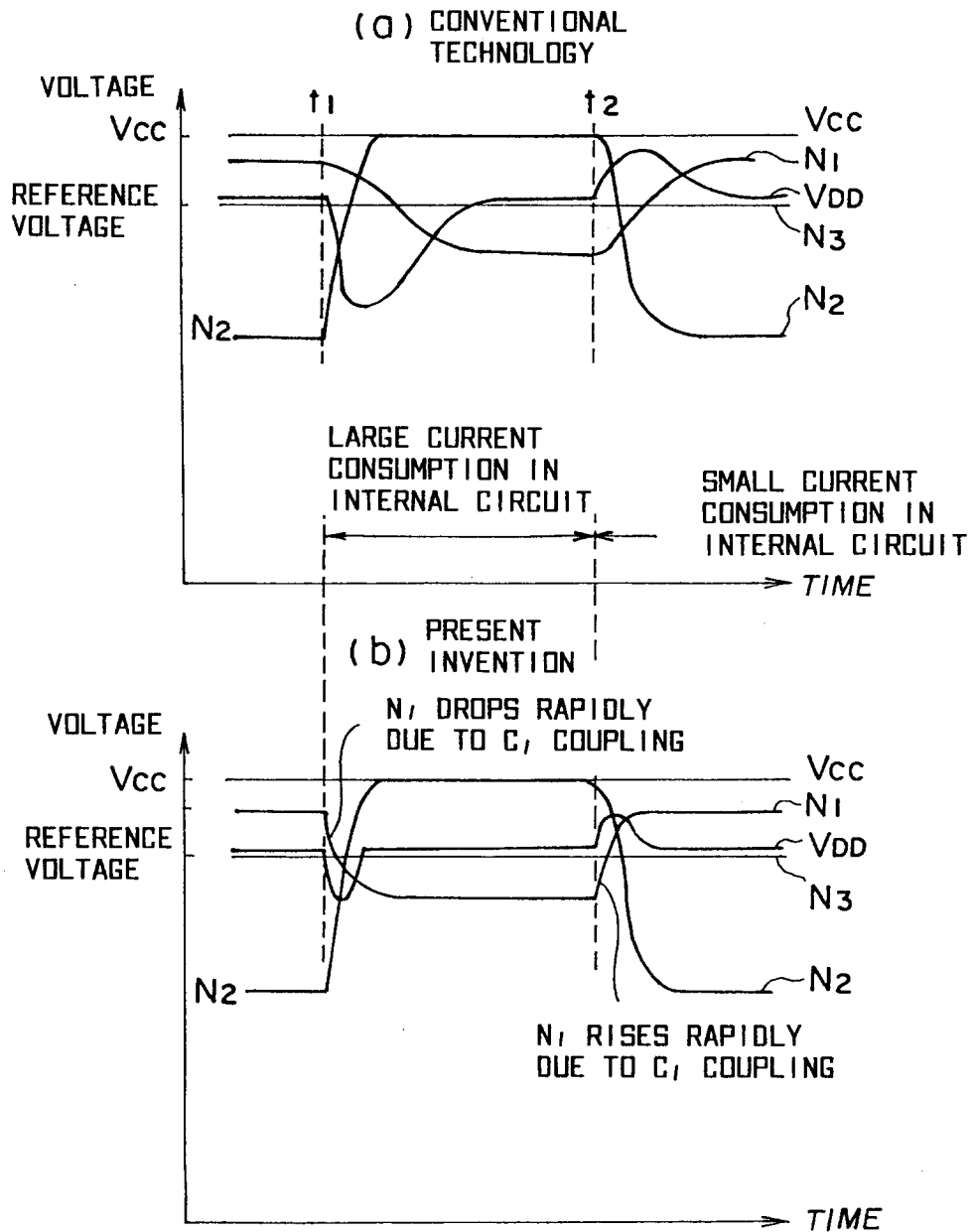


FIG. 5

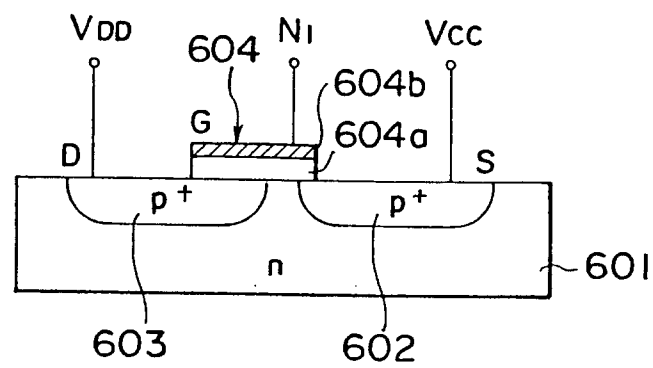
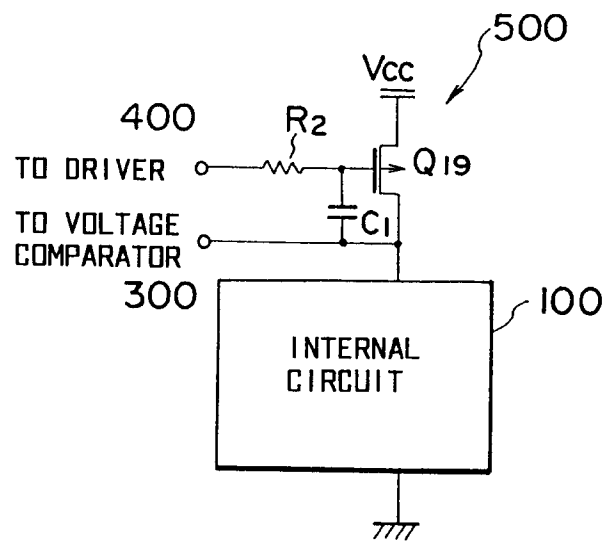


FIG. 6



INTERNATIONAL SEARCH REPORT

International Application No PCT/JP92/00326

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
Int. Cl ⁵ G05F1/56		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC	G05F1/56	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
Jitsuyo Shinan Koho 1926 - 1991 Kokai Jitsuyo Shinan Koho 1971 - 1991		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
X	JP, A, 63-316113 (Seiko Instruments Inc.), December 23, 1988 (23. 12. 88)	1-6
<p>¹⁰ Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
June 16, 1992 (16. 06. 92)	June 23, 1992 (23. 06. 92)	
International Searching Authority	Signature of Authorized Officer	
Japanese Patent Office		