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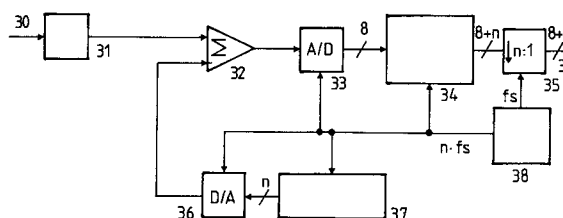
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W-3000 Hannover 91 (DE)(54) **Method and apparatus for A/D and D/A conversion.**

(57) Today's consumer video A/D and D/A converters or other digital video processing systems are restricted to 8-bit resolution. The quantizing noise introduced in these systems can result in visible artefacts in gradually shaped areas of an image or can lead in applications based on some critical algorithms to very severe distortions.

It is known to use a dither signal for masking contouring or correlation effects by adding a non-correlated noise signal to the video signal prior to A/D conversion.

For achieving an increased bit resolution for a given A/D or D/A converter, a special multilevel dither signal in conjunction with multiple oversampling is added to the bandlimited analog input signal which is afterwards converted with a clock rate of $n \cdot f_s$ and to the digital input signal, respectively.

**Fig.3****EP 0 543 220 A1**

The present invention relates to a method and to an apparatus for A/D and D/A conversion.

Background

Today's consumer video A/D and D/A converters or other digital video processing systems are restricted to 8-bit resolution. The quantizing noise introduced in these systems can result in visible artefacts in gradually shaped areas of an image or can lead in applications based on some critical algorithms to very severe distortions.

It is known to use a dither signal for masking contouring or correlation effects by adding a non-correlated noise signal to the video signal prior to A/D conversion.

Invention

It is one object of the invention to disclose an improved method for A/D conversion. This object is reached by the inventive method disclosed in claim 1.

In principle this inventive method consists in an improvement of the bit resolution of an A/D conversion with an effective sampling frequency f_s of the digital output signal, characterized in that a D/A converted periodic signal with 'n' steps and a sampling frequency of $n \cdot f_s$ is added to the analog signal prior to said A/D conversion with 'm' bit resolution and a sampling frequency of $n \cdot f_s$ and that the A/D converted digital signal is filtered to an output signal with $m+n$ bits resolution and subsampled with said effective sampling frequency f_s , whereby the response of said filtering has high attenuation or zero crossings at multiples of said effective sampling frequency f_s , except for frequencies $m \cdot n \cdot f_s$, $m = 0, \pm 1, \pm 2, \pm 3, \dots$, and whereby the amplitude of said periodic signal equals the amplitude of the LSB of said A/D conversion.

Advantageous additional embodiments of this inventive method are resulting from the respective dependent claim.

It is a further object of the invention to disclose an improved method for D/A conversion. This object is reached by the inventive method disclosed in claim 2.

In principle this inventive method consists in a D/A conversion with improvement of the bit resolution and an effective sampling frequency f_s of the digital input signal, characterized in that said input signal has a resolution of $m+n$ bits and is oversampled with a frequency of $n \cdot f_s$ and interpolated and added to a periodic signal with 'n' steps and a sampling frequency of $n \cdot f_s$, and that the sum signal with $m+n$ bit resolution is quantized to a signal with the 'm' most significant bits, which is D/A

converted with 'm' bit resolution and a sampling frequency of $n \cdot f_s$, whereby the amplitude of said periodic signal equals the amplitude of the LSB of said A/D conversion.

Advantageous additional embodiments of this inventive method are resulting from the respective dependent claim.

It is a further object of the invention to disclose an apparatus which utilizes the inventive A/D conversion method. This object is reached by the inventive A/D converter disclosed in claim 4.

In principle the inventive A/D converter consists of a summing circuit which receives the analog input signal and the output signal of a D/A converter which works with a clock frequency of $n \cdot f_s$, of an A/D converter with 'm' bits resolution which oversamples with a sampling frequency $n \cdot f_s$ and which is connected to the output of said summing circuit, of a conversion filter connected to the output of said A/D converter which adds 'n' bits to the 'm' input bits and which has high attenuation or zero crossings at multiples of said effective sampling frequency f_s , except for frequencies $m \cdot n \cdot f_s$, $m = 0, \pm 1, \pm 2, \pm 3, \dots$, of a following subsampler with a factor of 'n' which outputs a digital signal with $m+n$ bits resolution and a clock frequency f_s , and of a periodic signal generator which is connected to the input of said D/A converter, whereby the amplitude of the periodic signal generated in said periodic signal generator equals the amplitude of the LSB of said A/D converter.

Advantageous additional embodiments of this A/D converter are resulting from the respective dependent claim.

It is a further object of the invention to disclose an apparatus which utilizes the inventive D/A conversion method. This object is reached by the inventive D/A converter disclosed in claim 5.

In principle the inventive D/A converter consists of an oversampler which receives a digital signal with a clock frequency of f_s and a m -bit resolution and which generates a signal with a clock rate $n \cdot f_s$, of a following conversion filter which interpolates the new samples generated in said oversampler and outputs a signal with $m+n$ bits resolution, of an adder which adds a periodic signal with n bits resolution and $n \cdot f_s$ clock frequency generated in a periodic signal generator to the output signal of said conversion filter, of a following quantizer which takes the 'm' most significant bits from the output signal of said adder, of a following D/A converter with a clock frequency $n \cdot f_s$ and a m -bit resolution, whereby the amplitude of the periodic signal generated in said periodic signal generator equals the amplitude of a half LSB of said D/A converter.

Advantageous additional embodiments of this D/A converter are resulting from the respective dependent claim.

For achieving an increased bit resolution for a given A/D or D/A converter, a special multilevel dither signal in conjunction with multiple oversampling is added to the bandlimited analog input signal which is afterwards converted with a clock rate of $n \cdot f_s$ and to the digital input signal, respectively.

Drawings

Preferred embodiments of the invention will now be described with reference to the accompanying drawings, in which:

- Fig. 1 shows generally a digital video processing system;
- Fig. 2 shows the special multilevel dither signal;
- Fig. 3 depicts an inventive A/D converter;
- Fig. 4 shows the features of a conversion filter;
- Fig. 5 depicts an inventive D/A converter;
- Fig. 6 gives an illustration of the inventive conversion.

Preferred embodiments

In Fig. 1 an analog input signal 10 becomes A/D converted in an A/D converter 11 which outputs respective digital signals with 8-bit resolution. The digital signals are processed in a digital unit 12 and fed with 8-bit resolution to an D/A converter 14 which outputs analog output signals 15. A/D converter 11, digital unit 12 and D/A converter 14 are controlled with a clock f_s coming from a clock generator 13.

The special dither signal in Fig. 2 is represented by a staircase ramp signal 21 with an maximum amplitude 20 equalling a half LSB (least significant bit) amplitude of the A/D or D/A converter used. The clock $1/(n \cdot f_s)$ of the dither signal is n times higher than the sampling clock f_s necessary to fulfill the sampling theorem for the analog input signal. The sequence of the staircase steps can also be arranged in another way.

The term 'dither' signal used in this context differs from the normal applications of dither signals used.

In Fig. 3 the inventive A/D converter receives an analog input signal 30 which is filtered in lowpass filter 31 with a cut frequency f_{co} , $f_{co} \leq 2 \cdot f_s$. The output signal of this filter is fed to the first input of a summing circuit 32. The output of this circuit is connected to an A/D converter 33 which oversamples with factor ' n '. The 8-bit output signal is filtered in a conversion filter 34 which adds n bits to the eight input bits, resulting in a word size of $8+n$ bits. Conversion filter 34 has a frequency response as indicated in Fig. 4. The $8+n$ bit output signal of filter 34 is sampled in subsampler 35 with

a factor of ' n '.

In an n -bit counter 37 a staircase dither signal is generated and fed via D/A converter 36 to the second input of summing circuit 32. A clock generator 38 provides subsampler 35 with the clock frequency f_s and the conversion filter 34, A/D converter 33, counter 37 and D/A converter 36 with the clock frequency $n \cdot f_s$. The output signal 39 of subsampler 35 has a resolution of $8+n$ bits.

The response of conversion filter 34 in Fig. 4 must have a high attenuation or, better, zero crossings at multiples of frequency f_s , except for frequencies $m \cdot n \cdot f_s$, $m = 0, \pm 1, \pm 2, \pm 3, \dots$. Since the input video signal has been n times oversampled the filter output signal can be downsampled afterwards without losing the increased bit resolution.

Fig. 6 will be used for a better understanding of the inventive idea. The conversion curve is depicted in the domain 'quantized amplitude' 601 over 'input amplitude' 602 of the A/D converter. The video signal is assumed to have a DC input level 62. By means of a two level (1 bit) dither signal 63 with a peak-to-peak amplitude of $1/2$ LSB of the succeeding A/D converter the bit resolution of the A/D conversion can be increased by 1 bit. Due to the superimposed dither signal 63 the unfiltered output signal 64 of the A/D converter will vary in its amplitude by one bit, if the DC level 62 of the input signal 63 is smaller than $1/4$ LSB or greater than $3/4$ LSB within the corresponding quantizing interval. In Fig. 6 the DC level 62 is assumed to be greater than $3/4$ LSB within the corresponding quantizing interval. That leads to an oscillation of the output signal with a peak-to-peak value of 1 LSB. The following conversion filtering will completely suppress this oscillation due to its zero crossings in the frequency response. The resulting output signal can then supply an intermediate DC level 61 which corresponds with an increased resolution by 1 bit.

The inventive D/A converter in Fig. 5 receives a digital input signal 50 with $8+n$ bit resolution. In oversampler 51 this signal is sampled with a clock rate n times higher than before. The new samples are interpolated in a conversion filter 52 which outputs $8+n$ bit words. In adder 53 a special n -bit multilevel dither signal according to Fig. 2 and generated in n -bit counter 58 is added to the output signal of filter 52. A quantizer 54 takes the eight most significant bits from each $8+n$ bit word and is connected with its output to D/A converter 55. The following analog lowpass filter 56 suppresses in the output signal 59 all the harmonics introduced by the dither signal.

A clock frequency $n \cdot f_s$, which can be generated in a frequency multiplier 57 from the clock frequency f_s , is fed to oversampler 51, conversion filter 52,

counter 58, quantizer 54 and D/A converter 55.

The invention can be applied e.g. to digital SECAM decoding in TV receivers or VCR's, in which a composite signal is converted to 8-bit words. The FM modulated colour subcarrier with its small amplitude, which is included in the composite signal, is subjected to a high degree of quantizing noise. This poses serious problems for the FM demodulation and results in 'coloured fishes' in the reconstructed pictures. To overcome the perceived inadequacy of the 8-bit quantization a word size is necessary large enough to ensure that the noise generation is insignificant in the normal processing and that the maintenance of the quality is given also in critical conditions. Also for other TV standards, e.g. PAL and NTSC, the invention can be applied.

Claims

1. Method for A/D conversion with improvement of bit resolution and an effective sampling frequency f_s of the digital output signal (39), **characterized in** that a D/A converted (36) periodic signal (21) with 'n' steps and a sampling frequency of $n \cdot f_s$ is added (32) to the analog signal prior to a A/D conversion (33) with 'm' bit resolution and a sampling frequency of $n \cdot f_s$ and that the A/D converted digital signal is filtered (34) to an output signal with $m+n$ bits resolution and subsampled (35) with said effective sampling frequency f_s , whereby the response of said filtering has high attenuation or zero crossings at multiples of said effective sampling frequency f_s , except for frequencies $m \cdot n \cdot f_s$, $m = 0, \pm 1, \pm 2, \pm 3, \dots$, and whereby the amplitude (20) of said periodic signal (21) equals the amplitude of the LSB of said A/D conversion (33).
2. Method for D/A conversion with improvement of bit resolution and an effective sampling frequency f_s of the digital input signal (50), **characterized in** that said input signal (50) has a resolution of $m+n$ bits and is oversampled (51) with a frequency of $n \cdot f_s$ and interpolated (52) and added (53) to a periodic signal (21) with 'n' steps and a sampling frequency of $n \cdot f_s$, and that the sum signal with $m+n$ bit resolution is quantized (54) to a signal with the 'm' most significant bits, which is D/A converted (55) with 'm' bit resolution and a sampling frequency of $n \cdot f_s$, whereby the amplitude (20) of said periodic signal (21) equals the amplitude of the LSB of said A/D conversion (55).
3. Method according to claim 1 or 2, **characterized in** that said periodic signal (21) is a staircase ramp signal.
4. Apparatus for A/D conversion according to claim 1 or 3, consisting of a summing circuit (32) which receives the analog input signal (30) and the output signal of a D/A converter (36) which works with a clock frequency of $n \cdot f_s$, of an A/D converter (33) with 'm' bits resolution which oversamples with a sampling frequency $n \cdot f_s$ and which is connected to the output of said summing circuit (32), of a conversion filter (34) connected to the output of said A/D converter (33) which adds 'n' bits to the 'm' input bits and which has high attenuation or zero crossings at multiples of said effective sampling frequency f_s , except for frequencies $m \cdot n \cdot f_s$, $m = 0, \pm 1, \pm 2, \pm 3, \dots$, of a following subsampler (35) with a factor of 'n' which outputs a digital signal with $m+n$ bits resolution and a clock frequency f_s , and of a periodic signal generator (37) which is connected to the input of said D/A converter (36), whereby the amplitude (20) of the periodic signal (21) generated in said periodic signal generator (37) equals the amplitude of a half LSB of said A/D converter (33).
5. Apparatus for D/A conversion according to claim 2 or 3, consisting of an oversampler (51) which receives a digital signal with a clock frequency of f_s and a m -bit resolution and which generates a signal with a clock rate $n \cdot f_s$, of a following conversion filter (52) which interpolates the new samples generated in said oversampler (51) and outputs a signal with $m+n$ bits resolution, of an adder (53) which adds a periodic signal with n bits resolution and $n \cdot f_s$ clock frequency generated in a periodic signal generator (58) to the output signal of said conversion filter (52), of a following quantizer (54) which takes the 'm' most significant bits from the output signal of said adder (53), of a following D/A converter (55) with a clock frequency $n \cdot f_s$ and a m -bit resolution, whereby the amplitude (20) of the periodic signal (21) generated in said periodic signal generator (58) equals the amplitude of a half LSB of said D/A converter (55).
6. Apparatus according to claim 4 or 5, **characterized in** that said periodic signal generator (37, 58) is a n -bit counter.

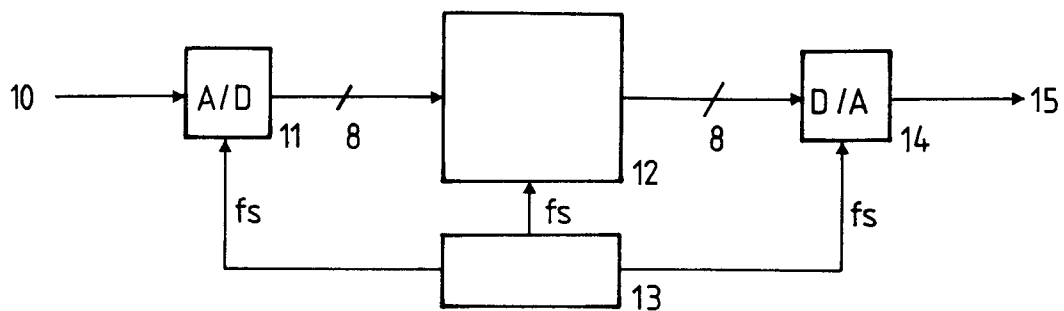


Fig.1

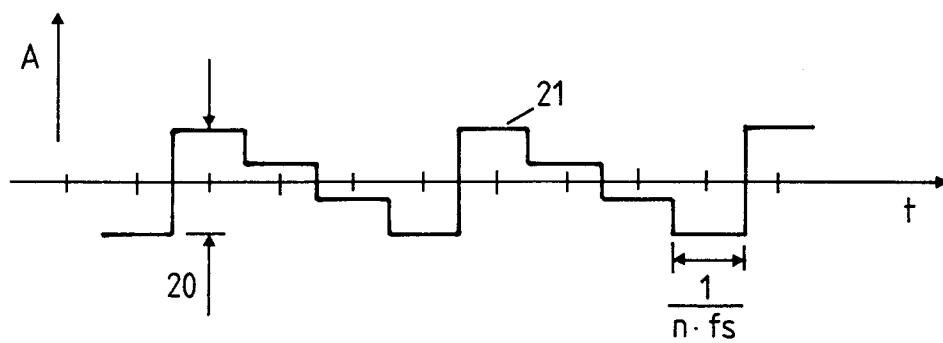


Fig.2

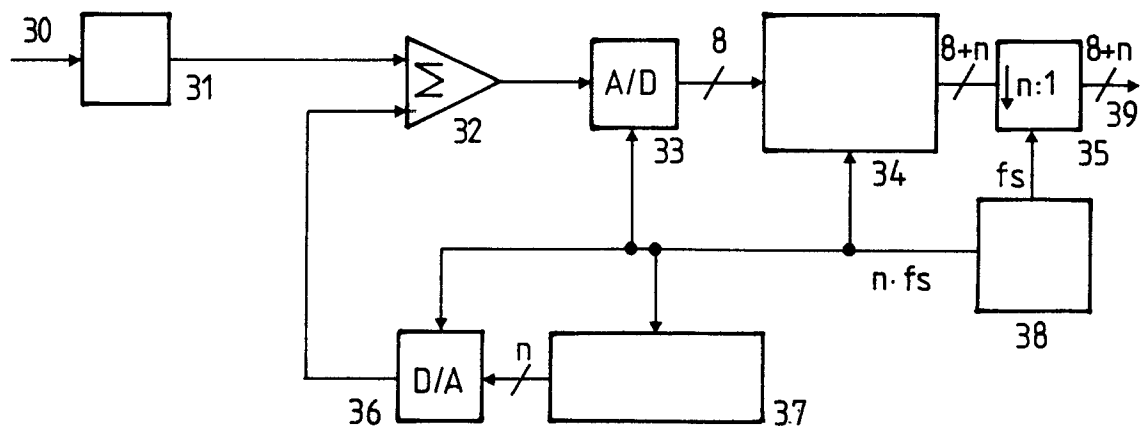


Fig.3

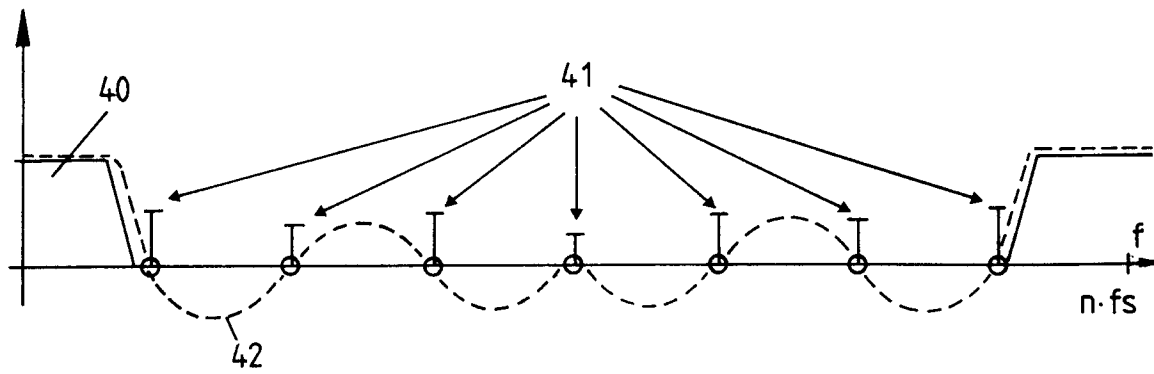


Fig.4

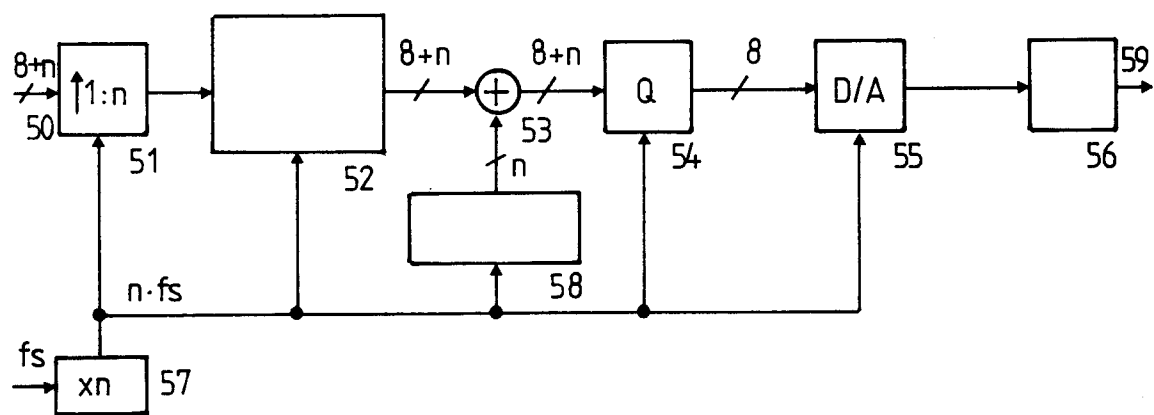


Fig.5

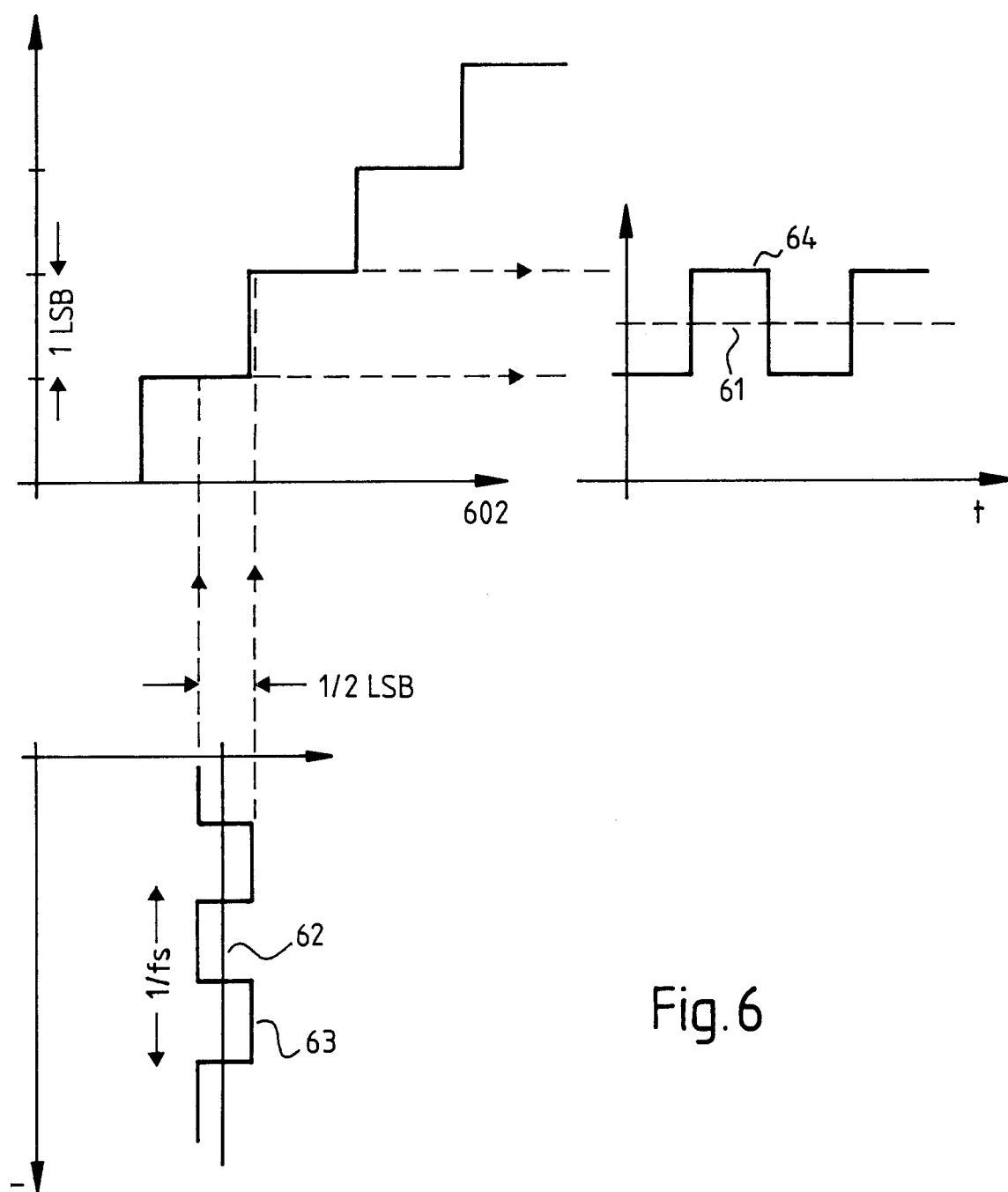


Fig.6



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EUROPEAN SEARCH REPORT

Application Number

EP 92 11 8855

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	PATENT ABSTRACTS OF JAPAN vol. 16, no. 108 (E-1179)17 March 1992 & JP-A-32 83 822 (TOSHIBA) 13 December 1991 * abstract * ---	1,2	H04N7/13
P,X	EP-A-0 502 571 (PHILIPS ELECTRONIQUE GRAND PUBLIC) * column 2, line 33 - column 5, line 3; figure 1 * ---	1,2	
A	DE-A-3 924 505 (ANT NACHRICHTENTECHNIK) * column 1, line 33 - column 2, line 42 * ---	1,2	
A	GRUNDIG TECHNISCHE INFORMATIONEN vol. 31, no. 1/2, 1984, pages 3 - 7 GLAAB 'WELCHE VORTEILE BIETET DAS OVERSAMPLING-VERFAHREN DER GRUNDIG COMPACT-DISC-SPIELER' * paragraph 2.2; figure 6 * ---	1,2	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 115 (E-315)18 May 1985 & JP-A-60 004 383 (MATSUSHITA) 10 January 1985 * abstract * ---	1,2	
A	US-A-4 710 747 (HOLLAND) * the whole document * ---	1,2	
A	US-A-4 566 028 (LEWIS ET AL.) * column 2, line 5 - line 30 * ---	1,2	
A	FR-A-2 529 043 (THOMSON-CSF) * page 2, line 4 - page 3, line 2 * * page 3, line 19 - page 4, line 11 * -----	1,2	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 11 MARCH 1993	Examiner BOSCH F.M.D.
CATEGORY OF CITED DOCUMENTS			
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