

(19)



Europäisches Patentamt
European Patent Office
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(11) Publication number:

0 544 427 A2

(12)

EUROPEAN PATENT APPLICATION(21) Application number: **92310381.6**(51) Int. Cl.⁵: **G09G 3/36**(22) Date of filing: **13.11.92**(30) Priority: **27.11.91 JP 312319/91**(43) Date of publication of application:
02.06.93 Bulletin 93/22(84) Designated Contracting States:
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London SW1H 0RJ (GB)(54) **Display module drive circuit having a digital source driver capable of generating multi-level drive voltages from a single external power source.**

(57) A display module drive circuit has a gate driver and a source driver. The source driver has a shift register (1), a sampling memory (2), a hold memory (3), a timing signal generating circuit (4), a voltage control circuit (5), and an output voltage generating circuit (6) having a capacitor and a switch. The timing signal generating circuit (4) generates timing signals (T_0 - T_7) having different pulse widths in each of horizontal periods. The number of the timing signals (T_0 - T_7) depends on the number of density levels of an image to be displayed. Upon receipt of digital video signals (HnD_0 , HnD_1 , HnD_2) and the timing signals (T_0 - T_7), the voltage control circuit (5) selects one of the timing signals (T_0 - T_7) based on the contents of the video signals (HnD_0 , HnD_1 , and HnD_2) in each horizontal period and outputs a control signal (CON1, CON2) at a specified level for a period corresponding to the pulse width of the selected timing signal. The capacitor of the output voltage generating circuit (6) is charged with an external power voltage while the control signal (CON1, CON2) is being received by the switch, so that a drive voltage is generated. The external power voltage is supplied from an external power source offering an electrical potential which becomes higher with time.

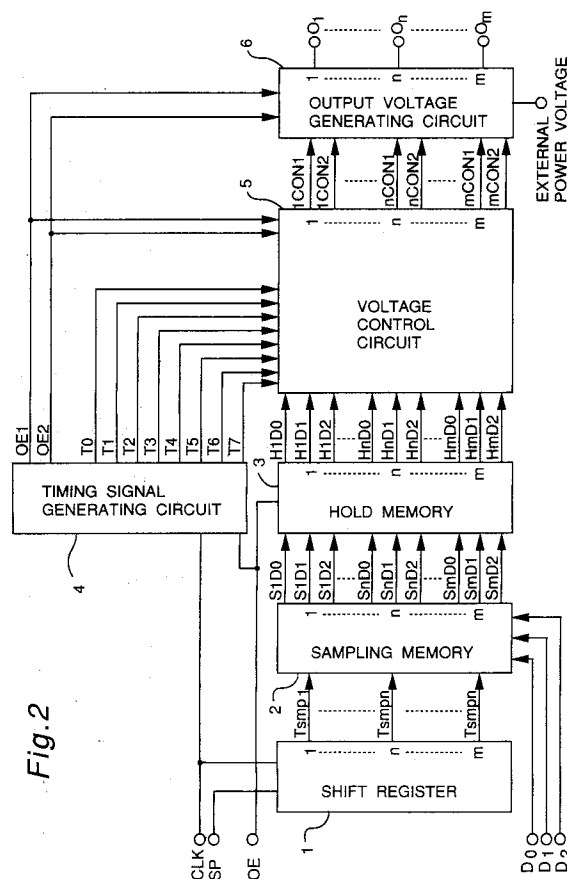


Fig. 2

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a display module drive circuit having a gate driver and a source driver, and more particularly to a digital source driver for outputting multi-level drive voltages for display of a multi-density-level image based on an input digital video signal of a specified number of bits.

2. Description of the Prior Art

Fig. 13 schematically shows a conventional matrix type liquid crystal display module. The matrix type liquid crystal display module employs a TFT (Thin Film Transistor) as a switching element for driving pixel electrodes. A TFT liquid crystal display panel 300 includes m signal electrodes 302 (Nos. O_1 through O_m) arranged in parallel with each other and i scanning electrodes 301 (Nos. 1 through i) arranged in parallel with each other and perpendicularly to the signal electrodes 302. In proximity to the intersecting point between each scanning electrode 301 and each signal electrode 302 is provided a TFT 304 for driving a corresponding pixel electrode 303. One horizontal scanning line is composed of m pixel electrodes 303 connected to one scanning electrode 301.

The TFT liquid crystal panel 300 is driven by an LCD module drive circuit 200 including a source driver 201 and a gate driver 202. The source driver 201 and the gate driver 202 are connected respectively to the signal electrodes 302 and the scanning electrodes 301. The source driver 201 samples and holds an input digital image signal or a video signal to supply the signal to the signal electrodes 302. On the other hand, the gate driver 202 successively outputs scanning pulses to the scanning electrodes 301. The gate driver 202 and the source driver 201 receive control signals such as a clock signal from a control circuit 203. An external power voltage generating circuit 204 generates a plurality of external power voltages of different levels (for example, eight) from an input power voltage and supplies them to the source driver 201.

Fig. 14 shows in detail the construction of the source driver 201 shown in Fig. 13. The source driver 201 includes a shift register 101, a sampling memory 102, a hold memory 103, a decoder 104, and an output voltage selecting circuit 105. The source driver 201 has m signal systems corresponding to the m signal electrodes.

Fig. 15 shows the construction of an n th ($1 \leq n \leq m$) signal system of the source driver 201. As shown in Fig. 15, part belonging to the n th signal system of the output voltage selecting circuit 105 is

composed of eight analog switches ASW_0 through ASW_7 . In operation, the shift register 101 shown in Figs. 13 and 14 outputs a SAMPLING pulse $Tsmpn$ for the n th pixel. At the leading edge of the SAMPLING pulse $Tsmpn$, externally input video signals D_0 , D_1 , and D_2 are taken into the sampling memory 102 and held in three D-flip-flops 121, 122, and 123 belonging to the n th signal system of the sampling memory 102. When the sampling operation for one horizontal period is completed, an OUTPUT pulse OE is input to the hold memory 103. In response to this pulse OE , the video signals D_0 , D_1 , and D_2 held in the sampling memory 102 are transferred to the hold memory 103 (three D-flip-flops 131, 132, and 133) and then to the decoder 104. The decoder 104 decodes the input video signals D_0 , D_1 , and D_2 and outputs eight enabling signals Y_0 through Y_7 (only one of these signals is at a high (H) level and the others are at a low (L) level). According to the contents of the enabling signals Y_0 through Y_7 , one of analog switches ASW_0 through ASW_7 in the output voltage selecting circuit 105 becomes conductive. Therefore, from among the eight external power voltages V_0 through V_7 transmitted from the external power voltage generating circuit 204 to the output voltage selecting circuit 105, one voltage which has been applied to the analog switch made conductive is output to the signal electrode (source line) On ($1 \leq n \leq m$). In this way, the external power voltages V_0 through V_7 having multiple levels or gradations can be supplied as drive voltages to the TFT liquid crystal panel 300 in accordance with the contents of the video signal D_0 , D_1 , and D_2 .

However, when increasing the number of bits of the video signal to improve the multi-density-level image reproducibility, the above-mentioned conventional drive circuit is accompanied by a problem of requiring an increased number of external power voltages which serve as density-scale reference voltages. For example, as the number of bits of the video signal increases to 3, 4, 6, 8, ..., the number of external power voltages increases to $2^3 (= 8)$, $2^4 (= 16)$, $2^6 (= 64)$, $2^8 (= 256)$, ... Therefore, the following problems take place.

- (1) The external power source increases in scale, resulting in cost increase.
- (2) An LSI (Large-Scale Integrated circuit) having the above-mentioned source driver built therein is required to have an increased number of input terminals so that it becomes difficult to package the LSI.
- (3) The external power voltages are required to have a higher accuracy, resulting in difficulty in controlling voltage adjustment operations.

SUMMARY OF THE INVENTION

The object of the present invention is therefore to provide a display module drive circuit having a source driver which solves the above problems and which is capable of supplying multi-level drive voltages corresponding to multiple density levels of an image to be displayed, without increasing the number of the external power sources.

In order to achieve the above object, the present invention provides a display module drive circuit including a gate driver to be connected with scanning electrodes of a display module for supplying scanning pulses to the scanning electrodes and a source driver to be connected with signal electrodes of the display module for outputting drive voltages of multiple levels for display of an image having multiple density levels to the signal electrodes based on an input digital video signal represented by a specific number of bits, the source driver comprising:

a timing signal generating circuit for generating a specified number of timing signals having different pulse widths based on clock pulses in each of horizontal periods, the number of the timing signals corresponding to the number of the density levels of the image;

a voltage control circuit for, upon receipt of the digital video signal and the timing signals, selecting one of the timing signals based on the contents of the digital video signal in each horizontal period to output a control signal at a specified level for a time corresponding to the pulse width of the selected timing signal; and

an output voltage generating circuit for generating a drive voltage, including a capacitor and first switch means, said capacitor receiving an external power voltage through the first switch means during the time during which the control signal of the specified level is output from the voltage control circuit in each horizontal period.

The source driver in the display module drive circuit in accordance with an embodiment of the present invention operates as follows. First, the timing signal generating circuit generates the timing signals having different pulse widths in each horizontal period. The number of the timing signals (for example, 8) depends on the density levels of the image to be displayed. One of the timing signals is always held at a H level. Then the voltage control circuit receives video signals and the timing signals and selects one of the timing signals based on the contents of the video signals in each horizontal period. Fig. 9 shows an example of selection of the timing signal for generation of the control signal. As shown in Fig. 9, when the video signals indicated by D_0 , D_1 , and D_2 represent the levels L, L, and L respectively, the timing

signal T_0 is selected. When the video signals D_0 , D_1 , and D_2 represent the levels H, L, and L respectively, the timing signal T_1 is selected. When the video signals D_0 , D_1 , and D_2 represent the levels H, H, and H respectively, the timing signal T_7 is selected. Then the voltage control circuit outputs a control signal at a high level for a period corresponding to the pulse width of the selected timing signal. In the output voltage generating circuit, the capacitor receives the external power voltage from an external power source through the first switch means during the time when the control signal is output in each horizontal period so that a drive voltage is generated in each horizontal period. In this case, if the external power voltage is given from an external power source offering an electrical potential which becomes higher with time, as illustrated in Fig. 10 that shows a relationship between the timing signals and the drive voltages used in an embodiment of the invention, the level of the drive voltage is controllable in accordance with the pulse width of the selected timing signal so that drive voltages of multiple levels can be generated.

According to the above-mentioned display module drive circuit, drive voltages of multiple levels can be generated from a single external power source. As the number of bits of the video signal is increased to promote the multi-density-level display for the improvement of the image quality, the timing signal generating circuit generates an increased number of timing signals according to the amount of gradations. The number of the drive voltages increases accordingly. The above arrangement obviates any increase in number of the external power sources. In more detail, the multi-level drive voltages can be generated without increasing the external power source. Accordingly, the following advantages are produced.

(1) The external power source can be reduced in scale with cost reduction.

(2) An LSI (Large-Scale Integrated circuit) having the above-mentioned source driver built therein is permitted to have a reduced number of input terminals. This facilitates packaging of the LSI.

(3) The external power voltage is permitted to have an eased accuracy, which facilitates controlling of the external power voltage.

When the above-mentioned output voltage generating circuit has two capacitors and the two capacitors are alternately charged with the external power voltage in alternate horizontal periods, the drive voltages are output alternately from the two capacitors. In other words, when one of the capacitors is being charged, the other capacitor outputs the drive voltage. Therefore, continuous output of the drive voltage is achieved. In an embodiment, the two capacitors are switched by output-switching

signals which are generated by the timing signal generating circuit. The output-switching signals are at opposite levels from each other in their essential parts and respectively inverted every horizontal period.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Fig. 1 is a block diagram of a matrix type liquid crystal display module (TFT LCD module) which has a drive circuit including a gate driver and a source driver in accordance with an embodiment of the present invention;

Fig. 2 is a block diagram of the entire system of the source driver of Fig. 1;

Fig. 3 is a diagram showing the construction of a part processing a single signal group in the source driver;

Fig. 4 is a diagram showing a timing signal generating circuit being a constituent part of the source driver;

Fig. 5 is a timing chart of output waveforms of the timing signal generating circuit being a constituent part of the source driver;

Fig. 6 is a timing chart of other output waveforms of the timing signal generating circuit;

Fig. 7 is a chart for explaining a procedure for generating control signals in a voltage control circuit being a constituent part of the source driver;

Fig. 8 is a timing chart of alternative exemplified output waveforms of the timing signal generating circuit;

Fig. 9 is a chart for explaining a procedure for generating a control signal based on the contents of the input digital video signals in accordance with the present invention;

Fig. 10 is a graph showing the relationship between the timing signals and the drive voltages;

Fig. 11 is a characteristic curve showing the relationship between the applied voltages and the transmissivities of a normally-white liquid crystal;

Fig. 12 is a voltage-time characteristic curve for correcting an external power voltage;

Fig. 13 is a block diagram of a conventional matrix type liquid crystal display module (TFT LCD module);

Fig. 14 is a block diagram of the entire system of a conventional source driver employed in the conventional liquid crystal display module of Fig. 13; and

Fig. 15 is a diagram showing a part processing a single signal group in the source driver shown in Fig. 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 is a block diagram of a matrix type liquid crystal display module which uses a drive circuit 200 including a gate driver 202 which is the same as that of Fig. 13 and a source driver 7 in accordance with an embodiment of the present invention. In Fig. 1, the same components as those in Fig. 13 showing the conventional matrix type liquid crystal display module are denoted by the same numerals, and no detailed description on those components is provided here. It is of course that the liquid crystal display module of Fig. 1 has no circuit for generating a plurality of external power voltages of multiple levels such as the external power voltage generating circuit 204 shown in Fig. 13.

Fig. 2 shows the construction of the entire source driver 7 shown in Fig. 1. Fig. 3 shows a part processing the n th ($1 \leq n \leq m$) one of the m signal groups (each one represented by three bits) of the source driver 7. The m signal groups correspond to the m pixels. The source driver 7 includes a shift register 1, a sampling memory 2, a hold memory 3, a timing signal generating circuit 4, a voltage control circuit 5, and an output voltage generating circuit 6. The shift register 1, sampling memory 2, and hold memory 3 are the same as the shift register 101, sampling memory 102, and hold memory 103 shown in Fig. 13-15 respectively.

The timing signal generating circuit 4 is composed of two parts 4A and 4B as shown in Fig. 4. The part 4A is composed of D-flip-flop circuits 41, 42, and 43, an AND circuit 44, a NOR circuit 45, and a NAND circuit 47. As shown in Fig. 5, when receiving clock pulses CLK and a pulse signal OE input once a horizontal period, the part 4A of the timing signal generating circuit 4 generates output-switching signals OE1 and OE2, which are at opposite levels from each other in their essential parts and inverted respectively every horizontal period, as well as a clear signal CLR1 obtained by inverting most part of the pulse signal OE. It is noted that signals OEA and OEB in Fig. 5 are outputs of the D-flip-flop circuits 42 and 43 respectively.

On the other hand, the part 4B of the timing signal generating circuit 4 is composed of a 6-bit counter 46, an inverter 48, and D-flip-flop circuits 49 through 55, as shown in Fig. 4. When receiving the clock pulses CLK, the part 4B first generates a signal 64 CK representing 64 clock pulses as shown in Fig. 6. Then, eight kinds (corresponding

to the number of density levels of an image) of timing signals $T_0, T_1, \dots, T_7$ having different pulse widths are generated in one horizontal period based on the signal 64 CK. (Note that the timing signal T_0 is maintained at H level.)

The voltage control circuit 5, more specifically part thereof processing the n th signal group shown in Fig. 3, receives video signals HnD_0, HnD_1 , and HnD_2 from the hold memory 3, the timing signals $T_0, T_1, \dots, T_7$, and the output-switching signals OE1 and OE2 from the timing signal generating circuit 4. Then the voltage control circuit 5 outputs control signals CON1 and CON2 at specific levels every horizontal period, as shown in Fig. 7, according to the contents of the received signals and output-switching signals. In more detail, when the output-switching signals OE1 and OE2 represent respectively logic "1" and logic "0", the control signal CON1 is held at H level for a period corresponding to the pulse width of the timing signal $T_0, T_1, \dots$, or T_7 selected according to the contents of the video signals HnD_0, HnD_1 , and HnD_2 . Meanwhile, the control signal CON2 is maintained at L level, irrespective of the contents of the video signals HnD_0, HnD_1 , and HnD_2 . When the output-switching signals OE1 and OE2 represent respectively logic "0" (corresponding to L level) and logic "1" (corresponding to H level), the control signal CON1 assumes L level irrespective of the contents of the video signals HnD_0, HnD_1 , and HnD_2 . Meanwhile, the control signal CON2 is held at H level for a period corresponding to the pulse width of the timing signal $T_0, T_1, \dots$, or T_7 selected according to the contents of the video signals HnD_0, HnD_1 , and HnD_2 . When both the output-switching signals OE1 and OE2 represent logic "0", the control signals CON1 and CON2 are switched to "L" level whatever the contents of the video signals HnD_0, HnD_1 , and HnD_2 are. It is noted that there is no case where both the signals OE1 and OE2 represent logic "1" as apparent from Fig. 5.

As shown in Fig. 3, the output voltage generating circuit 6 (more specifically part thereof processing the n th signal group) is composed of wirings L1 and L2 connecting an external power source (voltage V) to a source line (signal electrode) On, capacitors C1 and C2 connected between each of the wirings L1 and L2 and the ground, and analog switches ASW1, ASW2, ASW3, and ASW4. The analog switches ASW1 and ASW3 are arranged on the wiring L1 and on opposite sides of the capacitor C1 toward the external power source and the source line On, respectively. These analog switches ASW1 and ASW3 are turned on and off respectively by the control signal CON1 from the voltage control circuit 5 and the output-switching signal OE2 from the timing signal generating circuit 4 (the switches are turned on when each control signal is

at H level and turned off when each control signal is at L level). On the other hand, the analog switches ASW2 and ASW4 are arranged on the wiring L2 and toward the external power source and the source line (signal electrode) On from the capacitor C2, respectively. These switches ASW2 and ASW4 are turned on and off respectively by the control signal CON2 from the voltage control circuit 5 and the output-switching signal OE1 from the timing signal generating circuit 4 (the switches are turned on when each control signal is at H level and turned off when each control signal is at L level).

The above-mentioned source driver 7 operates as follows. First, when the shift register 1 outputs a sampling pulse T_{smpn} for the n th pixel, the externally input video signals D_0, D_1 , and D_2 are taken into the sampling memory 2 at the leading edge of the sampling pulse T_{smpn} . Then those sampled video signals are held as video signals SnD_0, SnD_1 , and SnD_2 in the three D-flip-flops 21, 22, and 23 of the sampling memory 2 (part processing the n th signal group). When the sampling operation in one horizontal period is completed, the pulse signal OE is input to the hold memory 3. In response to the pulse signal OE, the video signals SnD_0, SnD_1 , and SnD_2 held in the sampling memory 2 are received by the hold memory 3 (three D-flip-flops 31, 32, and 33) to be then transferred as video signals HnD_0, HnD_1 , and HnD_2 to the voltage control circuit 5. The voltage control circuit 5 outputs the control signal CON1 or CON2 of H level for the period corresponding to the pulse width of the timing signal $T_0, T_1, \dots$, or T_7 selected in each horizontal period based on the contents of the video signals HnD_0, HnD_1 , and HnD_2 , as described hereinbefore. It is now assumed that the output-switching signal OE1 is at H level and the output-switching signal OE2 is at L level in a specified horizontal period. In this case, the control signal CON1 is turned to H level and the control signal CON2 is turned to L level. Consequently, in the output voltage generating circuit 6, the analog switches ASW1 and ASW4 are turned on while the analog switches ASW2 and ASW3 are turned off. Therefore, the capacitor C1 is charged with the external power voltage V through the analog switch ASW1 for the period corresponding to the pulse width of the timing signal $T_0, T_1, \dots$, or T_7 selected by the voltage control circuit 5. At this time, by supplying the external power voltage V from an external power source having a potential which gets higher with time as shown in Fig. 10, a drive voltage corresponding to the contents of the video signals D_0, D_1 , and D_2 is formed across the electrodes of the capacitor C1. On the other hand, a voltage having been charged to the capacitor C2 in the preceding horizontal period is output therefrom by way of the analog switch ASW4 to the source

line (signal electrode) On.

As obvious from the above, the output-switching signals OE1, OE2 serve to determine which of the capacitors C1, C2 should be charged with the external power voltage and which of the voltages charged in the capacitors C1, C2 should be supplied to the source line On.

In the next horizontal period, the output-switching signal OE1 is switched to L level and the output-switching signal OE2 is switched to H level. In this case, the control signal CON1 is switched to L level and the control signal CON2 is switched to H level. With these voltage status changes, the analog switches ASW1 and ASW4 are turned off while the analog switches ASW2 and ASW3 are turned on in the output voltage generating circuit 6. Therefore, the capacitor C2 is charged with the external power voltage V by way of the analog switch ASW2 for the period corresponding to the pulse width of the timing signal T_0 , T_1 , ..., or T_7 selected by the voltage control circuit 5. At this time, because the external power voltage V is supplied from the external power source having a potential which gets higher with time as shown in Fig. 10, a drive voltage of a level corresponding to the contents of the video signals D_0 , D_1 , and D_2 is formed across the electrodes of the capacitors C2. On the other hand, the voltage (drive voltage) having been charged in the previous horizontal period is output from the capacitor C1 by way of the analog switch ASW3 to the source line On. As apparent from the above, while one capacitor is being charged, the other capacitor can output a drive voltage, so that drive voltages of multiple levels are continuously output from the output voltage generating circuit 6. Although there is produced a moment that the output-switching signals OE1 and OE2 are both at L level and the control signals CON1 and CON2 are both at L level (the analog switches ASW1 through ASW4 are all in off status) in a transition from one horizontal period to another, almost no influence is exerted on the above-mentioned operation in each horizontal period.

As described above, the source driver 7 can generate multi-level drive voltages from only a single external power source. When increasing the number of bits of the video signal to increase the number of density levels of an image, the timing signal generating circuit 4 generates an increased number of timing signals according to the number of the density levels to enable generation of multi-level drive voltages based on the timing signals. In this way, multi-level drive signals can be offered without increasing the number of the external power sources.

When a normally-white liquid crystal display panel is used as a display panel 300, the light

transmissivity varies in the medium voltage region and is saturated in the low and high voltage regions as shown in Fig. 11. Since digital one bit display system has only the on and off status, a high contrast can be obtained so long as the display panel is driven at voltages in the low and high voltage regions. However, in a multi-density-level display system, since the light transmissivity varies nonlinearly in the low and high voltage regions of the applied voltage V, intended brightness cannot be obtained without any modification to the applied voltage V, resulting in failing to display correct colors. Therefore, the characteristic curve (voltage-time characteristic) of the external power voltage shown in Fig. 10 is corrected as shown in Fig. 12 to provide the voltage levels or gradations with a linear characteristic.

It is to be noted that, although the transmissivity varies in the medium voltage region at the present time as shown in Fig. 11, the transmissivity needs to change in the low voltage region in the future because a liquid crystal display device using a low drive voltage such as 3V, for example, can be used then.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A display module drive circuit (200) including a gate driver (202) to be connected with scanning electrodes (301, 1-i) of a display module (300) for supplying scanning pulses to the scanning electrodes and a source driver (7) to be connected with signal electrodes (302, O_1 - O_m) of the display module (300) for outputting drive voltages of multiple levels for display of an image having multiple density levels to the signal electrodes based on an input digital video signal (D_0 , D_1 , D_2) represented by a specific number of bits, the source driver comprising:

a timing signal generating circuit (4) for generating a specified number of timing signals (T_0 - T_7) having different pulse widths based on clock pulses (CLK) in each of horizontal periods, the number of the timing signals (T_0 - T_7) corresponding to the number of the density levels of the image;

a voltage control circuit (5) for, upon receipt of the digital video signal (D_0 , D_1 , D_2 - ($H_n D_0$, $H_n D_1$, $H_n D_2$)) and the timing signals (T_0 - T_7), selecting one of the timing signals (T_0 - T_7)

based on the contents of the digital video signal (D_0 , D_1 , D_2) in each horizontal period to output a control signal (CON1, CON2) at a specified level for a time corresponding to the pulse width of the selected timing signal (T_0 - T_7); and

an output voltage generating circuit (6) for generating a drive voltage, including a capacitor (C1, C2) and first switch means (ASW1, ASW2), said capacitor (C1, C2) receiving an external power voltage (V) through the first switch means (ASW1, ASW2) during the time during which the control signal (CON1, CON2) of the specified level is output from the voltage control circuit (5) in each horizontal period.

2. The display module drive circuit as claimed in claim 1, wherein the timing signal generating circuit (4) further generates output-switching signals (OE1, OE2) which are at opposite levels from each other in their essential parts and which are respectively inverted every horizontal period, and wherein the voltage control circuit (5) receives the digital video signal (D_0 , D_1 , D_2 ($H_n D_0$, $H_n D_1$, $H_n D_2$)), the timing signals (T_0 - T_7) and the output-switching signals (OE1, OE2) and selects one of the timing signals (T_0 - T_7) based on the contents of the video signal (D_0 , D_1 , D_2 ($H_n D_0$, $H_n D_1$, $H_n D_2$)) and the output-switching signals in each horizontal period to output the control signal (CON1, CON2) at the specified level for the time corresponding to the pulse width of the selected timing signal (T_0 - T_7).
3. The display module drive circuit as claimed in claim 2, wherein the timing signal generating circuit has a first part (4A) which includes D-flip-flop circuits (41, 42, 43), an AND circuit (44), a NOR circuit (45) and a NAND circuit (47), and a second part (4B) which includes a counter (46), an inverter (48), and D-flip-flop circuits (49-55), and wherein the first part generates the output-switching signals (OE1, OE2) and the second part generates the timing signals (T_0 - T_7).
4. The display module drive circuit as claimed in claim 1, wherein the output voltage generating circuit (6) has two capacitors (C1, C2) and these two capacitors (C1, C2) are alternately charged with the external power voltage so that the drive voltages are generated and output from the capacitors (C1, C2) alternately.
5. The display module drive circuit as claimed in claim 4, wherein the output voltage generating circuit (6) has second switch means (ASW 3,

ASW4) for outputting the drive voltages from the capacitors (C1, C2) alternately.

6. The display module drive circuit as claimed in claim 4, wherein the external power voltage is supplied from an external power source offering an electrical potential which becomes higher with time.
7. The display module drive circuit as claimed in claim 2, wherein the output voltage generating circuit (6) has two capacitors (C1, C2) and these two capacitors (C1, C2) are alternately charged with the external power voltage so that the drive voltages are generated and output from the capacitors (C1, C2) alternately.
8. The display module drive circuit as claimed in claim 7, wherein the output voltage generating circuit (6) has second switch means (ASW 3, ASW4) for outputting the drive voltages from the capacitors alternately, based on the states of the output-switching signals (OE1, OE2) received from the timing signal generating circuit (4).
9. The display module drive circuit as claimed in claim 7, wherein the external power voltage is supplied from an external power source offering an electrical potential which becomes higher with time.
10. A display module drive circuit adapted to generate from an external power source a plurality of output voltage signals for controlling the display intensity of pixel elements of a matrix type display panel, each output voltage signal having a level corresponding to a selected one of a number of predetermined display intensities according to an input signal representing the image to be displayed, the circuit comprising:
 - means (4) for generating a number of timing signals of different width, the number of timing signals being equal to said number of display intensities;
 - means (5) for selecting one of the timing signals according to the level of said input signal and for generating therefrom a control signal; and
 - means (ASW1;ASW3) for coupling said external power source to a capacitor (C1;C2) for a predetermined period in response to said control signal, said capacitor thereafter providing a said output voltage signal.
11. A display module drive circuit according to claim 10, wherein said external power source

provides a time-varying voltage output.

- 12.** A display module drive circuit according to claim 11, wherein the voltage waveform of the power source output is arranged to correct non-linearity in the applied voltage-transmissivity characteristic of a liquid crystal material used in said display panel.

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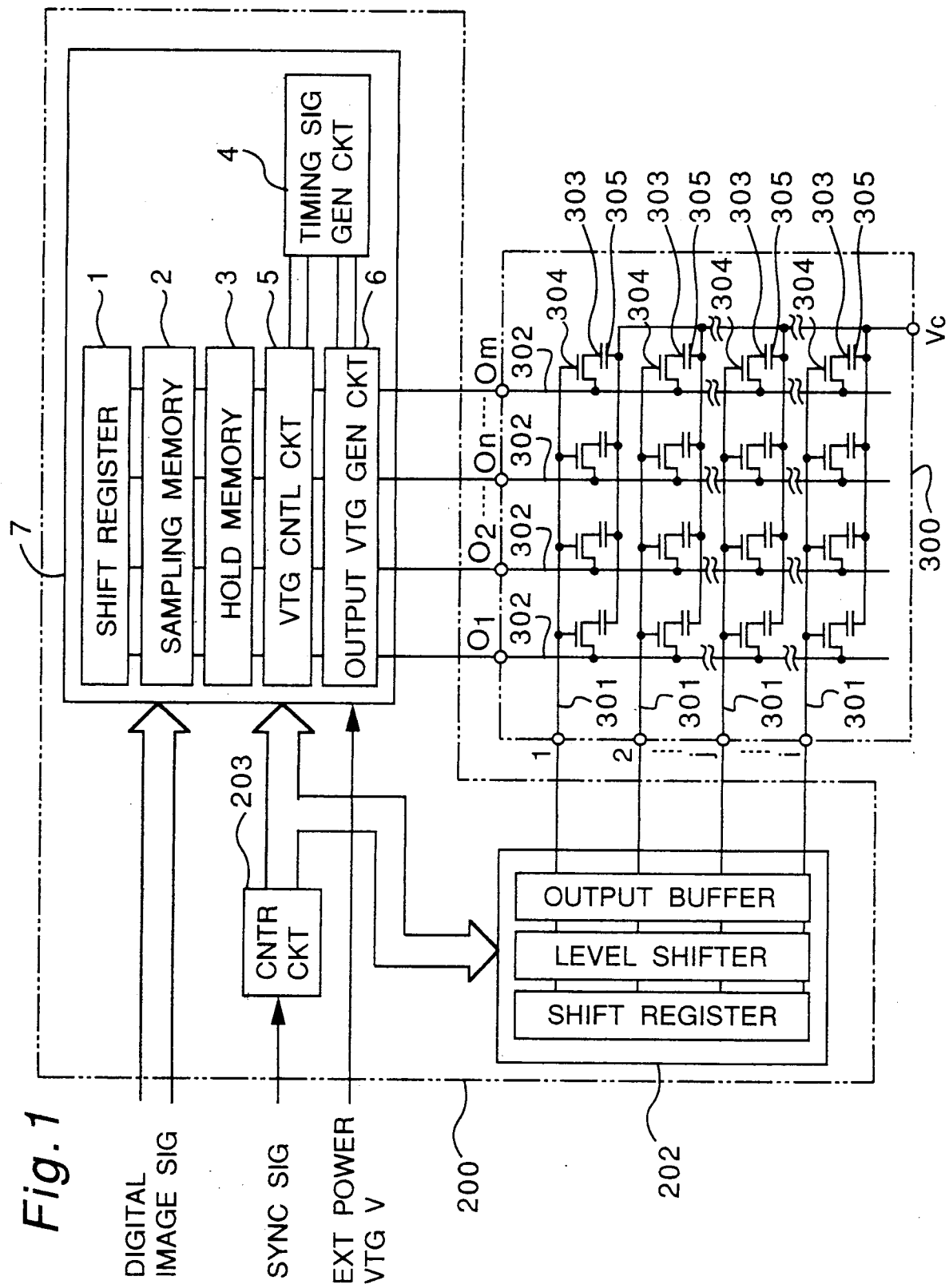
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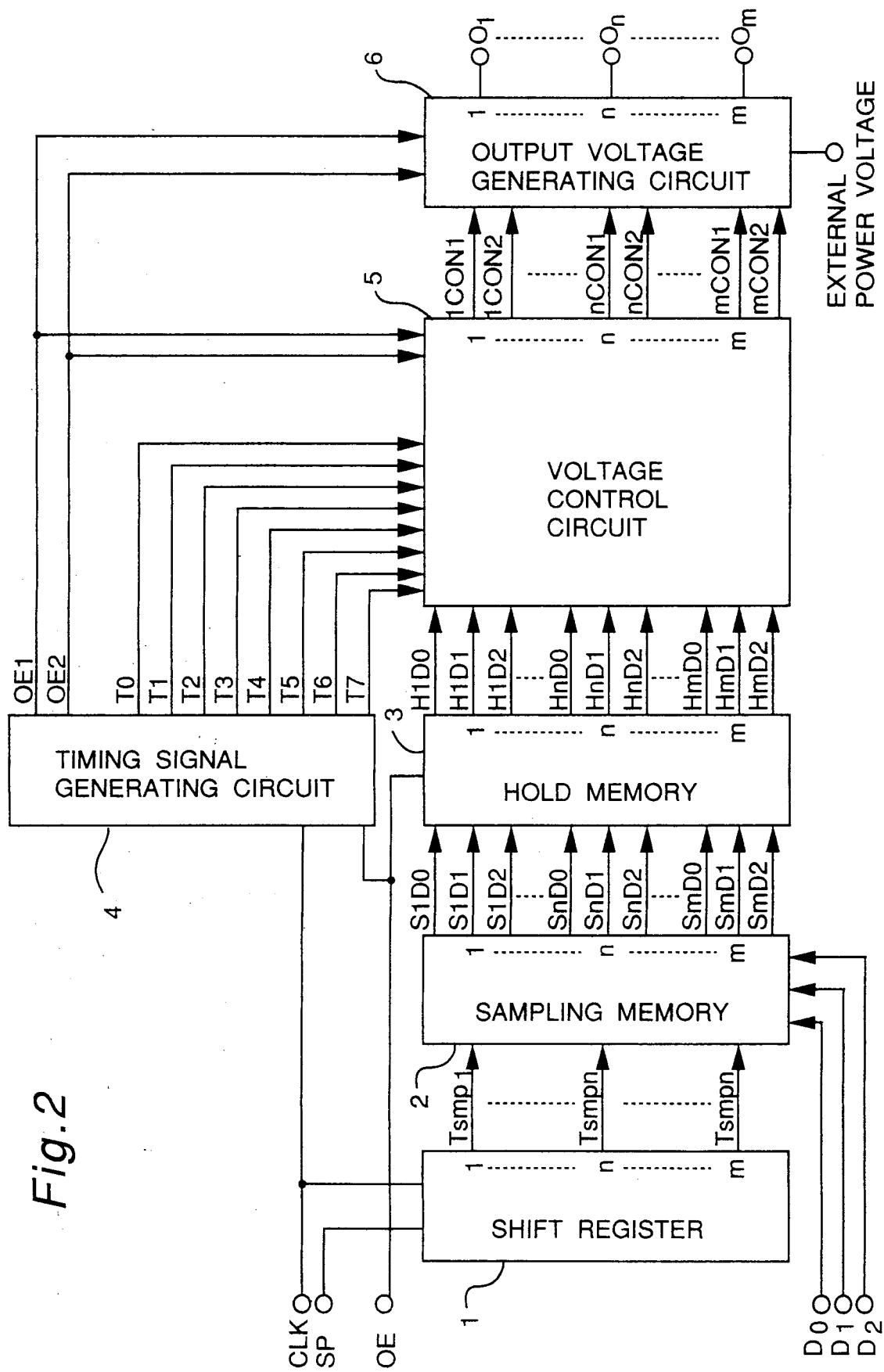
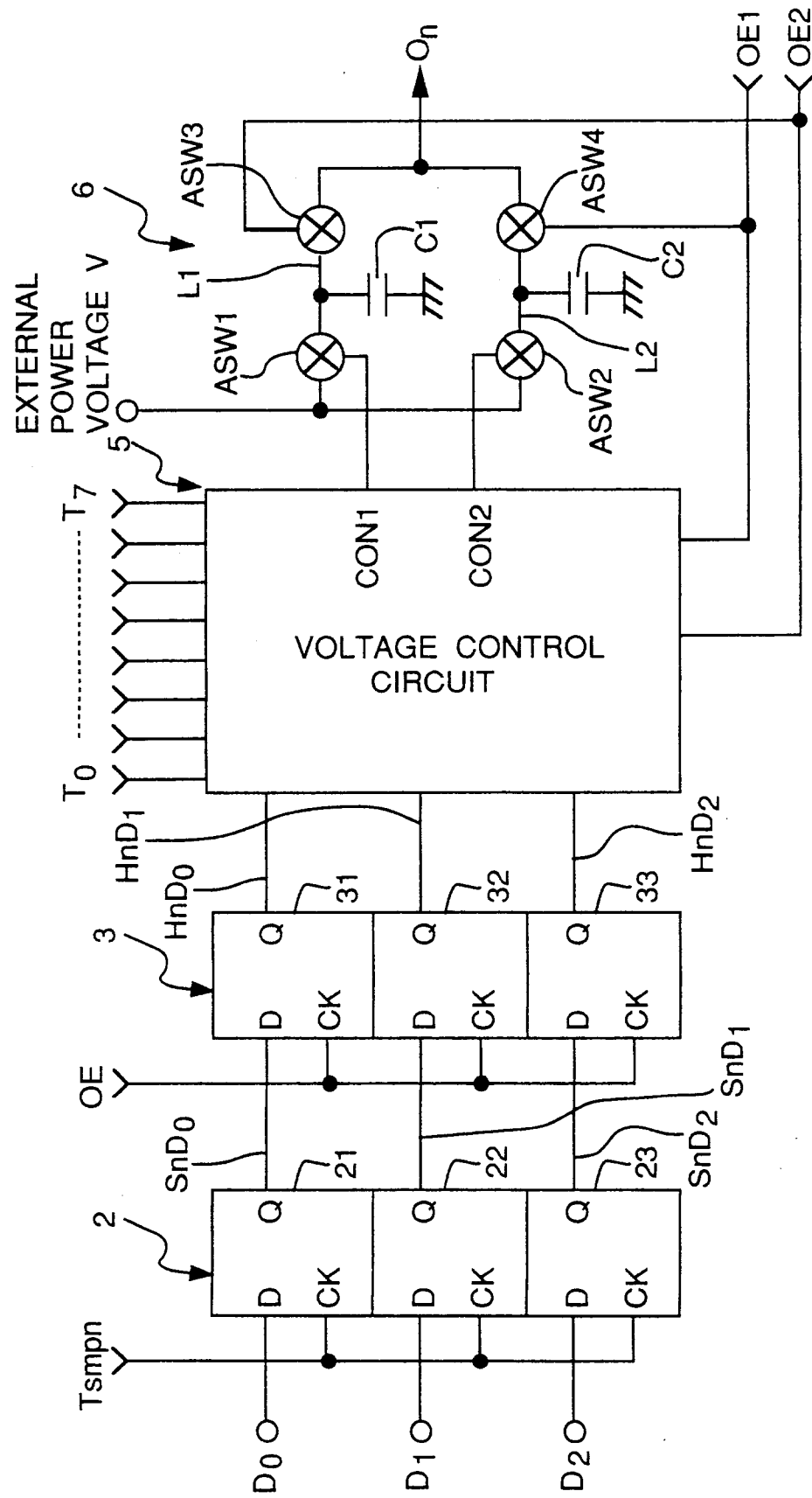


Fig. 3



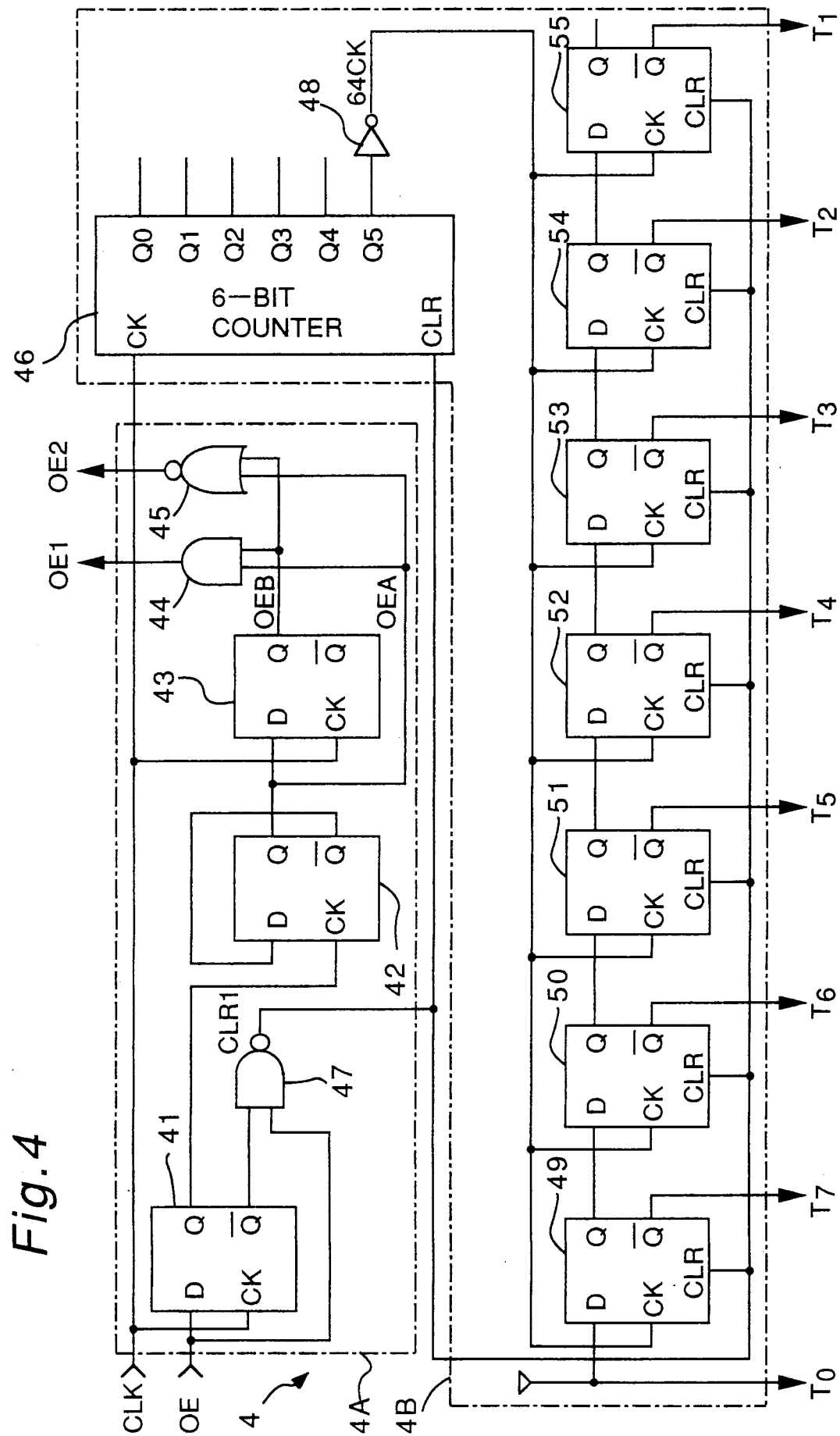


Fig. 5

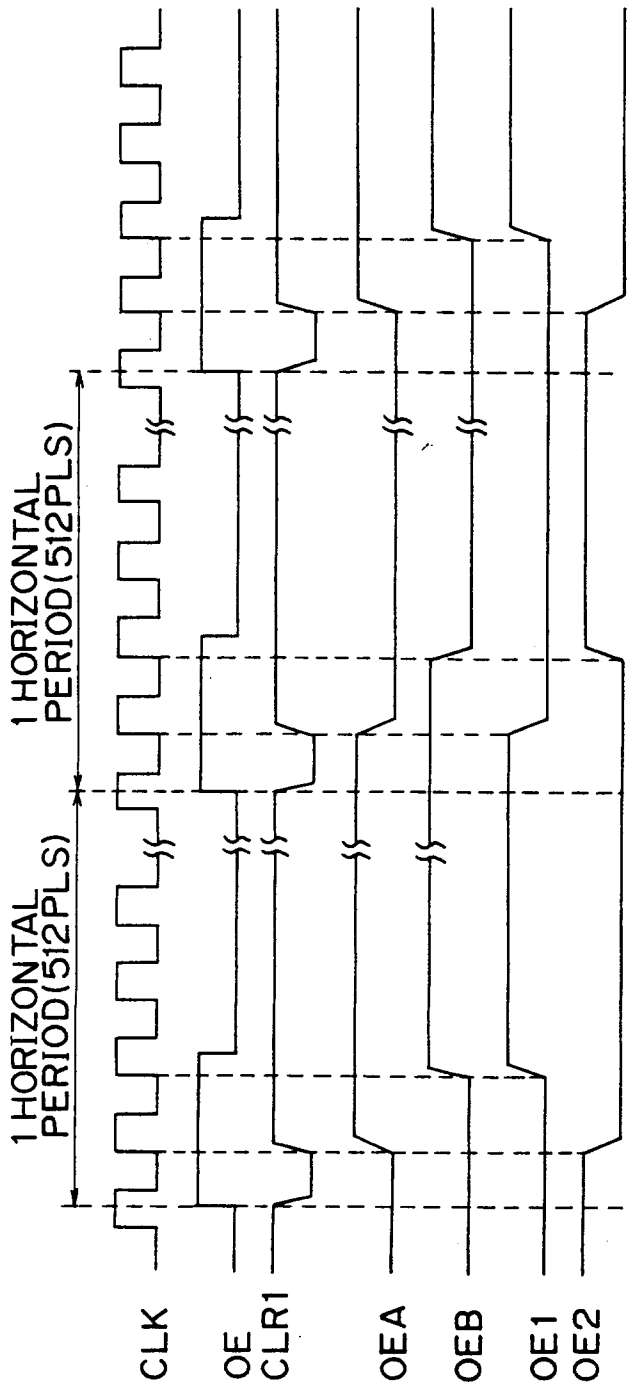


Fig. 6

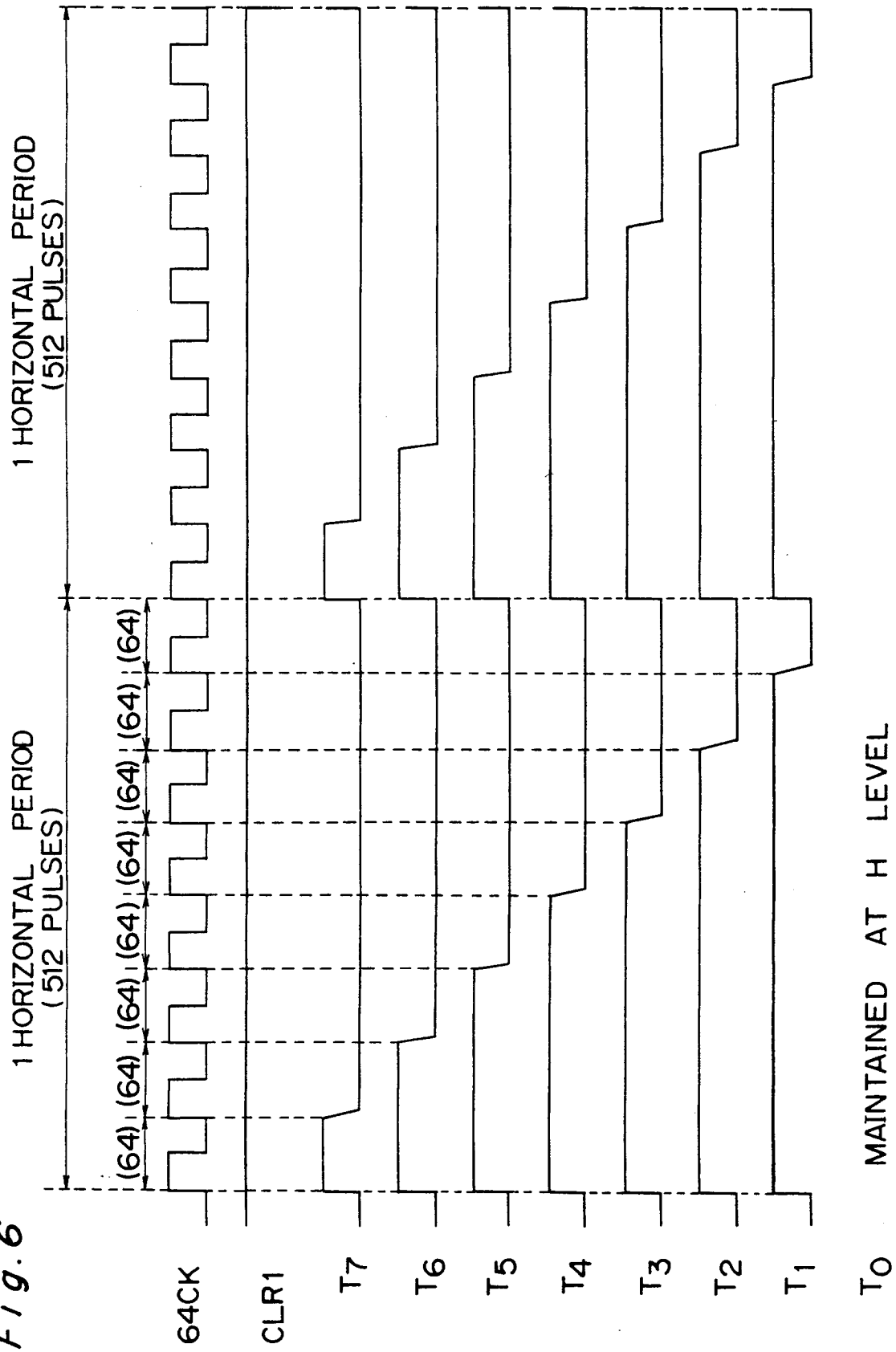


Fig. 7

	OE1=0 OE2=0		OE1=1 OE2=0		OE1=0 OE2=1		OE1=1 OE2=1	
HnD ₂ HnD ₁ HnD ₀	CON1	CON2	CON1	CON2	CON1	CON2	CON1	CON2
0 0 0	L	L	T ₀	L	L	T ₀	—	—
0 0 1	L	L	T ₁	L	L	T ₁	—	—
0 1 0	L	L	T ₂	L	L	T ₂	—	—
0 1 1	L	L	T ₃	L	L	T ₃	—	—
1 0 0	L	L	T ₄	L	L	T ₄	—	—
1 0 1	L	L	T ₅	L	L	T ₅	—	—
1 1 0	L	L	T ₆	L	L	T ₆	—	—
1 1 1	L	L	T ₇	L	L	T ₇	—	—

Fig. 8

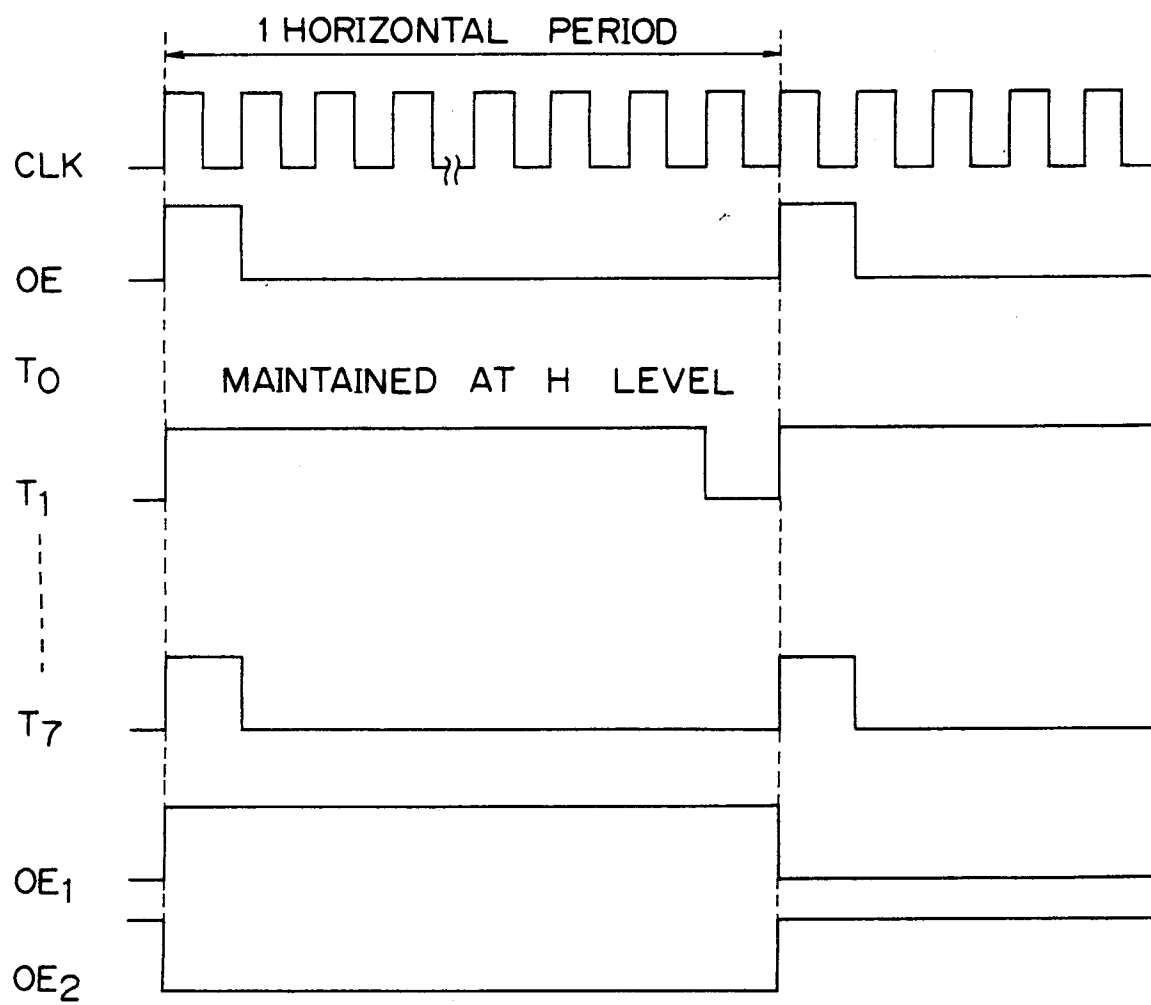


Fig. 9

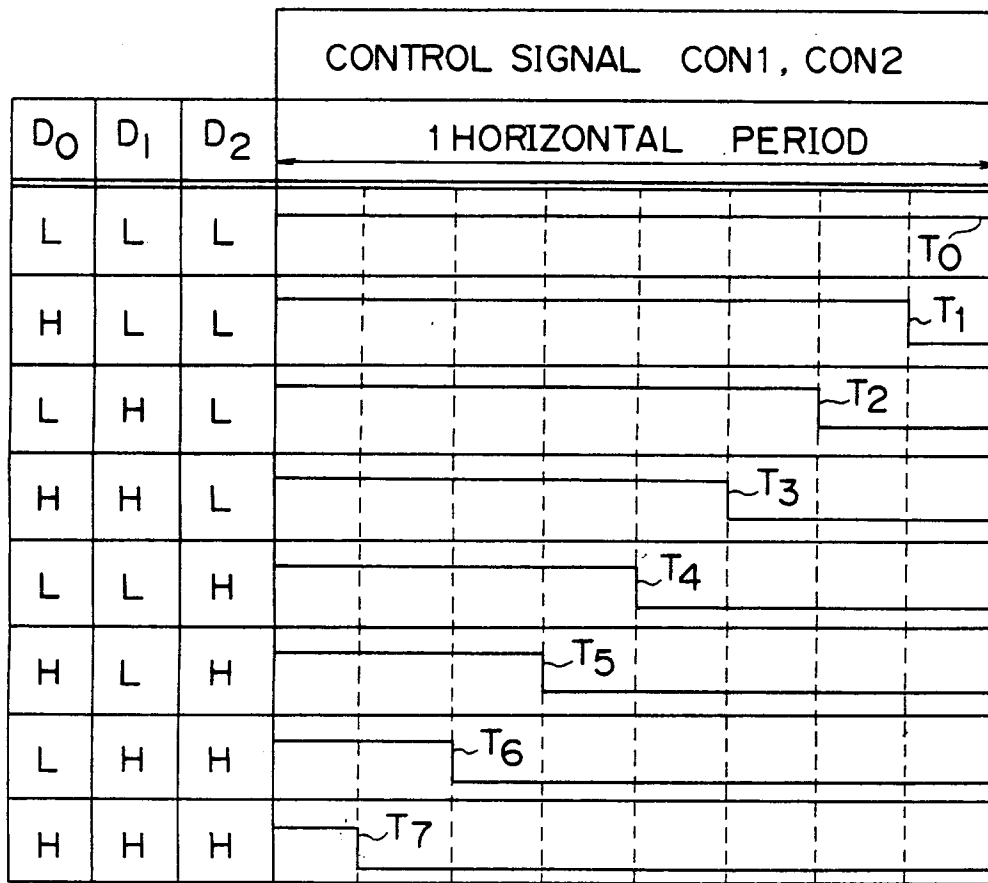


Fig. 10

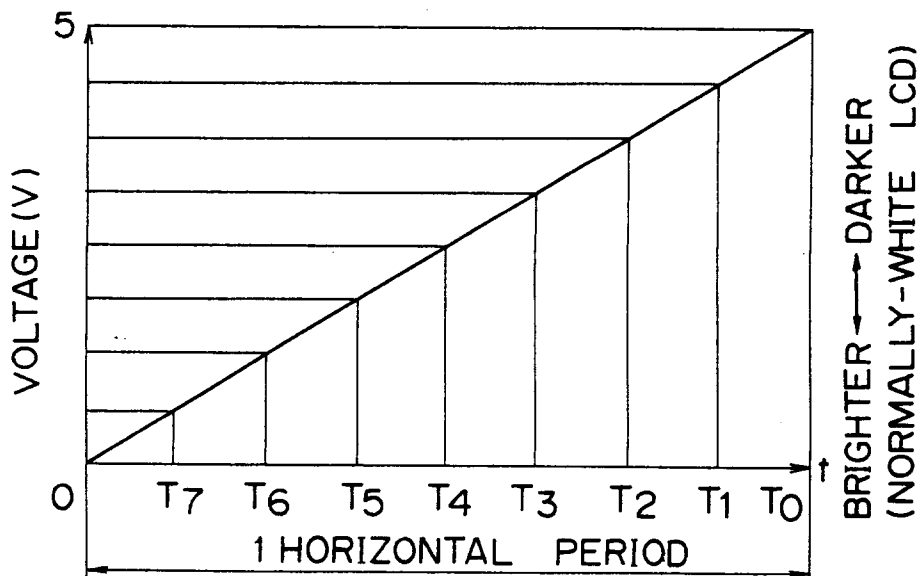


Fig. 11

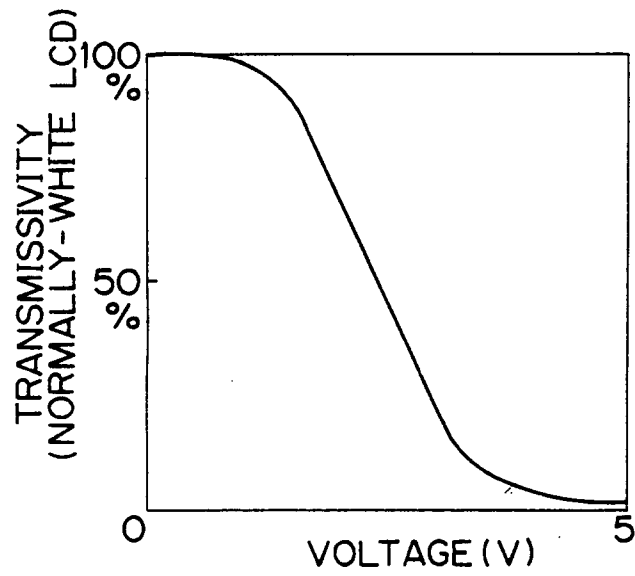
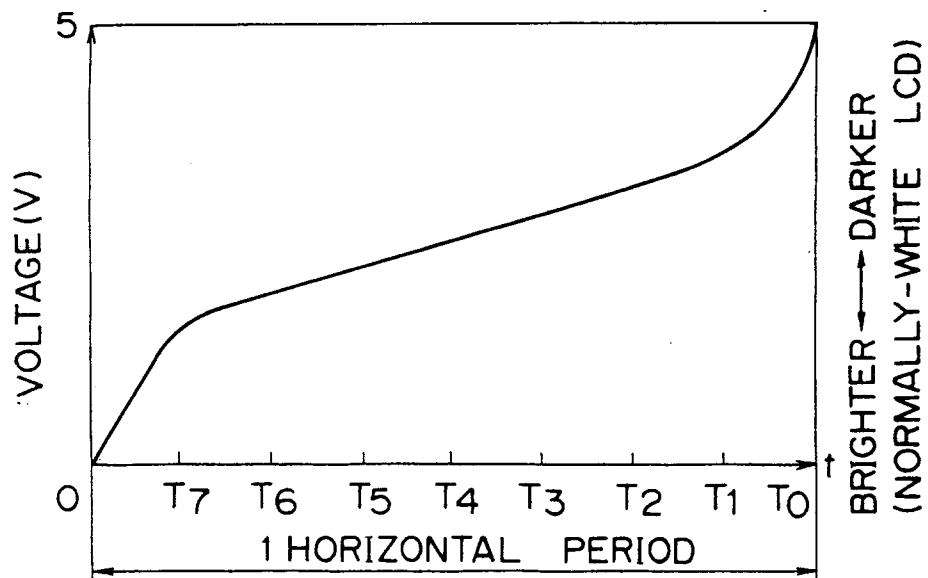


Fig. 12



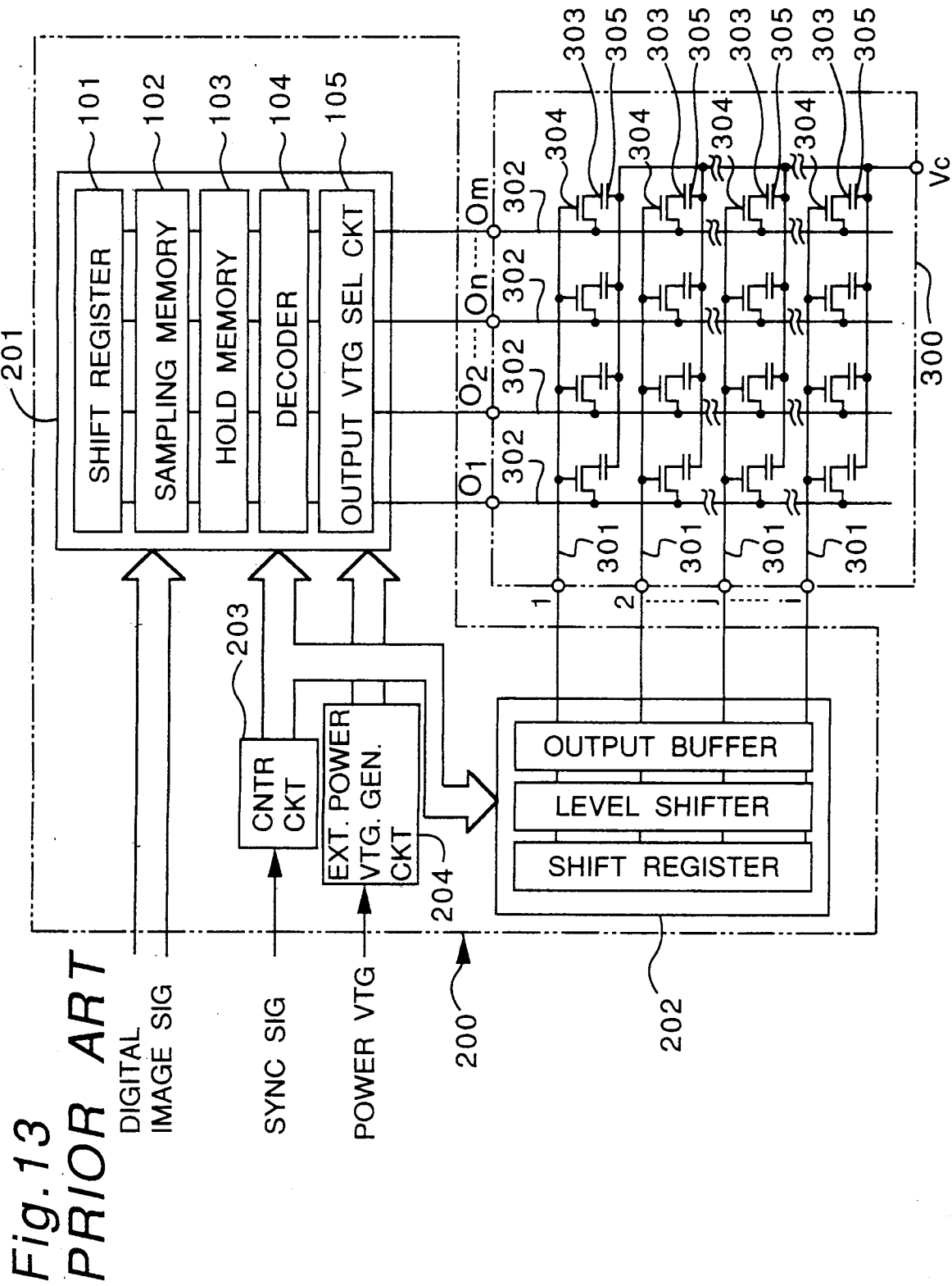


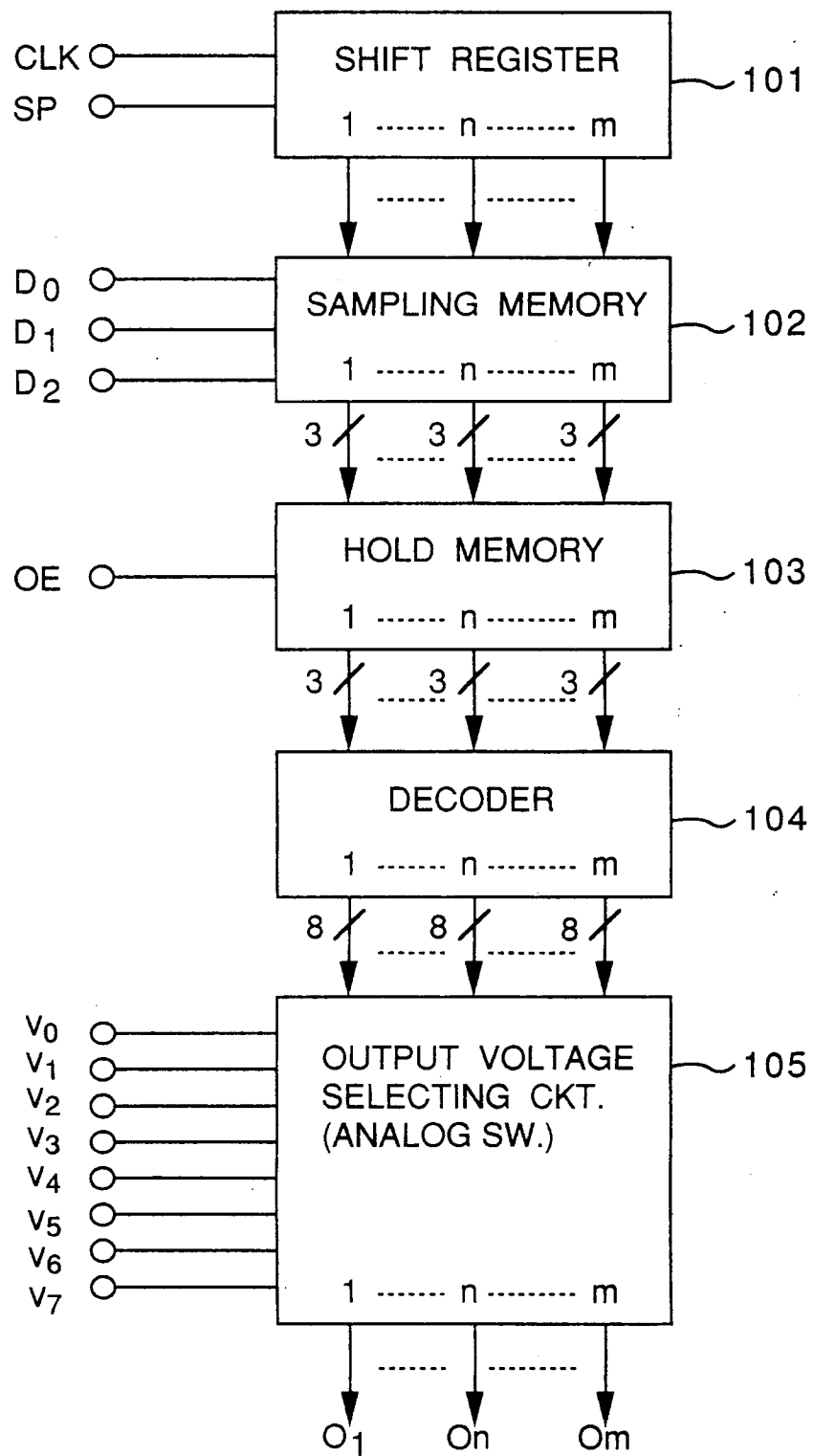
Fig.14 PRIOR ART

Fig.15 PRIOR ART

